Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h753vit6

Contents

3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

3.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

3.27 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.28 Cryptographic acceleration (CRYPT and HASH)

The devices embed a cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure confidentiality, authentication, data integrity and non-repudiation when exchanging messages with a peer:

- Encryption/Decryption
  - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
  - AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (Counter mode) chaining algorithms, 128, 192 or 256-bit key
- Universal HASH
  - SHA-1 and SHA-2 (secure HASH algorithms)
  - MD5
  - HMAC

The cryptographic accelerator supports DMA request generation.

3.29 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
High-resolution timer	HRTIM1	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes	400	400
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	200

Table 8. STM32H753xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	14	G3	J3	20	23	J5	PF4	I/O	FT_ha	-	FMC_A4, EVENTOUT	ADC3_INN5, ADC3_INP9
-	-	15	F5	K3	21	24	J4	PF5	I/O	FT_ha	-	FMC_A5, EVENTOUT	ADC3_INP4
10	-	16	B10	G2	22	25	C10	VSS	S	-	-	-	-
11	-	17	G1	G3	23	26	E9	VDD	S	-	-	-	-
-	-	18	G4	K2	24	27	K2	PF6	I/O	FT_ha	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, QUADSPI_BK1_IO3, EVENTOUT	ADC3_INN4, ADC3_INP8
-	-	19	F6	K1	25	28	K3	PF7	I/O	FT_ha	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT	ADC3_INP3
-	-	20	H4	L3	26	29	K4	PF8	I/O	FT_ha	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_INN3, ADC3_INP7
-	-	21	G5	L2	27	30	L4	PF9	I/O	FT_ha	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_INP2
-	-	22	H3	L1	28	31	L3	PF10	I/O	FT_ha	-	TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	ADC3_INN2, ADC3_INP6
12	C1	23	H1	G1	29	32	J2	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	D1	24	H2	H1	30	33	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
14	E1	25	G6	J1	31	34	K1	NRST	I/O	RST	-	-	-

Table 8. STM32H753xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
97	D4	141	D5	A4	169	200	C4	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, FDCAN1_RXFD_MODE, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	C4	142	D4	A3	170	201	B4	PE1	I/O	FT_h	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, FDCAN1_TXFD_MODE, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	-	A7	VCAP	S	-	-	-	-
99	-	-	-	D5	-	202	-	VSS	S	-	-	-	-
-	F7	143	C4	C6	171	203	E7	PDR_ON	S	-	-	-	-
-	F4	-	B4	-	-	-	A6	VDDLDO	S	-	-	-	-
100	-	144	-	C5	172	204	-	VDD	S	-	-	-	-
-	-	-	-	D4	173	205	A4	PI4	I/O	FT_h	-	TIM8_BKIN, SAI2_MCK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	C4	174	206	A3	PI5	I/O	FT_h	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	-	A4	C3	175	207	A2	PI6	I/O	FT_h	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	-	E2	C2	176	208	B3	PI7	I/O	FT_h	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-
-	-	-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K10	-	-	-	VSS	S	-	-	-	-

1. When this pin/ball was previously configured as an oscillator, the oscillator function is kept during and after a reset. This is valid for all resets except for power-on reset.
2. This ball should remain floating.

Table 9. Port A alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port A	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	HRTIM_FLT1	-	HDMI_CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS	-	-	UART7_TX	-	-	-	EVENT-OUT

Table 10. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENT-OUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENT-OUT
	PB2	-	-	SAI1_D1	-	DFSDM_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	QUADSPI_CLK	SAI4_D1	-	-	-	-	EVENT-OUT
	PB3	JTDO/TRACESWO	TIM2_CH2	HRTIM_FLT4	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	SDMMC2_D2	-	UART7_RX	-	-	-	EVENT-OUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	HRTIM_EEV6	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO	SDMMC2_D3	-	UART7_TX	-	-	-	EVENT-OUT
	PB5	-	TIM17_BKIN	TIM3_CH2	HRTIM_EEV7	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI	FDCAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	UART5_RX	EVENT-OUT
	PB6	-	TIM16_CH1N	TIM4_CH1	HRTIM_EEV8	I2C1_SCL	HDMI_CEC	I2C4_SCL	USART1_TX	LPUART1_TX	FDCAN2_TX	QUADSPI_BK1_NCS	DFSDM_DATIN5	FMC_SDNE1	DCMI_D5	UART5_TX	EVENT-OUT
	PB7	-	TIM17_CH1N	TIM4_CH2	HRTIM_EEV9	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	FDCAN2_TXFD_MODE	-	DFSDM_CKIN5	FMC_NL	DCMI_VSYNC	-	EVENT-OUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVENT-OUT

Table 15. Port G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/SPDIFRX	SAI2/4/TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD	I2C4/UART7/SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/COMP	UART5/ LCD	SYS
Port G	PG14	TRACED1	LPTIM1_ ETR	-	-	-	SPI6_ MOSI	-	USART6_ TX		QUADSPI_ BK2_IO3	-	ETH_MII_ TXD1/ETH_ RMII_TXD1	FMC_A25	-	LCD_ B0	EVENT-OUT
	PG15	-	-	-	-	-	-	-	USART6_ CTS_NSS	-	-	-	-	FMC_ SDNCAS	DCMI_ D13	-	EVENT-OUT

Table 21. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

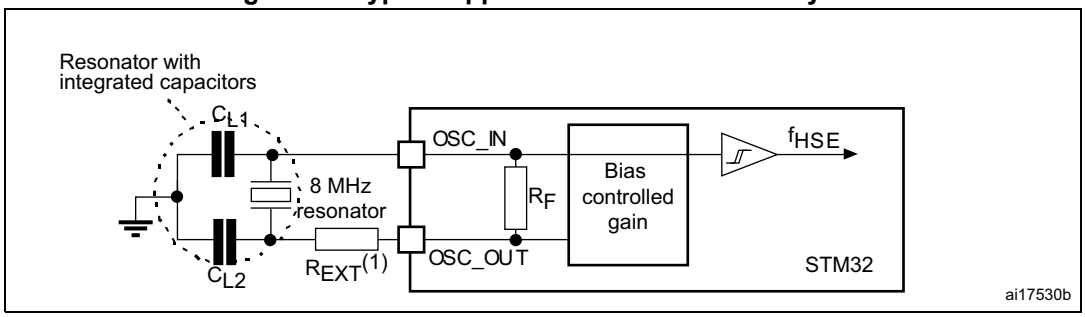
6.3.1 General operating conditions

Table 23. General operating conditions

Symbol	Parameter		Operating conditions	Min	Max	Unit
V_{DD}	Standard operating voltage		-	1.62(1)	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator		$V_{DDLDO} \le V_{DD}$	1.62(1)	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain		USB used	3.0	3.6	
			USB not used	0	3.6	
V_{DDA}	Analog operating voltage		ADC or COMP used	1.62	3.6	
			DAC used	1.8		
			OPAMP used	2.0		
			VREFBUF used	1.8		
			ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{IN}	I/O Input voltage		TT_xx I/O	−0.3	V_{DD}+0.3	
			BOOT0	0	9	
			All I/O except BOOT0 and TT_xx	−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$)+3.6V < 5.5V(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6(4)	TFBGA240+25	-	-	1093	mW
		LQFP208	-	-	943	
		LQFP176	-	-	930	
		UFBGA176+25	-	-	1070	
		UFBGA169	-	-	1061	
		LQFP144	-	-	915	
		LQFP100	-	-	889	
		TFBGA100	-	-	1018	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(5)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(5)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	125	°C

1. When RESET is released functionality is guaranteed down to V_{BOR0} min
2. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.

Figure 19. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. Low-speed external user clock characteristics(1)

Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 00, Low drive capability	-	290	-	nA
		LSEDRV[1:0] = 01, Medium Low drive capability	-	390	-	
		LSEDRV[1:0] = 10, Medium high drive capability	-	550	-	
		LSEDRV[1:0] = 11, High drive capability	-	900	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(3)	Startup time	VDD is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers.
3. t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Table 52. Flash memory programming (single bank configuration nDBANK=1)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580(2)	µs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-			
t_{ME}	Mass erase time	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

Table 53. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_J = –40 to +125 °C (6 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	20	

1. Guaranteed by characterization results.

Figure 26. Asynchronous multiplexed PSRAM/NOR write waveforms

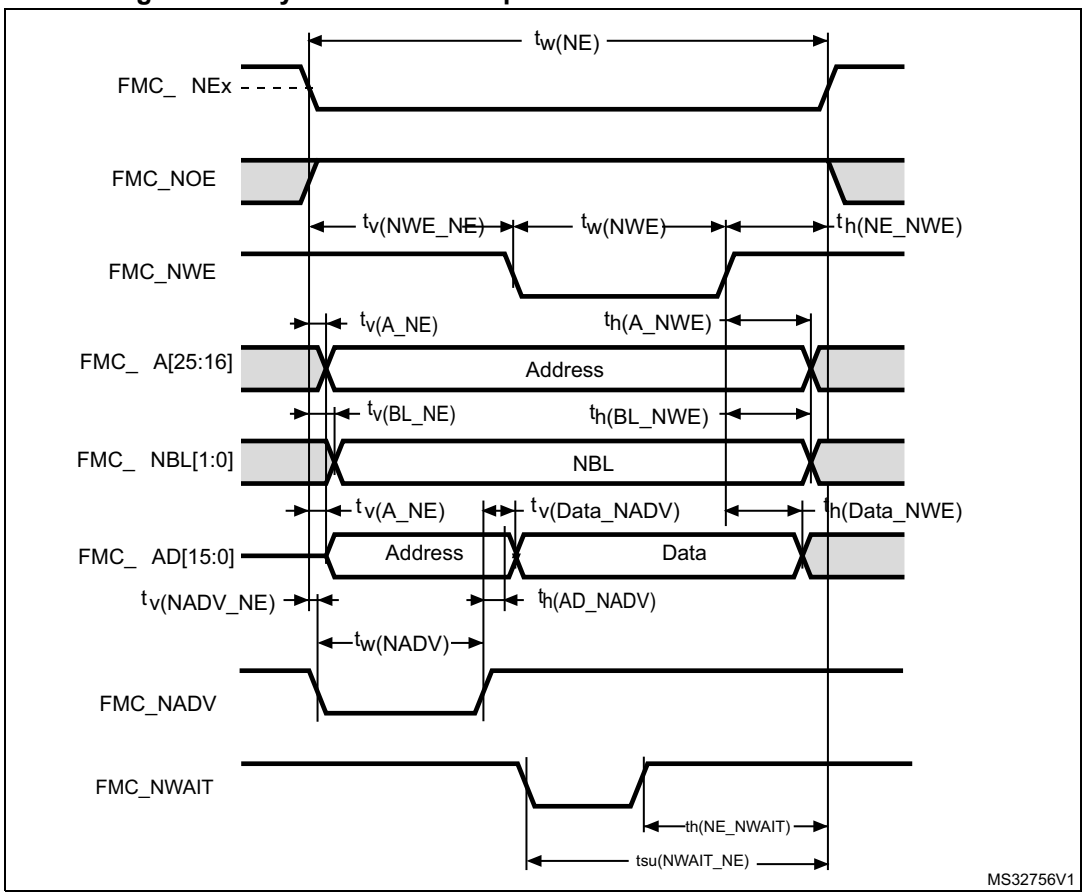


Table 70. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc\_ker\_c} - 1$	$4T_{fmc\_ker\_ck}$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_c} - 1$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc\_ker\_ck} - 0.5$	$2T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck}+0.5$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc\_ker\_ck}+0.5$	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc\_ker\_ck}+0.5$	-	

1. Guaranteed by characterization results.

Table 83. Quad SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{ck1/t(CK)}$	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	100	MHz
		1.62 V<V_{DD}<3.6 V CL=15 pF	-	-	100	
$t_{w(CKH)}$	Quad-SPI clock high and low time	-	$t_{(CK)}$/2 - 0.5	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$			$t_{(CK)}$/2	-	$t_{(CK)}$/2+0.5	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	2	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	3.5	4	
		DHHC=1 Pres=1, 2...	-	$t_{(CK)}$/4+3.5	$t_{(CK)}$/4+4	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHHC=0	3	-	-	
		DHHC=1 Pres=1, 2...	$t_{(CK)}$/4+3	-	-	

1. Guaranteed by characterization results.

Figure 37. Quad-SPI timing diagram - SDR mode

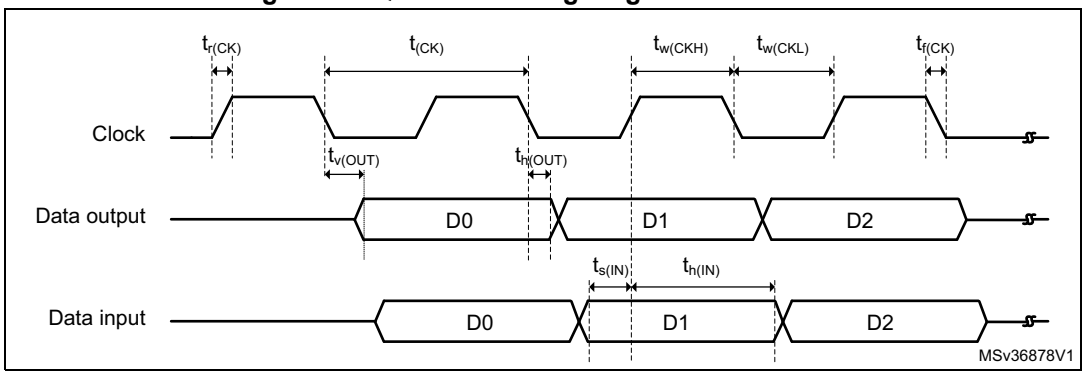


Figure 38. Quad-SPI timing diagram - DDR mode

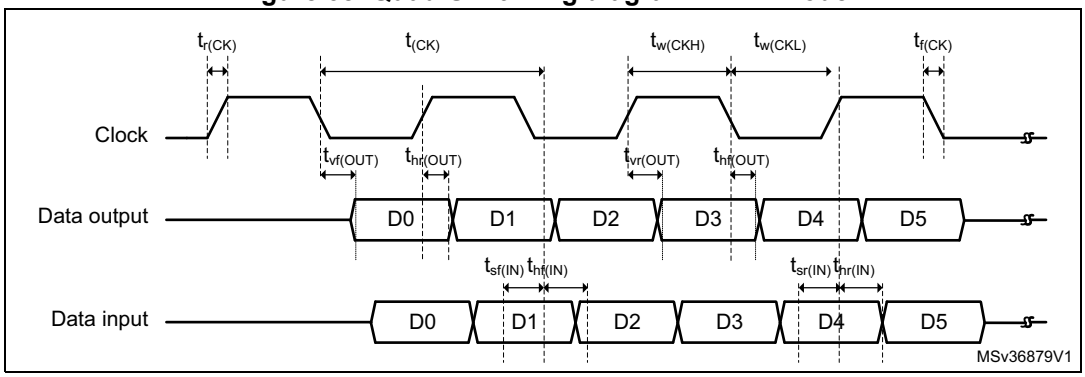


Table 86. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions(4)		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	BOOST = 1	-	±6	-	±LSB
			BOOST = 0	-	±8	-	
		Differential	BOOST = 1	-	±10	-	
			BOOST = 0	-	±16	-	
ED	Differential linearity error	Single ended	BOOST = 1	-	2	-	
			BOOST = 0	-	1	-	
		Differential	BOOST = 1	-	8	-	
			BOOST = 0	-	2	-	
EL	Integral linearity error	Single ended	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
		Differential	BOOST = 1	-	±6	-	
			BOOST = 0	-	±4	-	
ENOB(5)	Effective number of bits (2 MSPS)	Single ended	BOOST = 1	-	11.6	-	bits
			BOOST = 0	-	12	-	
		Differential	BOOST = 1	-	13.3	-	
			BOOST = 0	-	13.5	-	
SINAD(5)	Signal-to-noise and distortion ratio (2 MSPS)	Single ended	BOOST = 1	-	71.6	-	dB
			BOOST = 0	-	74	-	
		Differential	BOOST = 1	-	81.83	-	
			BOOST = 0	-	83	-	
SNR(5)	Signal-to-noise ratio (2 MSPS)	Single ended	BOOST = 1	-	72	-	
			BOOST = 0	-	74	-	
		Differential	BOOST = 1	-	82	-	
			BOOST = 0	-	83	-	
THD(5)	Total harmonic distortion	Single ended	BOOST = 1	-	−78	-	
			BOOST = 0	-	−80	-	
		Differential	BOOST = 1	-	−90	-	
			BOOST = 0	-	−95	-	

1. Guaranteed by characterization for BGA packages, the values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. The above table gives the ADC performance in 16-bit mode.
4. ADC clock frequency ≤ 36 MHz, 2 V ≤ V_{DDA} ≤3.3 V, 1.6 V ≤ V_{REF} ≤ V_{DDA}, BOOSTEN (for I/O) = 1.
5. ENOB, SINAD, SNR and THD are specified for V_{DDA} = V_{REF} = 3.3 V.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion

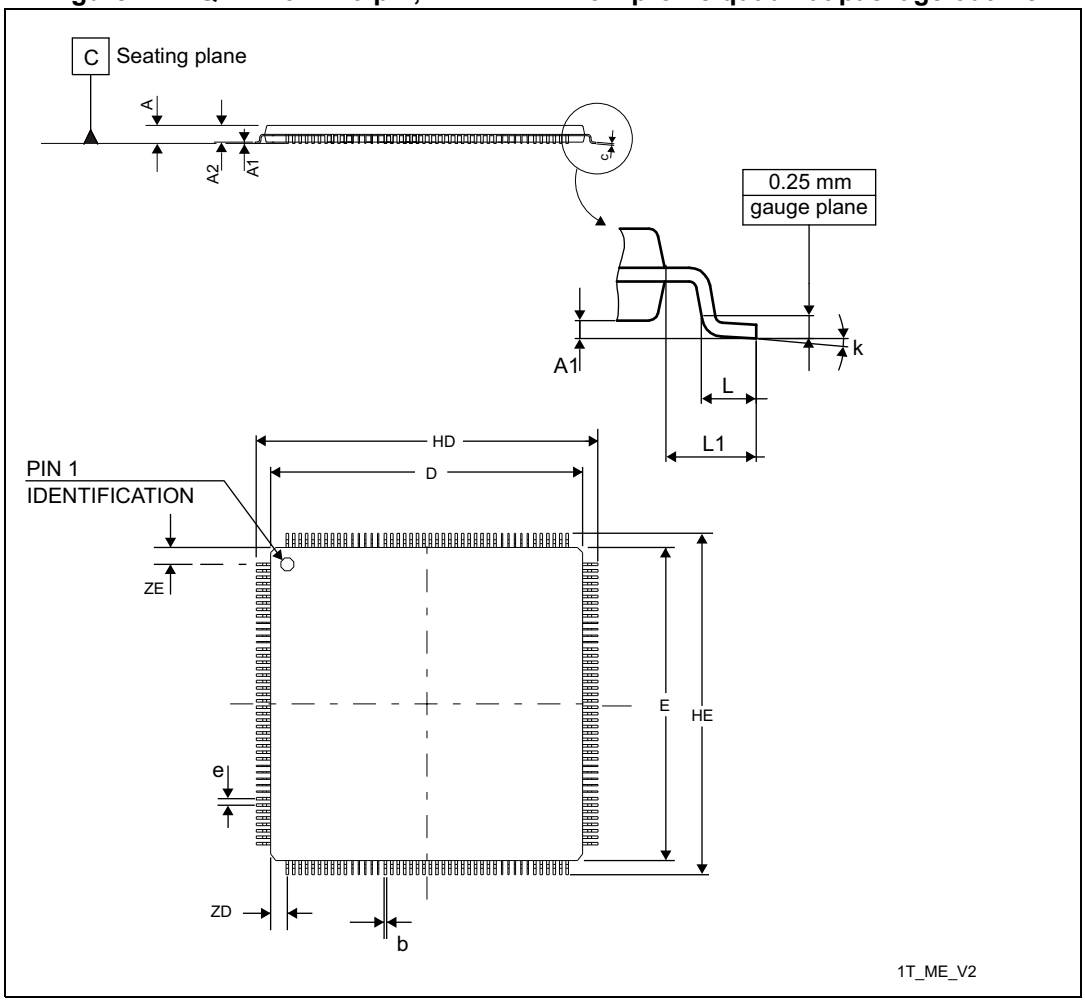
Table 120. UFBGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

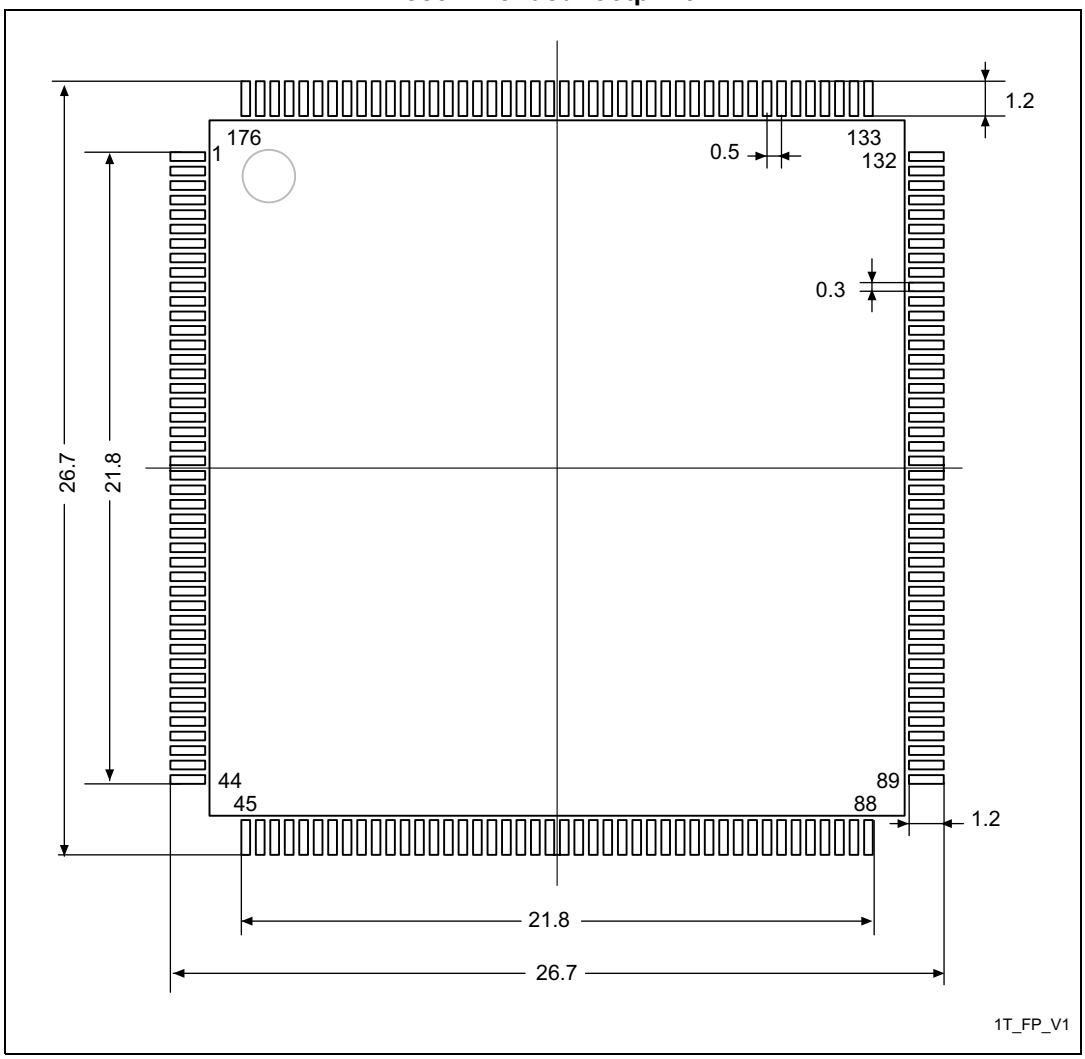
7.5 LQFP176 package information

Figure 74. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Figure 75. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package recommended footprint



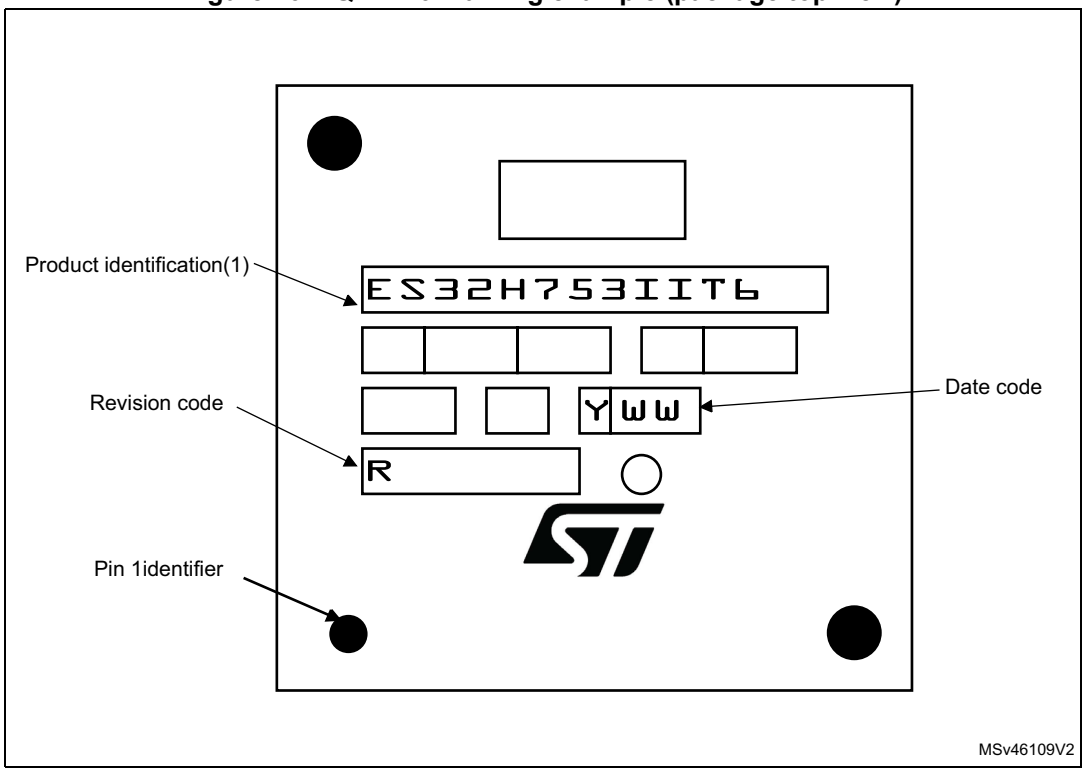
1. Dimensions are expressed in millimeters.

Device marking for LQFP176

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 76. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Table 122. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1811	1.1732	1.1890
D1	27.800	28.000	28.200	1.1024	1.0945	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1811	1.1732	1.1890
E1	27.800	28.000	28.200	1.1024	1.0945	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 126. TFBGA - 240+25ball recommended PCB design rules (0.8 mm pitch)

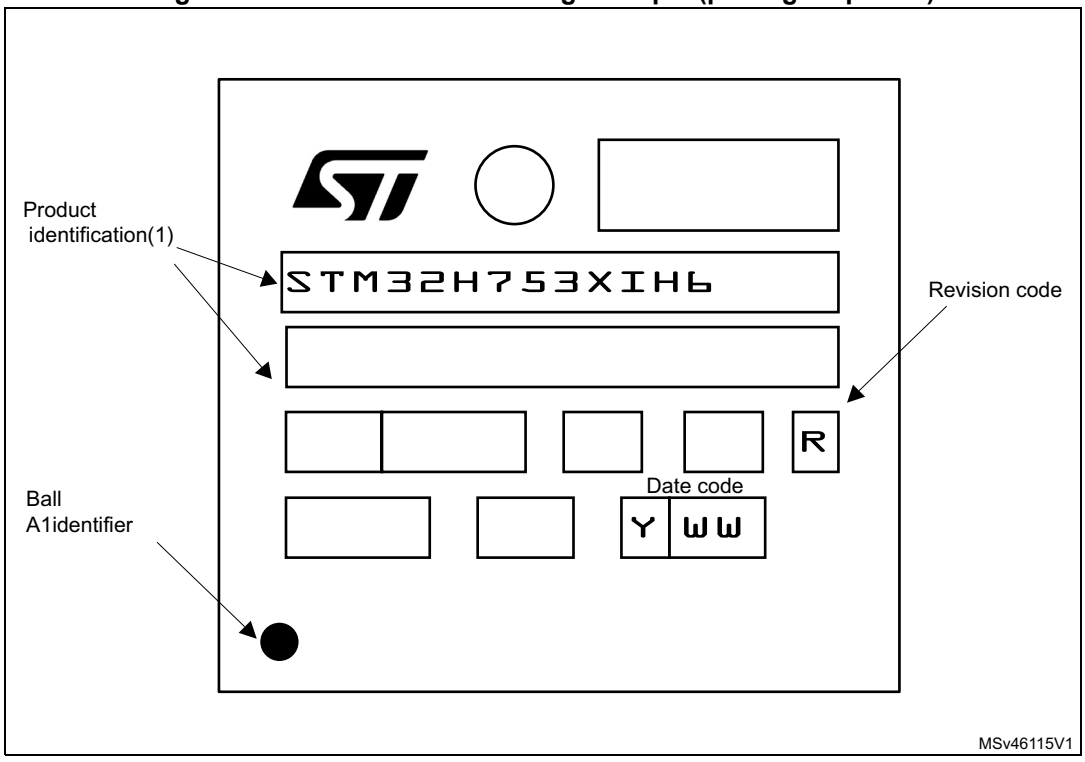
Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for TFBGA240+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 85. TFBGA240+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.