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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	265-TFBGA
Supplier Device Package	240+25-TFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h753xih6

3.29.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

The HRTIM1 timer is made of a digital kernel clocked at 400 MHz The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, Burst mode controller, Push-pull and Resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.34 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

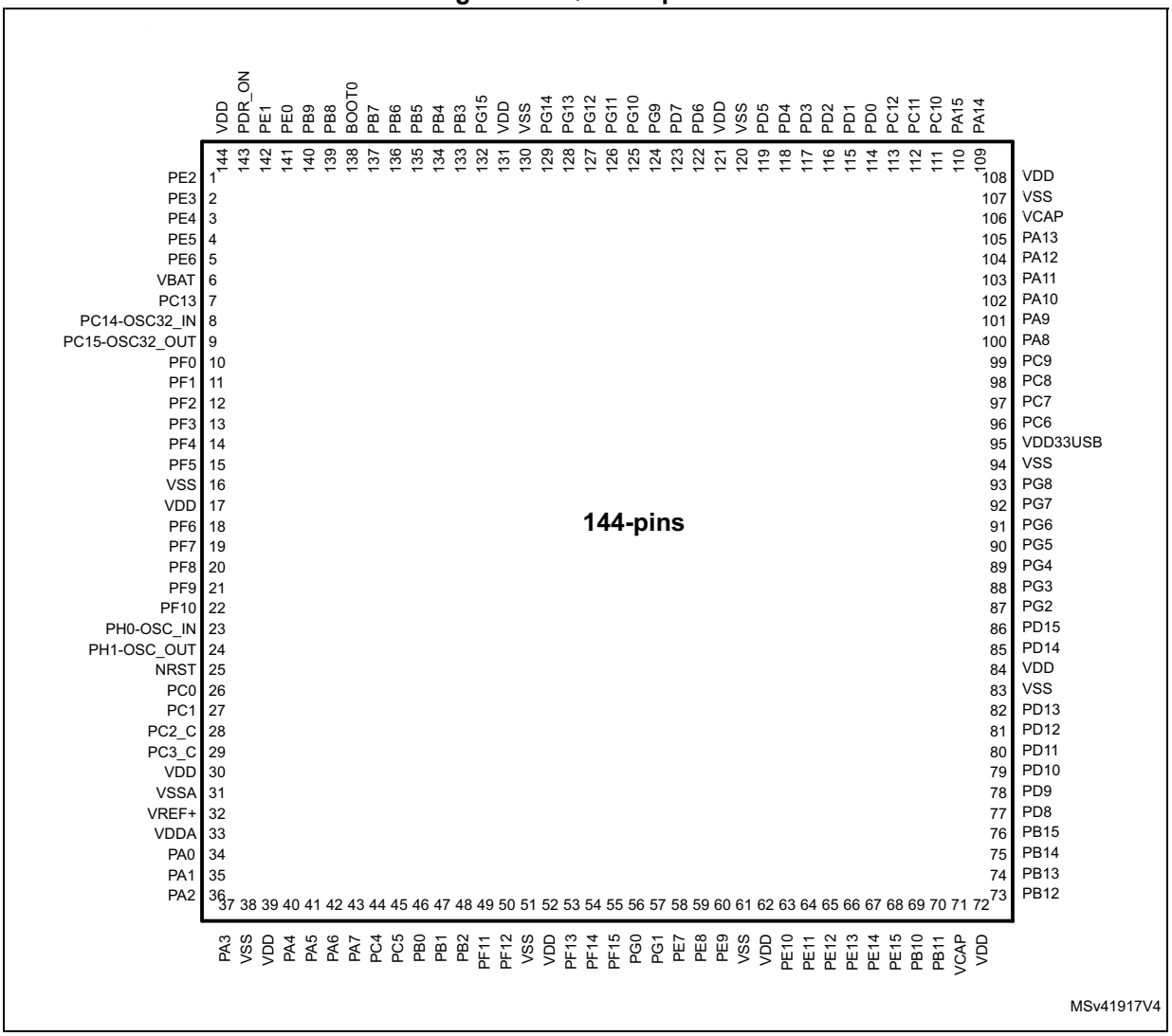
The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communicating up to 150 Mbits/s in Master and Slave modes, in Half-duplex, Full-duplex and Simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in Simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in Master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

3.35 Serial audio interfaces (SAI)

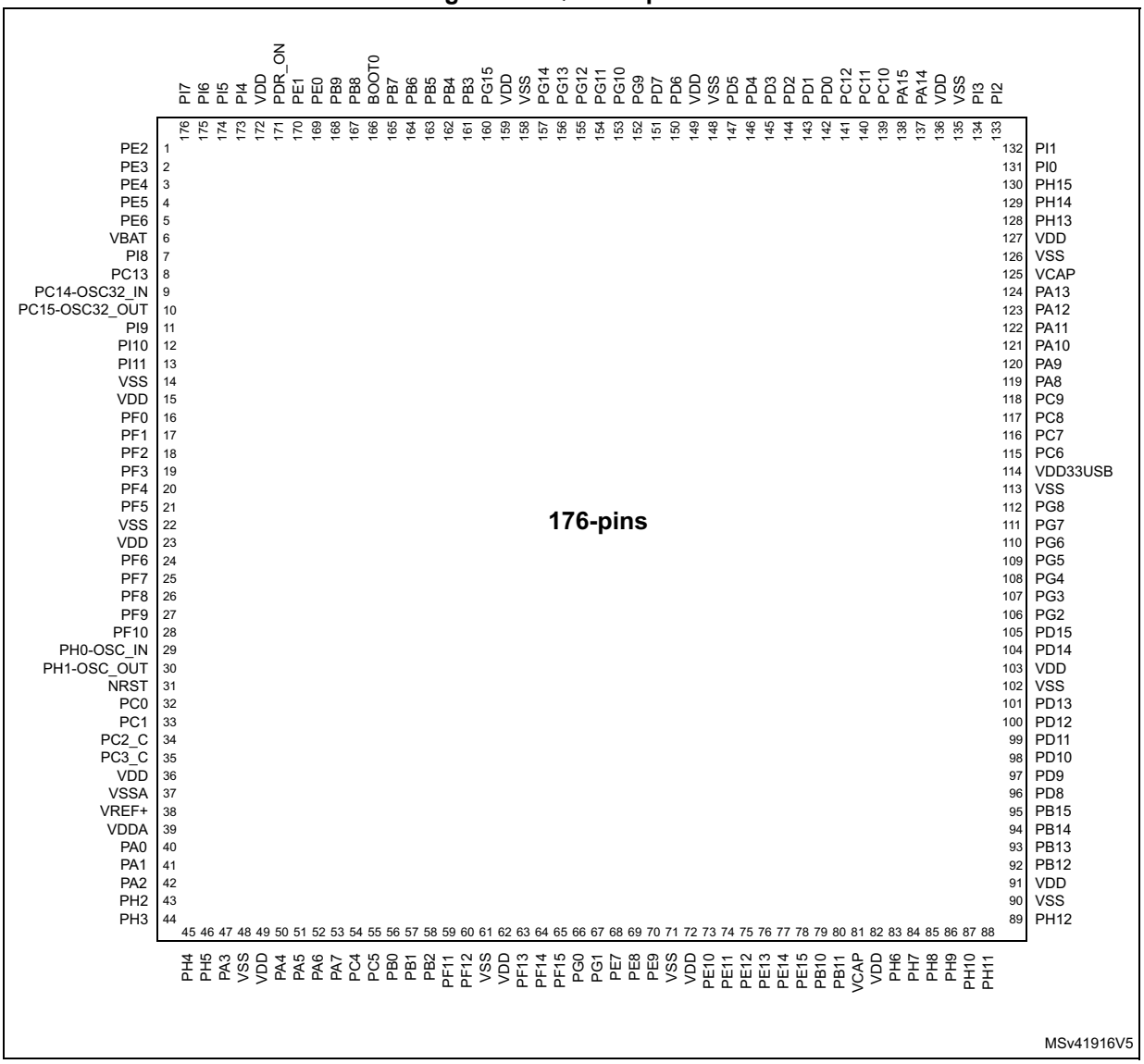
The devices embed 4 SAIs (SAI1, SAI2, SAI3 and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 8 microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

Figure 6. LQFP144 pinout



1. The above figure shows the package top view.

Figure 8. LQFP176 pinout



1. The above figure shows the package top view.

3. This ball should not remain floating. It can be connected to VSS or VDD. It is reserved for future use.
4. This ball should be connected to V_{SS}.
5. Pxy_C and Pxy pins/balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
6. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
7. VREF+ pin, and consequently the internal voltage reference, are not available on the TFBGA100 package. On this package, this pin is double-bonded to VDDA which can be connected to an external reference. The internal voltage reference buffer is not available and must be kept disabled

Table 9. Port A alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port A	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	HRTIM_FLT1	-	HDMI_CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS	-	-	UART7_TX	-	-	-	EVENT-OUT

Table 10. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENT-OUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENT-OUT
	PB2	-	-	SAI1_D1	-	DFSDM_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	QUADSPI_CLK	SAI4_D1	-	-	-	-	EVENT-OUT
	PB3	JTDO/TRACESWO	TIM2_CH2	HRTIM_FLT4	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	SDMMC2_D2	-	UART7_RX	-	-	-	EVENT-OUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	HRTIM_EEV6	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO	SDMMC2_D3	-	UART7_TX	-	-	-	EVENT-OUT
	PB5	-	TIM17_BKIN	TIM3_CH2	HRTIM_EEV7	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI	FDCAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	UART5_RX	EVENT-OUT
	PB6	-	TIM16_CH1N	TIM4_CH1	HRTIM_EEV8	I2C1_SCL	HDMI_CEC	I2C4_SCL	USART1_TX	LPUART1_TX	FDCAN2_TX	QUADSPI_BK1_NCS	DFSDM_DATIN5	FMC_SDNE1	DCMI_D5	UART5_TX	EVENT-OUT
	PB7	-	TIM17_CH1N	TIM4_CH2	HRTIM_EEV9	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	FDCAN2_TXFD_MODE	-	DFSDM_CKIN5	FMC_NL	DCMI_VSYNC	-	EVENT-OUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	FDCAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVENT-OUT

Table 15. Port G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/SPDIFRX	SAI2/4/TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD	I2C4/UART7/SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/COMP	UART5/ LCD	SYS
Port G	PG14	TRACED1	LPTIM1_ ETR	-	-	-	SPI6_ MOSI	-	USART6_ TX		QUADSPI_ BK2_IO3	-	ETH_MII_ TXD1/ETH_ RMII_TXD1	FMC_A25	-	LCD_ B0	EVENT-OUT
	PG15	-	-	-	-	-	-	-	USART6_ CTS_NSS	-	-	-	-	FMC_ SDNCAS	DCMI_ D13	-	EVENT-OUT

Table 17. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	FDCAN1_RXFD_MODE	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT-OUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_D25	DCMI_D8	LCD_G6	EVENT-OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT-OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENT-OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	TIM8_BKIN_COMP12	FMC_NBL2	DCMI_D5	LCD_B4	EVENT-OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENT-OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENT-OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENT-OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENT-OUT
	PI10	-	-	-	-	-	-	-	-	-	FDCAN1_RXFD_MODE	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENT-OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENT-OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENT-OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENT-OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT-OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT-OUT

6.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 26. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	-	µs
V_{BOR0}	Brown-out reset threshold 0	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	Hysteresis in Run mode	-	100	-	mV
$I_{DD\_BOR\_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}	-	-		0.630	µA

Table 37. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ(1)				Max (3 V)				Unit
		Backup SRAM	RTC & LSE	1.2 V	2 V	3 V	3.4 V	T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD} (VBAT)	Supply current in standby mode	OFF	OFF	0.024	0.035	0.062	0.096	0.5(1)	4.1(1)	10(1)	24(1)	µA
		ON	OFF	1.4	1.6	1.8	1.8	4.4(1)	22(1)	48(1)	87(1)	
		OFF	ON	0.24	0.45	0.62	0.73	-	-	-	-	
		ON	ON	1.97	2.37	2.57	2.77	-	-	-	-	

1. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 59: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 38: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

Table 49. PLL characteristics (wide VCO frequency range)(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LOCK}	PLL lock time	Normal mode		-	50(3)	150(3)	µs
		Sigma-delta mode (CKIN ≥ 8 MHz)		-	58(3)	166(3)	
Jitter	Cycle-to-cycle jitter	VCO = 192 MHz		-	134	-	±ps
		VCO = 200 MHz		-	134	-	
		VCO = 400 MHz		-	76	-	
		VCO = 800 MHz		-	39	-	
	Long term jitter	Normal mode		-	±0.7	-	%
		Sigma-delta mode (CKIN = 16 MHz)		-	±0.8	-	
$I_{DD(PLL)}$(3)	PLL power consumption on V_{DD}	VCO freq = 836 MHz	V_{DDA}	-	590	1500	µA
			V_{CORE}	-	720	-	
		VCO freq = 192 MHz	V_{DDA}	-	180	600	
			V_{CORE}	-	280	-	

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation (400 MHz for VOS1, 300 MHz for VOS2, 200 MHz for VOS3).
3. Guaranteed by characterization results.

Table 50. PLL characteristics (medium VCO frequency range)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	1	-	2	MHz
	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	Voltage scaling Range 1	1.17	-	210	MHz
		Voltage scaling Range 2	1.17	-	210	
		Voltage scaling Range 3	1.17	-	200	
f_{VCO_OUT}	PLL VCO output	-	150	-	420	MHz
t_{LOCK}	PLL lock time	Normal mode	-	60(2)	100(2)	µs
		Sigma-delta mode	forbidden	-	-	µs

Table 61. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	85	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	35	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	110	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	40	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	166	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	100	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	3.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	6.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.8	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.2	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	1.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.3	
11	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	100	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	50	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	133	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	66	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	220	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	85	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	3.3	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	6.6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.4	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	1.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.7	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 59: I/O static characteristics*).

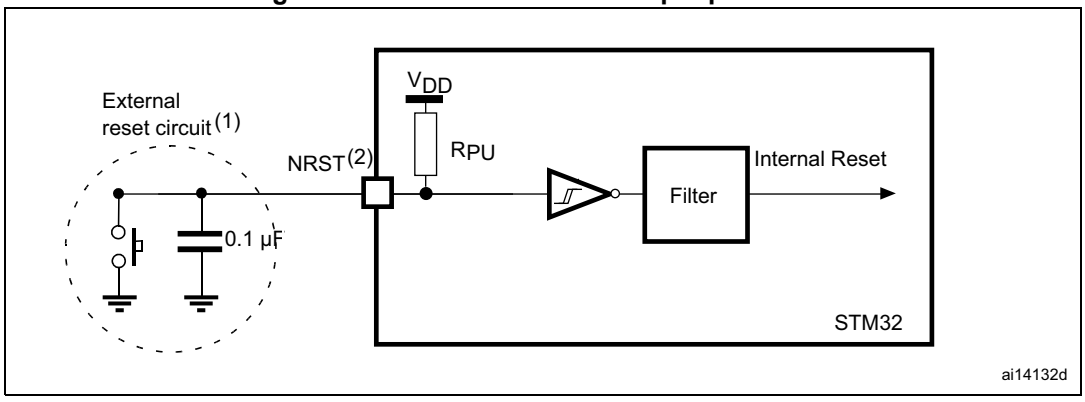
Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 63. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	300	-	-	
		1.62 V < V_{DD} < 3.6 V	1000	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 63*. Otherwise the reset is not taken into account by the device.

Table 71. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc\_ker\_ck} - 1$	$9T_{fmc\_ker\_ck}$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc\_ker\_ck} - 0.5$	$7T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{fmc\_ker\_ck} + 3$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc\_ker\_ck}$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 27 through *Figure 30* represent synchronous waveforms and *Table 72* through *Table 75* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 2.7 V<V_{DD}<3.6 V, FMC_CLK =133 MHz at 20 pF
- For 1.8 V<V_{DD}<1.9 V, FMC_CLK =100 MHz at 20 pF
- For 1.62 V<V_{DD}<1.8 V, FMC_CLK =100 MHz at 15 pF

Table 73. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	2.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

6.3.28 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 97* for DFSDM are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDMx_CKINx, DFSDMx_DATINx, DFSDMx_CKOUT for DFSDMx).

Table 97. DFSDM measured timing 1.62-3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.62 V < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 V < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.62 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	20 ($f_{DFSDMCLK}$/4)	
f_{CKOUT}	Output clock frequency	1.62 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	45	50	55	%

Table 97. DFSDM measured timing 1.62-3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	TCKIN/2 - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	4	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.62 < V_{DD} < 3.6 V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

1. Guaranteed by characterization results.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 104* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- I/O compensation cell enabled

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 104. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	MHz
		Slave data	-	64xFs	
$t_{v(WS)}$	WS valid time	Master mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

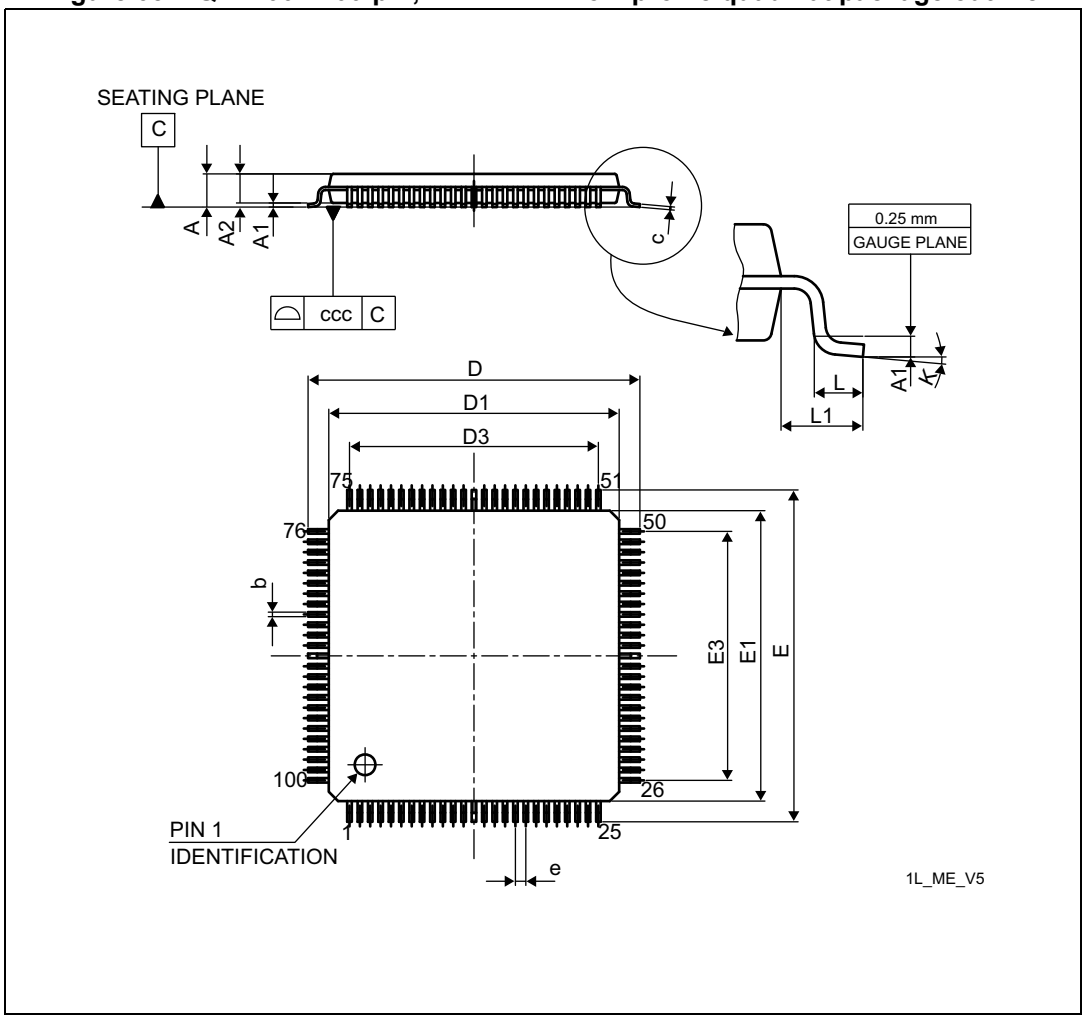
1. Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP100 package information

Figure 65. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 119. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.