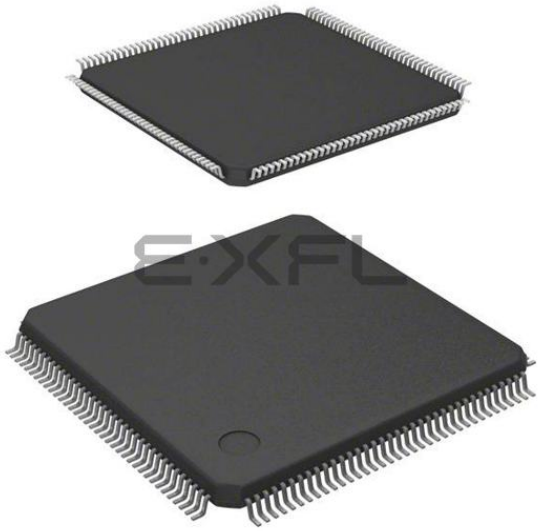

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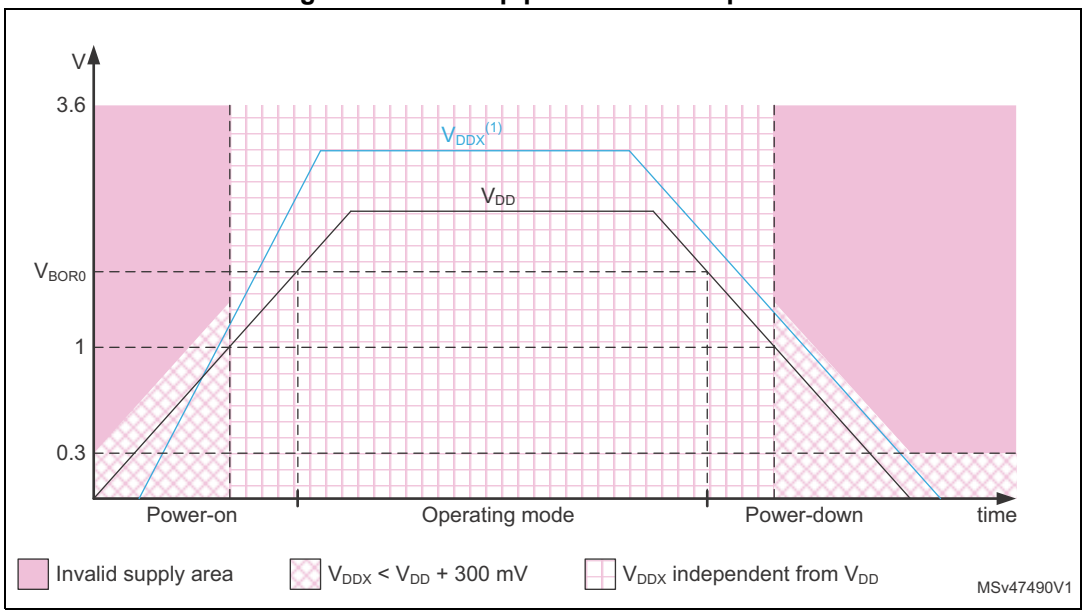
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h753zit6

Figure 2. Power-up/power-down sequence



1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$.

3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in Reset mode when V_{DD} is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

3.10 DMA controllers

. The devices feature four DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.
- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved on interrupt entry, and restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events .

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, HRTIM1 and LPTIM1 timer.

3.18 Temperature sensor

STM32H753xI devices embed a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from − 40 to +125 °C.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the System memory area, which is accessible in Read-only mode.

3.19 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{DD} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

3.31 Inter-integrated circuit interface (I2C)

STM32H753xI devices embed four I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.32 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H753xI devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 6* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire Half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 12.5 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

Figure 9. UFBGA176+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD 33USB	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	VSS								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2_C	PC3_C	PB2	PG1	VSS	VSS	VCAP	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

MSv41912V3

1. The above figure shows the package top view.

Table 8. STM32H753xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	K3	H4	45	48	P3	PH4	I/O	FT_fa	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_INN14, ADC3_INP15
-	-	-	L3	J4	46	49	P4	PH5	I/O	FT_fa	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INN15, ADC3_INP16
25	K2	37	N3	R2	47	50	U2	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC12_INP15
26	-	38	G2	K6	-	51	F2(4)	VSS	S	-	-	-	-
-	-	-	-	L4	48	-	-	VSS	S	-	-	-	-
27	-	39	-	K4	49	52	G5	VDD	S	-	-	-	-
28	G3	40	H6	N4	50	53	U3	PA4	I/O	TT_a	-	TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
29	H3	41	L4	P4	51	54	T3	PA5	I/O	TT_ha	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_INN18, ADC12_INP19, DAC1_OUT2
30	J3	42	K5	P3	52	55	R3	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_INP3

Table 8. STM32H753xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
44	G7	67	J9	P11	77	88	U10	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
45	H7	68	N9	R11	78	89	R11	PE15	I/O	FT_h	-	TIM1_BKIN, HDMI__TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12, LCD_R7, EVENTOUT	-
46	J7	69	L9	R12	79	90	P11	PB10	I/O	FT_f	-	TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	K7	70	M9	R13	80	91	P12	PB11	I/O	FT_f	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
48	F8	71	N10	M10	81	92	U11	VCAPVCAP	S	-	-	-	-
49	E4	-	-	K7	-	93	L15	VSS	S	-	-	-	-
-	-	-	M10	-	-	-	U12	VDDLDO	S	-	-	-	-
50	-	72	M1	N10	82	94	L13	VDD	S	-	-	-	-
-	-	-	-	-	-	95	R12	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	T11	PH6	I/O	FT	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	-	-	N12	84	97	U13	PH7	I/O	FT_fa	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-

Table 10. Port B alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7	LCD_B7	EVENT-OUT
	PB10	-	TIM2_CH3	HRTIM_SCOUT	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM_DATIN7	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENT-OUT
	PB11	-	TIM2_CH4	HRTIM_SCIN	LPTIM2_ETR	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	LCD_G5	EVENT-OUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM_DATIN1	USART3_CK	-	FDCAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	TIM1_BKIN_COMP12	UART5_RX	EVENT-OUT
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	-	SPI2_SCK/I2S2_CK	DFSDM_CKIN1	USART3_CTS_NSS	-	FDCAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	UART5_TX	EVENT-OUT
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SDI	DFSDM_DATIN2	USART3_RTS	UART4_RTS	SDMMC2_D0	-	-	OTG_HS_DM	-	-	EVENT-OUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM_CKIN2	-	UART4_CTS	SDMMC2_D1	-	-	OTG_HS_DP	-	-	EVENT-OUT

6.3 Operating conditions

6.3.1 General operating conditions

Table 23. General operating conditions

Symbol	Parameter		Operating conditions	Min	Max	Unit
V_{DD}	Standard operating voltage		-	1.62(1)	3.6	V
V_{DDLDO}	Supply voltage for the internal regulator		$V_{DDLDO} \le V_{DD}$	1.62(1)	3.6	
$V_{DD33USB}$	Standard operating voltage, USB domain		USB used	3.0	3.6	
			USB not used	0	3.6	
V_{DDA}	Analog operating voltage		ADC or COMP used	1.62	3.6	
			DAC used	1.8		
			OPAMP used	2.0		
			VREFBUF used	1.8		
			ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{IN}	I/O Input voltage		TT_xx I/O	−0.3	V_{DD}+0.3	
			BOOT0	0	9	
			All I/O except BOOT0 and TT_xx	−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$)+3.6V < 5.5V(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6(4)	TFBGA240+25	-	-	1093	mW
		LQFP208	-	-	943	
		LQFP176	-	-	930	
		UFBGA176+25	-	-	1070	
		UFBGA169	-	-	1061	
		LQFP144	-	-	915	
		LQFP100	-	-	889	
		TFBGA100	-	-	1018	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(5)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(5)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	125	°C

1. When RESET is released functionality is guaranteed down to V_{BOR0} min
2. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.

Figure 29. Synchronous non-multiplexed NOR/PSRAM read timings

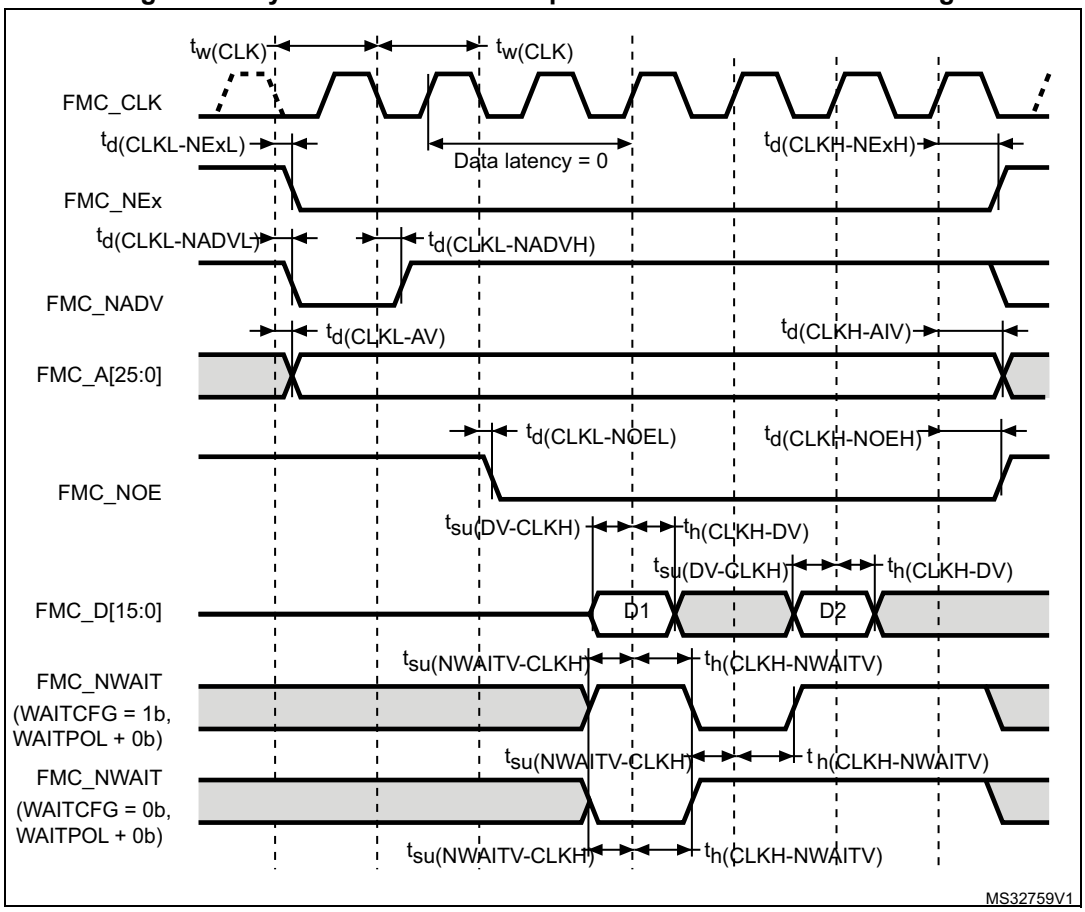


Table 74. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 34. NAND controller waveforms for common memory write access

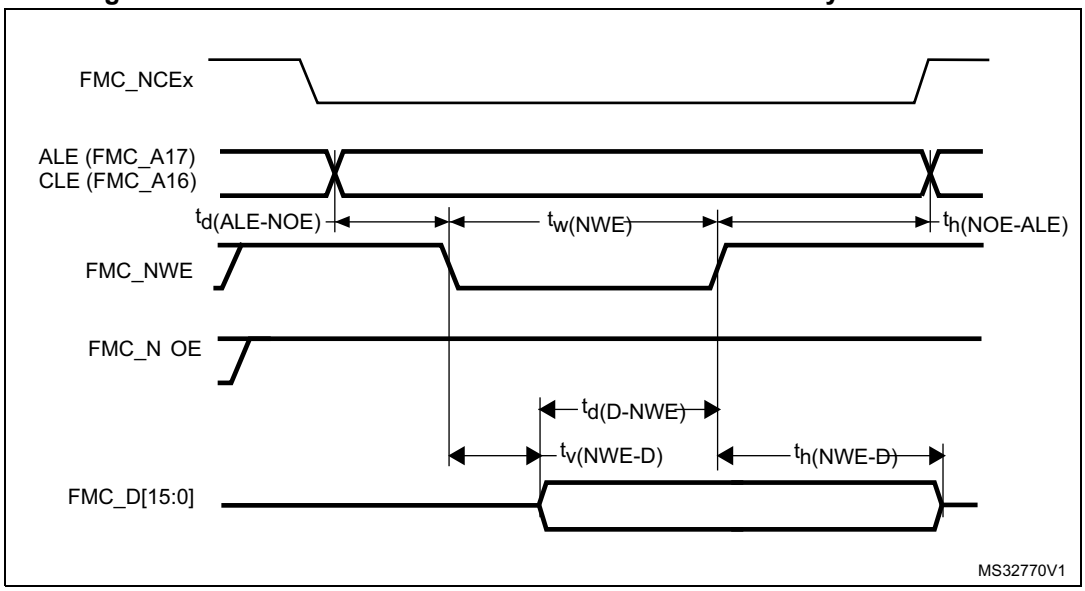


Table 76. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	8	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc\_ker\_ck} + 1$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc\_ker\_ck} - 2$	-	

1. Guaranteed by characterization results.

Table 77. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc\_ker\_ck} - 0.5$	$4T_{fmc\_ker\_ck} + 0.5$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc\_ker\_ck} - 0.5$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc\_ker\_ck} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc\_ker\_ck} - 1$	-	

1. Guaranteed by characterization results.

6.3.22 Voltage reference buffer characteristics

Table 89. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VSCALE = 000	2.8	3.3	3.6	V
			VSCALE = 001	2.4	-	3.6	
			VSCALE = 010	2.1	-	3.6	
			VSCALE = 011	1.8	-	3.6	
		Degraded mode	VSCALE = 000	1.62	-	2.80	
			VSCALE = 001	1.62	-	2.40	
			VSCALE = 010	1.62	-	2.10	
			VSCALE = 011	1.62	-	1.80	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode	VSCALE = 000	-	2.5	-	
			VSCALE = 001	-	2.048	-	
			VSCALE = 010	-	1.8	-	
			VSCALE = 011	-	1.5	-	
		Degraded mode(2)	VSCALE = 000	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 001	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 010	V_{DDA}– 150 mV	-	V_{DDA}	
			VSCALE = 011	V_{DDA}– 150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.2	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent Serial Resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40 °C < T_J < +125 °C	-	-	-	T_{coeff} xV_{REFINT} + 75	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100KHz	-	-	40	-	

Figure 44. Channel transceiver timing diagrams

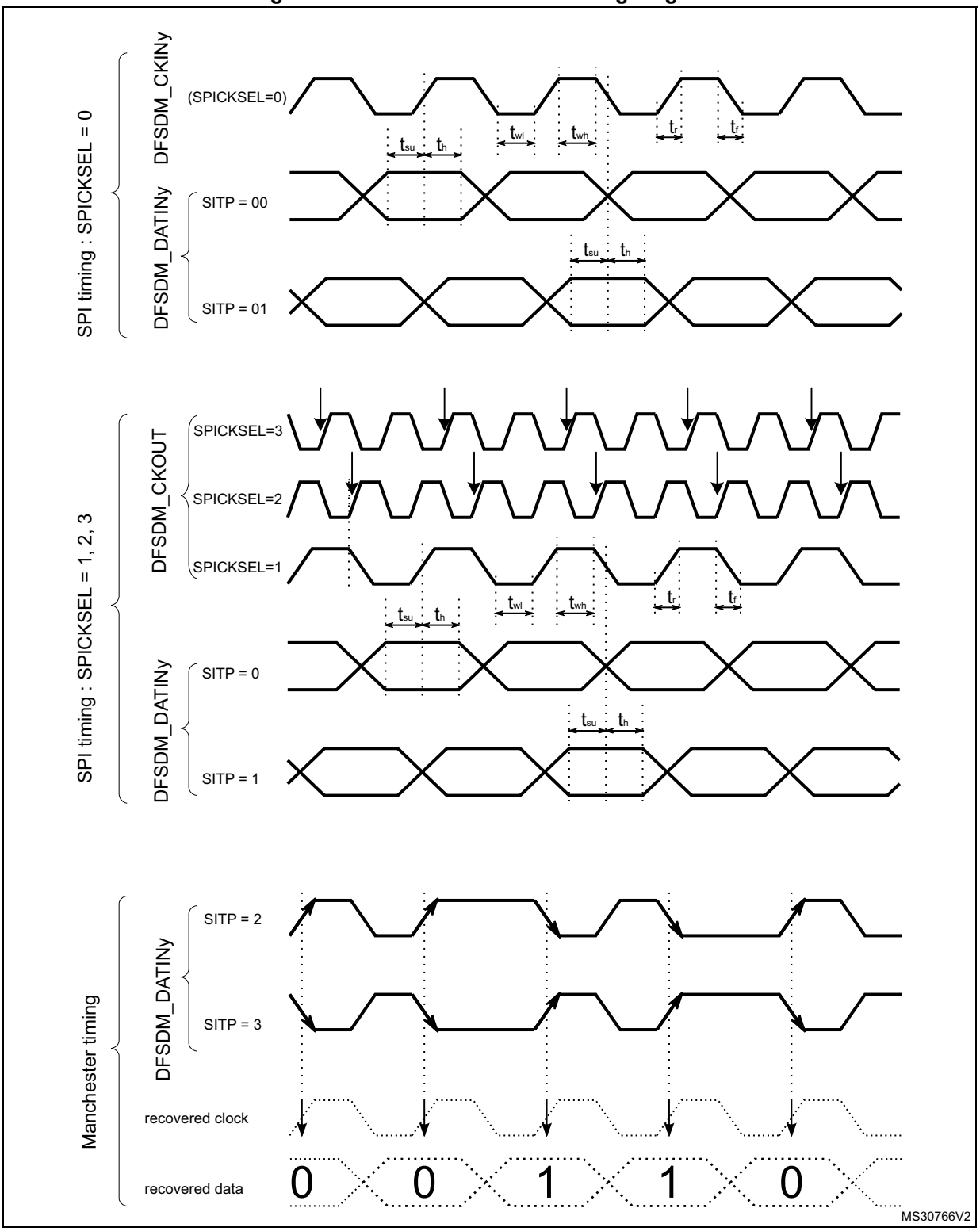


Table 103. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	13	27	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 V≤V_{DD}≤3.6 V	-	11.5	16	
		Slave mode 1.62 V≤V_{DD}≤3.6 V	-	13	20	
$t_{v(MO)}$		Master mode	-	1	3	
$t_{h(SO)}$	Data output hold time	Slave mode, 1.62 V≤V_{DD}≤3.6 V	9	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Figure 48. SPI timing diagram - slave mode and CPHA = 0

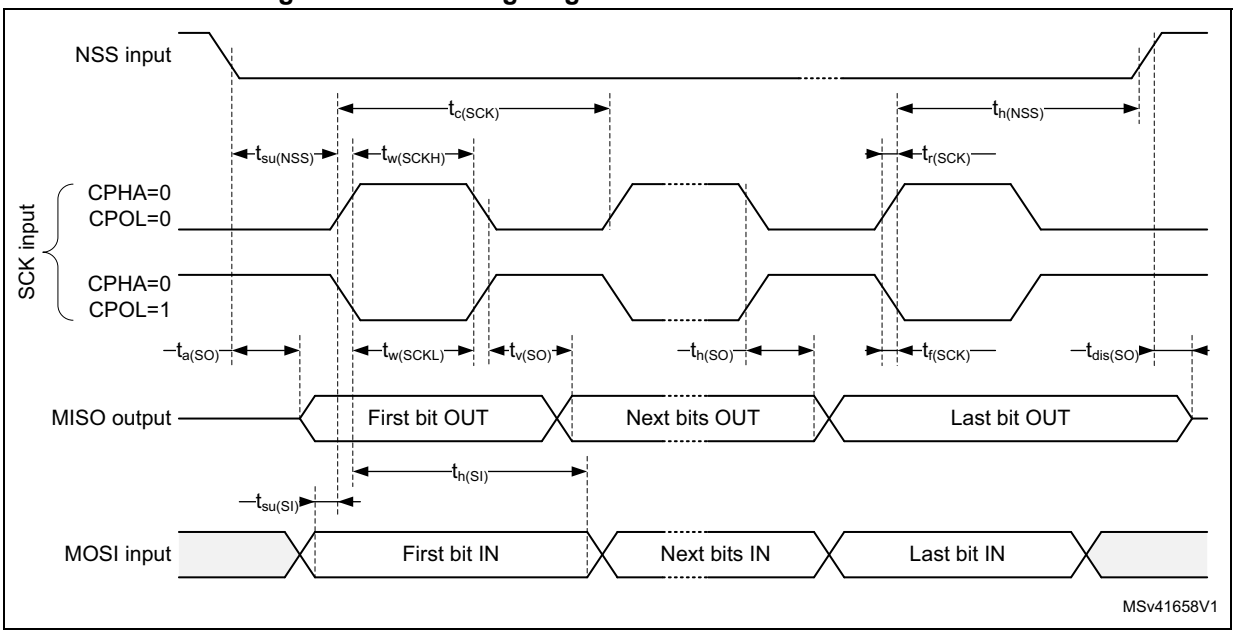
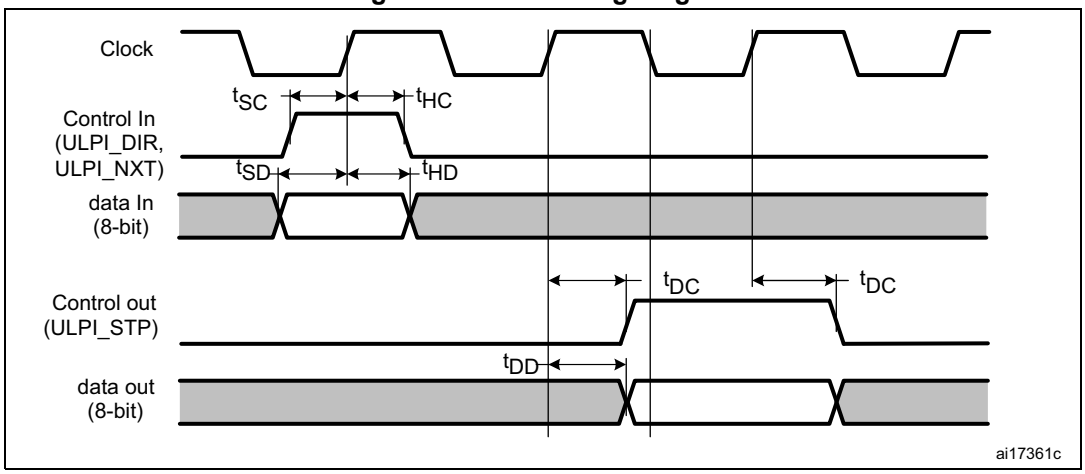


Figure 59. ULPI timing diagram



Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 111*, *Table 112* and *Table 113* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 111 gives the list of Ethernet MAC signals for the SMI and *Figure 60* shows the corresponding timing diagram.

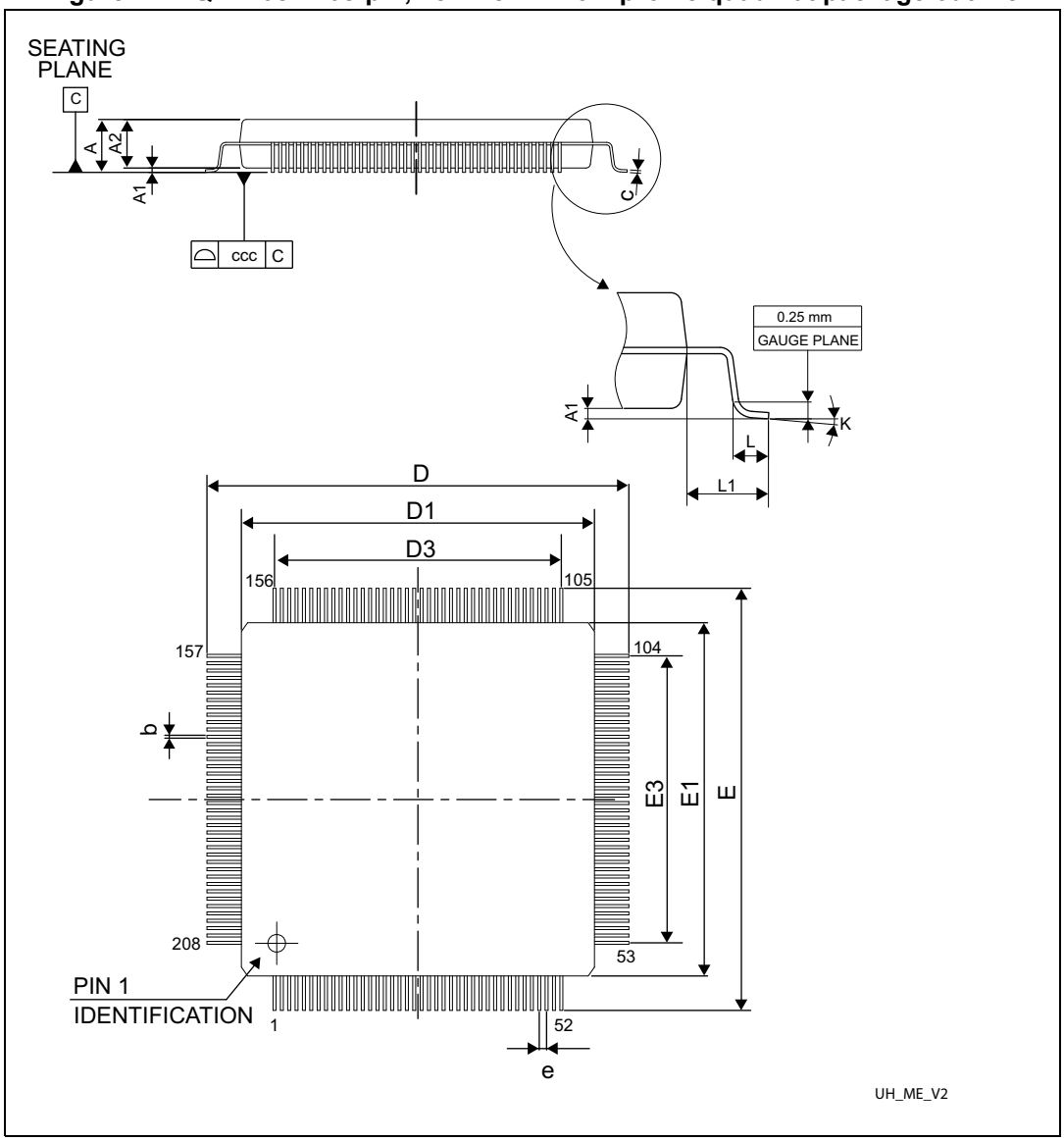
Table 111. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	1	1.5	3	
$t_{su(MDIO)}$	Read data setup time	8	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

7.6 LQFP208 package information

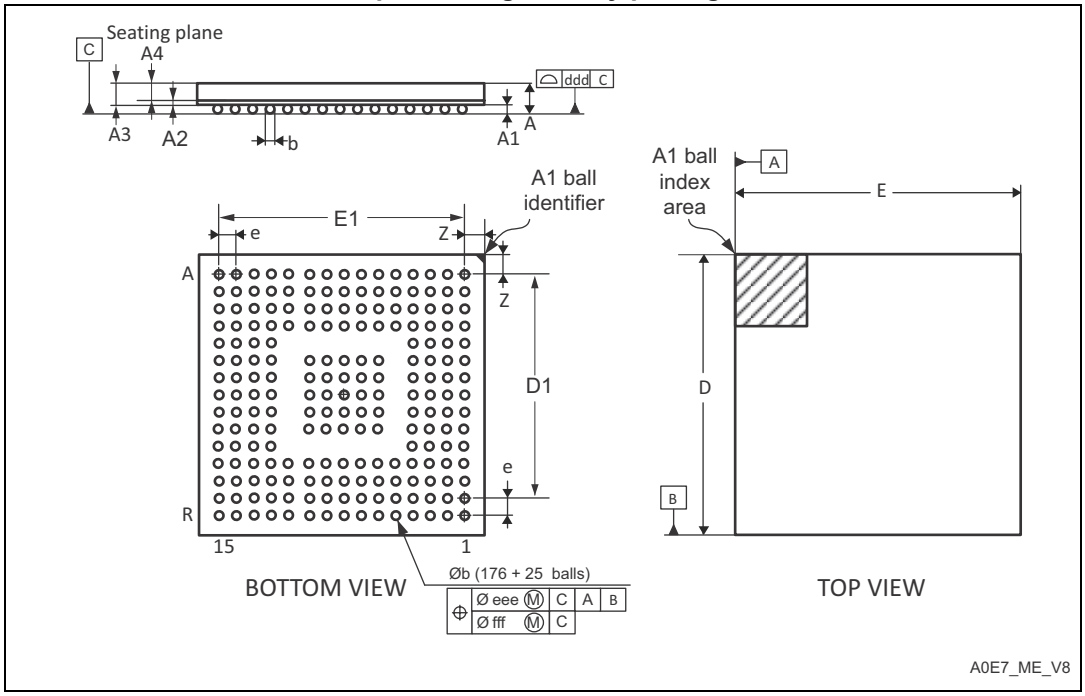
Figure 77. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.7 UFBGA176+25 package information

Figure 80. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 123. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 126. TFBGA - 240+25ball recommended PCB design rules (0.8 mm pitch)

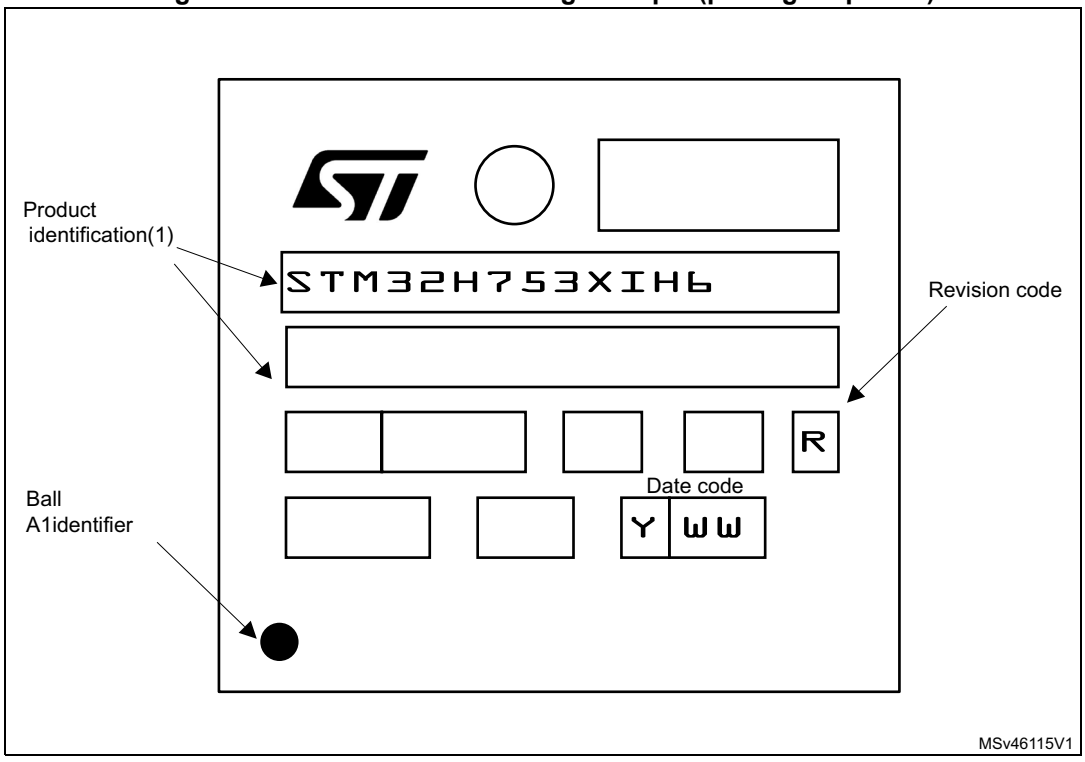
Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for TFBGA240+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 85. TFBGA240+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Table 129. Document revision history

Date	Revision	Changes
18-May-2018	4	Updated LSI clock frequency and ADC on cover page. Removed note related to UFBGA169 package. Updated ADC features on cover page and in *Table 2: STM32H753xI features and peripheral counts*. Added Arm trademark notice in *Section 1: Introduction*. Updated USB OTG interfaces to add crystal-less capability. Updated *Figure 1: STM32H753xI block diagram*. Updated GPIO default mode in *Section 3.8: General-purpose input/outputs (GPIOs)*. Added ADC sampling rate values in *Section 3.17: Analog-to-digital converters (ADCs)*. Updated *Section 3.18: Temperature sensor*. Updated LCD-TFT FIFO Size in *Section 3.25: LCD-TFT controller*. *Section 3.34: Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)*: changed maximum SPI frequency to 150 Mbits/s. Modified number of bidirectional endpoints in *Section 3.41: Universal serial bus on-the-go high-speed (OTG_HS)*. *Table 8: STM32H753xI pin/ball definition*: – Updated PC14 and PC15 function after reset. – Changed CAN1_TX/RX to FDCAN1_TX/RX and CAN1_TXFD/RXFD to FDCAN1_TXFD_MODE/RXFD_MODE – Changed CAN2_TX/RX to FDCAN2_TX/RX and CAN2_TXFD/RXFD to FDCAN2_TXFD_MODE/RXFD_MODE Replaced VCAP1/2/3 and VDDLDO1/2/3 by VCAP and VDDLDO, respectively. Updated PA0, PA13, PA14, PC14 and PC15 pin/ball signals in pinout/ballout schematics. Replaced f_{ACLK} by $f_{rcc\_c\_ck}$ in *Section : Typical and maximum current consumption*. Replaced system clock by CPU clock and f_{ACLK} by $f_{rcc\_c\_ck}$ in *Section : On-chip peripheral current consumption*. Updated Note *2.* in *Table 26: Reset and power control block characteristics*. Updated *Table 27: Embedded reference voltage*, *Table 29: Typical and maximum current consumption in Run mode, code with data processing running from ITCM, regulator ON*, *Table 30: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, cache ON, regulator ON* and *Table 35: Typical and maximum current consumption in Stop mode, regulator ON*. Updated typical and maximum current consumption in *Table 36: Typical and maximum current consumption in Standby mode* and *Table 37: Typical and maximum current consumption in VBAT mode*. Added note to f_{LSI} in *Table 48: LSI oscillator characteristics*.