Renesas Electronics America Inc - IDT79RC64T575-200DP Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-I
Number of Cores/Bus Width	1 Core, 64-Bit
Speed	200MHz
Co-Processors/DSP	System Control; CP0
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 85°C (TC)
Security Features	-
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc64t575-200dp

ferring data between the processor and memory at a peak rate of 1000MB/sec. A boot-time selectable option to run the system interface as 32-bits wide—using basically the same protocols as the 64-bit system—is also supported.

A **boot-time mode control interface** initializes fundamental processor modes and is a serial interface that operates at a very low frequency (SysClock divided by 256). This low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively, the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL. The boot-time serial stream is shown in Table 3.

Serial Bit	Description	Value & Mode Setting
0	Reserved	Must be set to 0.
1:4	Transmit-data-pattern. Bit 4 is MSB	64-bit bus width: 0: DDDD 1: DDxDDx 2: DDxxDDxx 3: DxDxDxDx 4: DDxxxDDxxx 5: DDxxxxDDxxxx 6: DxxDxxDxxDxx 7: DDxxxxxxDDxxxxxx 8: DxxxDxxxDxxxDxxx 9-15: Reserved. Must not be selected. 32-bit bus width: 0: WWWWWWWW 1: WWxWWxWWxWWx 2: WWxxWWxxWWxxWWxx 3: WxWxWxWxWxWxWxWx 4: WWxxxWWxxxWWxxxWWxxx 5: WWxxxxWWxxxxWWxxxxWWxxxx 6: WxxWxxWxxWxxWxxWxxWxxWxx 7: WWxxxxxxWWxxxxxxWWxxxxxxWWxxxxxx 8: WxxxWxxxWxxxWxxxWxxxWxxxWxxxWxxx 9-15: Reserved. Must not be selected.
5:7	PClock-to-SysClk-Ratio. Bit 7 is MSB	0: 2 1: 3 2: 4 3: 5 4: 6 5: 7 6: 8 7: Reserved
8	Endianness	0: Little endian 1: Big endian
9:10	Non-block write Mode. Bit 10 is MSB	00: R4400 compatible 01: Reserved 10: Pipelined-Write-Mode 11: Write-Reissue-Mode

Table 3 Boot-time Mode Stream (Page 1 of 2)

Serial Bit	Description	Value & Mode Setting
11	TimerIntEn	Timer interrupt settings: 0: Enable Timer Interrupt on Int(5) 1: Disable Timer Interrupt on Int(5)
12	System Interface Bus Width.	Interface bus width control settings: 0: 64-bit system interface 1: 32-bit system interface
13:14	Drv_Out Bit 14 is MSB	Slew rate control of the output drivers: 10: 100% strength (fastest) 11: 83% strength 00: 67% strength 01: 50% strength (slowest)
15:17	Write address to write data delay.	From 0 to 7 SysClk cycles: 0: AD... 1: AxD... 2: AxxD... 3: AxxxD... 4: AxxxxD... 5: AxxxxxD... 6: AxxxxxxD... 7: AxxxxxxxD...
18	Reserved	User must select '0'
19	Extend Multiplication Repeat Rate.	Initial setting of the "Fast Multiply" bit. 0: Enable Fast Multiply 1: Do not Enable Fast Multiply **Note:** For pipeline speeds >250MHz, this bit must be set to '1'.
20:24	Reserved	User must select '0'
25:26	System configuration identifier.	Software visible in processorConfig[21:20] 0: Config[21:20] = Mode Bit [25:26] Must be set to 0.
27:256	Reserved	User must select '0'

Table 3 Boot-time Mode Stream (Page 2 of 2)

The **clocking interface** allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock and can be between 33 and 125MHz. An on-chip **phase-locked-loop (PLL)** generates the pipeline clock (PClock) through multiplication of the system interface clock by values of 2,3,4,5,6,7 or 8, as defined at system reset. This allows the pipeline clock to be implemented at a significantly higher frequency than the system interface clock. The RC64574/575 support both single data (one byte through full CPU bus width) and 8-word block transfers on the SysAD bus.

The RC64574/575 implement additional **write protocols** that **double the effective write bandwidth**. The write re-issue has a repeat rate of 2 cycles per write. Pipelined writes have the same 2-cycle per write repeat rate, but can issue an additional write after WrRdy* de-asserts.

Choosing a 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles as well as whether a single data transfer—larger than 4 bytes—must be divided into two smaller transfers.

As shown in Table 3, the bus delay can be defined as 0 to 7 SysClock cycles and is activated and controlled through mode bit (17:15) settings selected during the reset initialization sequence. The '000' setting provides the same write operations timing protocol as the RC4640, RC4650, and RC5000 processors.

To facilitate discrete **interface to SyncDRAM**, the RC64574/575 bus interface is enhanced during write cycles with a programmable delay that is inserted between the write address and the write data (for both block and non-block writes).

Board-level testing during Run-Time mode is facilitated through the full JTAG boundary scan facility. Five pins—TDI, TDO, TMS, TCK, TRST*—have been incorporated to support the standard JTAG interface.

The RC64574/575 devices offer a direct migration path for designs that are based on IDT's RC4640/RC4650 and RC64474/RC64475 processors[2], through full pin and socket compatibility. Full 64-bit-family software and bus protocol compatibility ensures the RC64574/575 processors access to an existing market and development infrastructure, allowing quicker time to market.

Development Tools

An array of hardware and software tools is available to assist system designers in the rapid development of RC64574/575 based systems. This accessibility allows a wide variety of customers to take full advantage of the device's high-performance features while addressing today's aggressive time-to-market demands.

Cache Memory

To keep the high-performance pipeline of the RC64574/575 full and operating efficiently, on-chip instruction and data caches have been incorporated. Each cache has its own data path and can be accessed in the same single pipeline clock cycle.

The 32kB two-way set associative **instruction cache** is virtually indexed, physically tagged, and word parity protected. Because this cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing both operations to occur simultaneously. The instruction cache provides a peak instruction bandwidth of 2GB/sec at 250MHz.

The 32kB two-way set associative **data cache** is byte parity protected and has a fixed 32-byte (eight words) line size. Its tag is protected with a single parity bit. To allow simultaneous address translation and data cache access, the D-cache is virtually indexed and physically tagged. The data cache can provide 8 bytes each clock cycle, for a peak bandwidth of 2GB/s.

[2] To ensure socket compatibility, refer to Table 8 and Table 9.

To lock critical sections of code and/or data into the caches for quick access, a per line **"cache locking"** feature has been implemented. Once enabled, a cache is said to be locked when a particular piece of code or data is loaded into the cache and that cache location will not be selected later for refill by other data.

Power Management

Executing the WAIT instruction enables the processor to enter Standby mode. The internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) will continue to run. Once in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Thermal Considerations

The RC64574 is packaged in a 128-pin QFP footprint package and uses a 32-bit external bus, offering the ideal combination of 64-bit processing power and 32-bit low-cost memory systems. The RC64575 is packaged in a 208-pin QFP footprint package and uses the full 64-bit external bus. The RC64575 is ideal for applications requiring 64-bit performance and 64-bit external bandwidth.

Both devices are guaranteed in a case temperature range of 0° to +85° C for commercial temperature devices and -40° to +85° C for Industrial temperature devices. Package type, speed (power) of the device, and air flow conditions affect the equivalent ambient temperature conditions that will meet these specifications.

Using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package, the equivalent allowable ambient temperature, T_A, can be calculated. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device. Typical values for $\varnothing_{CA}$ at various air flow are shown in Table 4. Note that the RC64574/575 processor implements advanced power management, which substantially reduces the typical power dissipation of the device.

	∅CA					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
128 QFP	16	10	9	7	6	5
208 QFP	20	13	10	9	8	7

Table 4 Thermal Resistance (∅CA) at Various Airflows

Revision History

July 22, 1999: Original data sheet.

Pin Description Table

The following is a list of system interface pins available on the RC64574/575. Pin names ending with an asterisk (*) are active when low.

Pin Name	Type	Description
System Interface		
ExtRqst*	I	**External request** An external agent asserts ExtRqst* to request use of the System interface. The processor grants the request by asserting Release*.
Release*	O	**Release interface** In response to the assertion of ExtRqst* or a CPU read request, the processor asserts Release* and signals to the requesting device that the system interface is available.
RdRdy*	I	**Read Ready** The external agent asserts RdRdy* to indicate that it can accept a processor read request.
WrRdy*	I	**Write Ready** An external agent asserts WrRdy* when it can now accept a processor write request.
ValidIn*	I	**Valid Input** Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	O	**Valid Output** Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	I/O	**System address/data bus** A 64-bit address and data bus for communication between the processor and an external agent. In 64 bit interface mode, during address phases only, SysAd(35:0) contains invalid address information. The remaining SysAD(63:36) pins are not used. The whole 64-bit SysAD(63:0) may be used during the data transfer phase. For all double-word accesses (read or write), the low-order 3 bits (SysAD[2:0]) will always be output as zero during the address phase. In 32-bit interface mode and in the RC64574, SysAD(63:32) is not used, regardless of Endianness. A 32-bit address and data communication between processor and external agent is performed via SysAD(31:0).
SysADC(7:0)	I/O	**System address/data check bus** An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles. In 32-bit mode and in the RC64574, SysADC(7:4) is not used. The SysADC(3:0) contains check bits for SysAD(31:0).
SysCmd(8:0)	I/O	**System command/data identifier bus** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	I/O	**System Command Parity** A single, even-parity bit for the Syscmd bus. This signal is always driven low.
Clock/Control Interface		
SysClock	I	**SystemClock** The system clock input establishes the processor and bus operating frequency. It is multiplied internally by 2,3,4,5,6,7, or 8 to generate the pipeline clock (PClock).
$V_{CC}P$	I	**Quiet VCC for PLL** Quiet V_{CC} for the internal phase locked loop.
$V_{SS}P$	I	**Quiet V_{SS} for PLL** Quiet V_{SS} for the internal phase locked loop.

Table 5 Pin Descriptions (Page 1 of 2)

Logic Diagram — RC64574/RC64575

Figure 1 illustrates the direction and functional groupings for the processor signals.

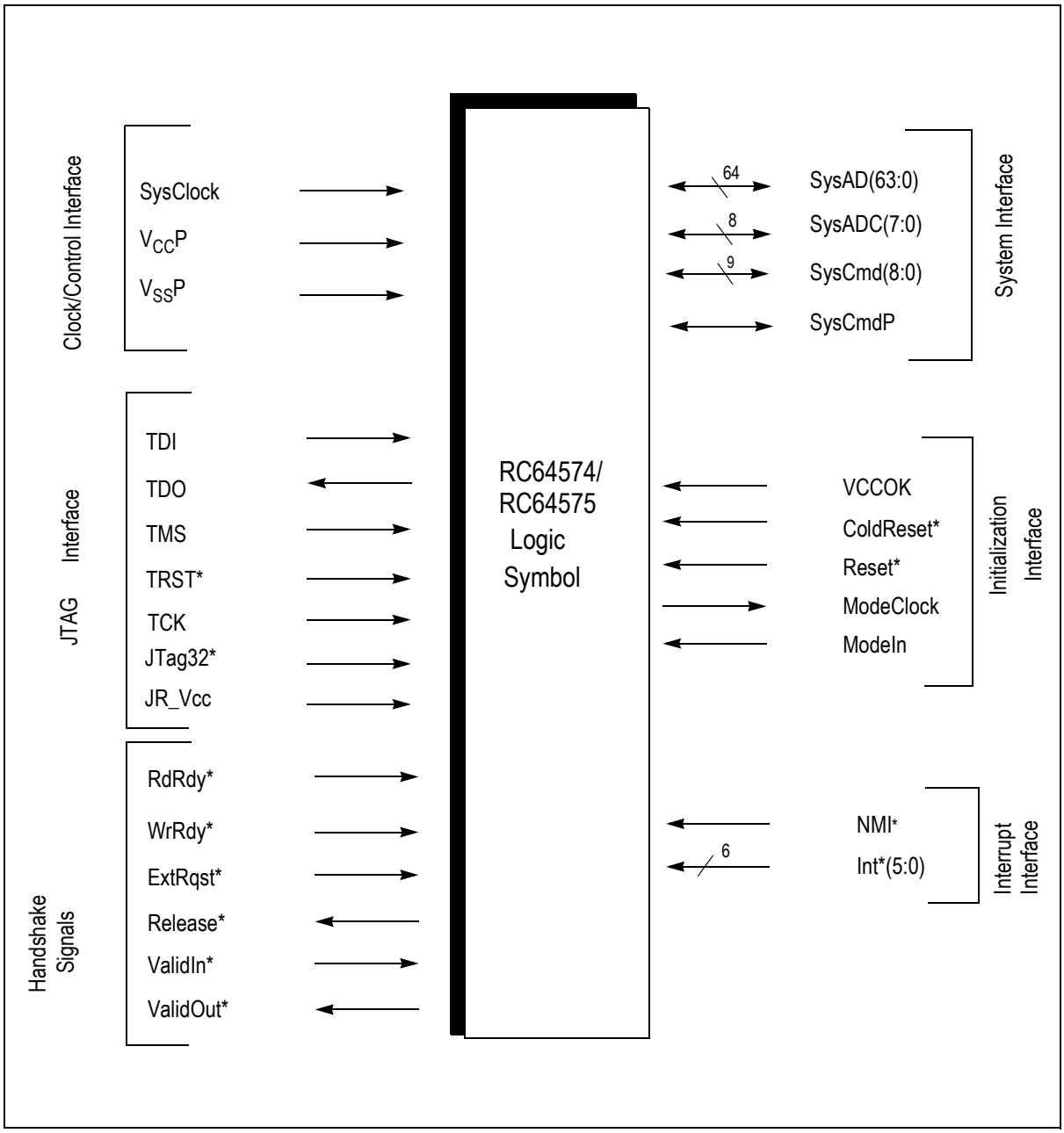


Figure 1 Logic Symbol for RC64574/RC64575

RC64575 208-pin QFP Package Pin-out

Pin names followed by an asterisk (*) are active when low. For maximum flexibility and compatibility with future designs, N.C. pins should be left floating.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	JTAG32*	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	N.C.	55	N.C.	107	N.C.	159	SysAD59
4	N.C.	56	N.C.	108	N.C.	160	ColdReset*
5	N.C.	57	SysCmd2	109	N.C.	161	SysAD28
6	N.C.	58	SysAD36	110	N.C.	162	V_{cc}
7	N.C.	59	SysAD4	111	N.C.	163	V_{ss}
8	N.C.	60	SysCmd1	112	N.C.	164	SysAD60
9	N.C.	61	V_{ss}	113	N.C.	165	Reset*
10	SysAD11	62	V_{cc}	114	SysAD52	166	SysAD29
11	V_{ss}	63	SysAD35	115	ExtRqst*	167	SysAD61
12	V_{cc}	64	SysAD3	116	V_{cc}	168	SysAD30
13	SysCmd8	65	SysCmd0	117	V_{ss}	169	V_{cc}
14	SysAD42	66	SysAD34	118	SysAD21	170	V_{ss}
15	SysAD10	67	V_{ss}	119	SysAD53	171	SysAD62
16	SysCmd7	68	V_{cc}	120	RdRdy*	172	SysAD31
17	V_{ss}	69	SysAD2	121	Modein	173	SysAD63
18	V_{cc}	70	Int5*	122	SysAD22	174	V_{cc}
19	SysAD41	71	SysAD33	123	SysAD54	175	V_{ss}
20	SysAD9	72	SysAD1	124	V_{cc}	176	V_{cc}OK
21	SysCmd6	73	V_{ss}	125	V_{ss}	177	SysADC3
22	SysAD40	74	V_{cc}	126	Release*	178	SysADC7
23	V_{ss}	75	Int4*	127	SysAD23	179	N.C.
24	V_{cc}	76	SysAD32	128	SysAD55	180	TDI
25	SysAD8	77	SysAD0	129	NMI*	181	TRst*
26	SysCmd5	78	Int3*	130	V_{cc}	182	TCK
27	SysADC4	79	V_{ss}	131	V_{ss}	183	TMS
28	SysADC0	80	V_{cc}	132	SysADC2	184	TDO
29	V_{ss}	81	Int2*	133	SysADC6	185	V_{cc}P
30	V_{cc}	82	SysAD16	134	SysAD24	186	V_{ss}P
31	SysCmd4	83	SysAD48	135	V_{cc}	187	SysClock
32	SysAD39	84	Int1*	136	V_{ss}	188	V_{cc}
33	SysAD7	85	V_{ss}	137	SysAD56	189	V_{ss}

Table 6 RC64575 208-pin QFP Package Pin-Out (Page 1 of 2)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
34	SysCmd3	86	V_{cc}	138	SysAD25	190	SysADC5
35	V_{ss}	87	SysAD17	139	SysAD57	191	SysADC1
36	V_{cc}	88	SysAD49	140	V_{cc}	192	V_{cc}
37	SysAD38	89	Int0*	141	V_{ss}	193	V_{ss}
38	SysAD6	90	SysAD18	142	N.C	194	SysAD47
39	ModeClock	91	V_{ss}	143	SysAD26	195	SysAD15
40	WrRdy*	92	V_{cc}	144	SysAD58	196	SysAD46
41	SysAD37	93	SysAD50	145	N.C.	197	V_{cc}
42	SysAD5	94	ValidIn*	146	V_{cc}	198	V_{ss}
43	V_{ss}	95	SysAD19	147	V_{ss}	199	SysAD14
44	V_{cc}	96	SysAD51	148	SysAD27	200	SysAD45
45	N.C.	97	V_{ss}	149	N.C.	201	SysAD13
46	N.C.	98	V_{cc}	150	JR_V_{cc}	202	SysAD44
47	N.C.	99	ValidOut*	151	N.C.	203	V_{ss}
48	N.C.	100	SysAD20	152	N.C.	204	V_{cc}
49	N.C.	101	N.C.	153	N.C.	205	SysAD12
50	N.C.	102	N.C.	154	N.C.	206	SysCmdP
51	N.C.	103	N.C.	155	N.C.	207	SysAD43
52	N.C.	104	N.C.	156	N.C.	208	N.C.

Table 6 RC64575 208-pin QFP Package Pin-Out (Page 2 of 2)

Absolute Maximum Ratings

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Rating	Commercial (2.5V±5%)	Industrial (2.5V±5%)	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5[1] to +4.0	–0.5[1] to +4.0	V
T_C	Operating Temperature (case)	0 to +85	-40 to +85	°C
T_{BIAS}[2]	Case Temperature Under Bias	–55 to +125	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	–55 to +125	°C
I_{IN}	DC Input Current	20[3]	20[3]	mA
I_{OUT}	DC Output Current	50[4]	50[4]	mA

1. V_{In} minimum = –2.0V for pulse width less than 15ns. For 3.3V tolerant input, V_{In} maximum is 3.8V.

2. Case temperature when device is powered up but not operating.

3. When V_{IN} < 0V or V_{IN} > V_{CC}.

4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Recommended Operation Temperature and Supply Voltage

Grade	Temperature	GND	RC64574/575
			Vcc
Commercial	0°C to +85°C (Case)	0V	2.5V±5%
Industrial	-40°C to + 85°C (Case)	0V	2.5V±5%

DC Electrical Characteristics

Commercial Temperature Range—RC64574/575

(T_{case} = 0°C to +85°C Commercial, T_{case} = -40°C to +85°C Industrial, V_{cc} = 2.5V± 5%)

Parameter	RC64574/RC64575 200MHz		RC64574/RC64575 250MHz		Conditions
	Min	Max	Min	Max	
V_{OL}	—	0.1V	—	0.1V	|IOUT|= 20uA
V_{OH}	V_{cc} - 0.1V	—	V_{cc} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	|IOUT|= 4mA
V_{OH}	2.0V	—	2.0V	—	
V_{IL}	–0.5V	0.2V_{cc}	–0.5V	0.2V_{cc}	—
V_{IH}	0.7 V_{cc}	3.8V	0.7 V_{cc}	3.8V	—
I_{IN}	—	±10uA	—	±10uA	0 ≤ VIN ≤ VCC
C_{IN}	—	10pF	—	10pF	—

Parameter	RC64574/RC64575 200MHz		RC64574/RC64575 250MHz		Conditions
	Min	Max	Min	Max	
C_{IO}	—	10pF	—	10pF	—
C_{clk}	—	10pF	—	10pF	
I/O_{LEAK}	—	20uA	—	20uA	Input/Output Leakage

Power Consumption—RC64574

Note: The following table assumes as 4:1 pipeline to bus clock ratio.

Parameter		RC64574 200MHz		RC64574 250MHz		Conditions
		Typical[1]	Max	Typical[1]	Max	
I_{CC}	stand-by	—	60 mA[2]	—	60 mA[2]	C_L = 0pF[3]
		—	120 mA[2]	—	120 mA[2]	C_L = 50pF
	active	470 mA[2]	550 mA[2]	550 mA[2]	680 mA[2]	C_L = 0pF No SysAd activity[3] Vcc = 2.63V
		550mA[2]	650 mA[2]	650 mA[2]	800 mA[2]	C_L = 50pF R4x00 compatible writes, T_C = 25°C Vcc = 2.63V
		600 mA[2]	715 mA[4]	715 mA[2]	880 mA[4]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[3] Vcc = 2.63V

1. Typical integer instruction mix and cache miss rates.

2. These are not tested. They are the results of engineering analysis and are provided for reference only.

3. Guaranteed by design.

4. These are the specifications IDT tests to insure compliance.

RC64574 Power Curves

The following two graphs contain power curves that show power consumption at various bus frequencies. Power consumption is based on the values for R4x00 compatible write mode, shown in the table above.

Note: Only pipeline frequencies that are integer multiples (2x, 3x, etc.) of bus frequencies are supported.

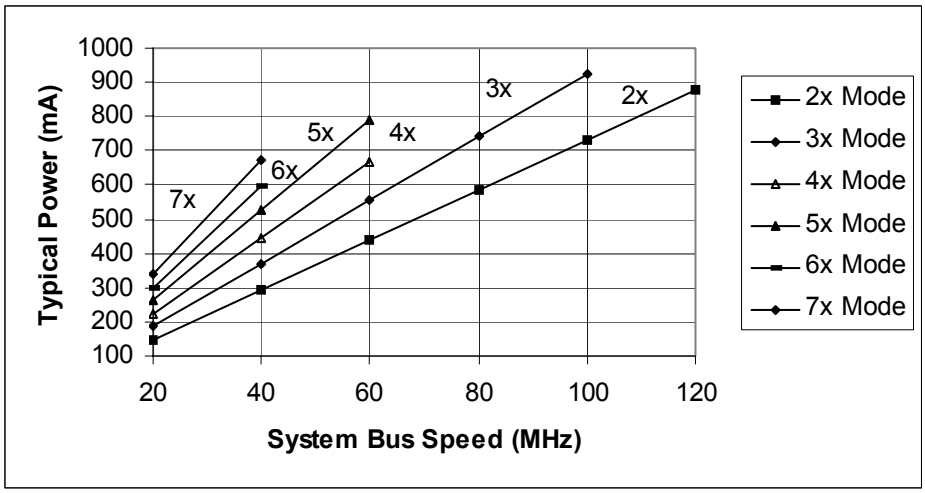


Figure 2 Typical Power Usage - RC64574

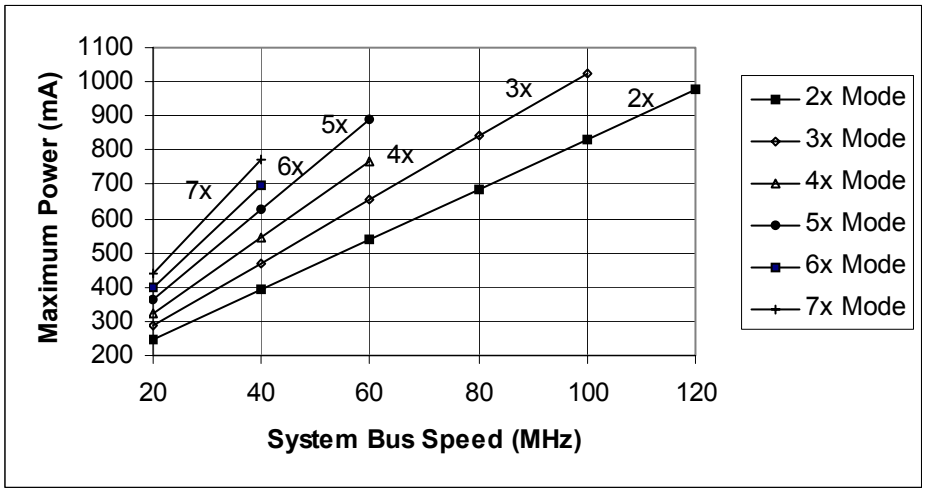


Figure 3 Maximum Power Usage - RC64574

Power Consumption—RC64575

Note: The following table assumes a 4:1 pipeline to bus clock ratio.

Parameter		RC64575 200MHz		RC64575 250MHz		Conditions
		Typical[1]	Max	Typical[1]	Max	
I_{CC}	stand-by	—	60 mA[2]	—	60 mA[2]	C_L = 0pF[3]
		—	120 m[2]A	—	120 m[2]A	C_L = 50pF
	active, 64-bit bus option[4]	510 mA[2]	680 mA[2]	600 mA[2]	810 mA[2]	C_L = 0pF No SysAd activity[3] Vcc = 2.63V
		600 mA[2]	800 mA[2]	700 mA[2]	950 mA[2]	C_L = 50pF R4x00 compatible writes, T_C = 25°C Vcc = 2.63V
		660 mA[2]	880 mA[5]	770 mA[2]	1050 mA[5]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[3] Vcc = 2.63V

1. Typical integer instruction mix and cache miss rates.

2. These are not tested. They are the results of engineering analysis and are provided for reference only.

3. Guaranteed by design.

4. In 32-bit bus option, use RC64574 power consumption values.

5. These are the specifications IDT tests to insure compliance.

RC64575 Power Curves

The following two graphs contain power curves that show power consumption at various bus frequencies. Power consumption is based on the values for R4x00 compatible write mode, shown in the table above.

Note: Only pipeline frequencies that are integer multiples (2x, 3x, etc.) of bus frequencies are supported.

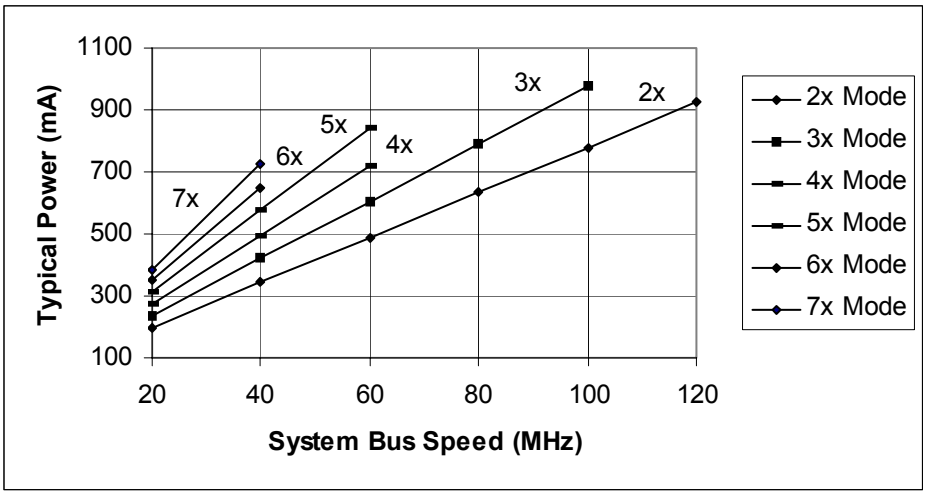


Figure 4 Typical Power Usage - RC64575

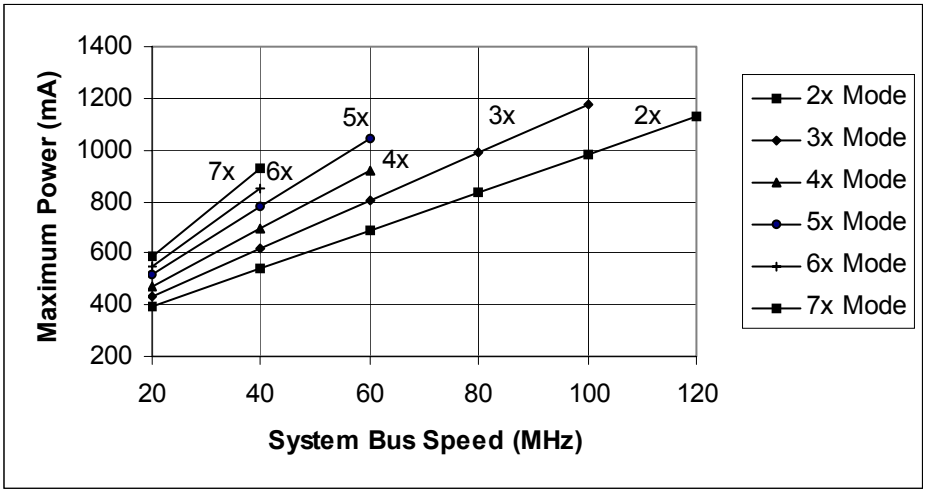


Figure 5 Maximum Power Usage - RC64575

Timing Characteristics—RC64574/RC64575

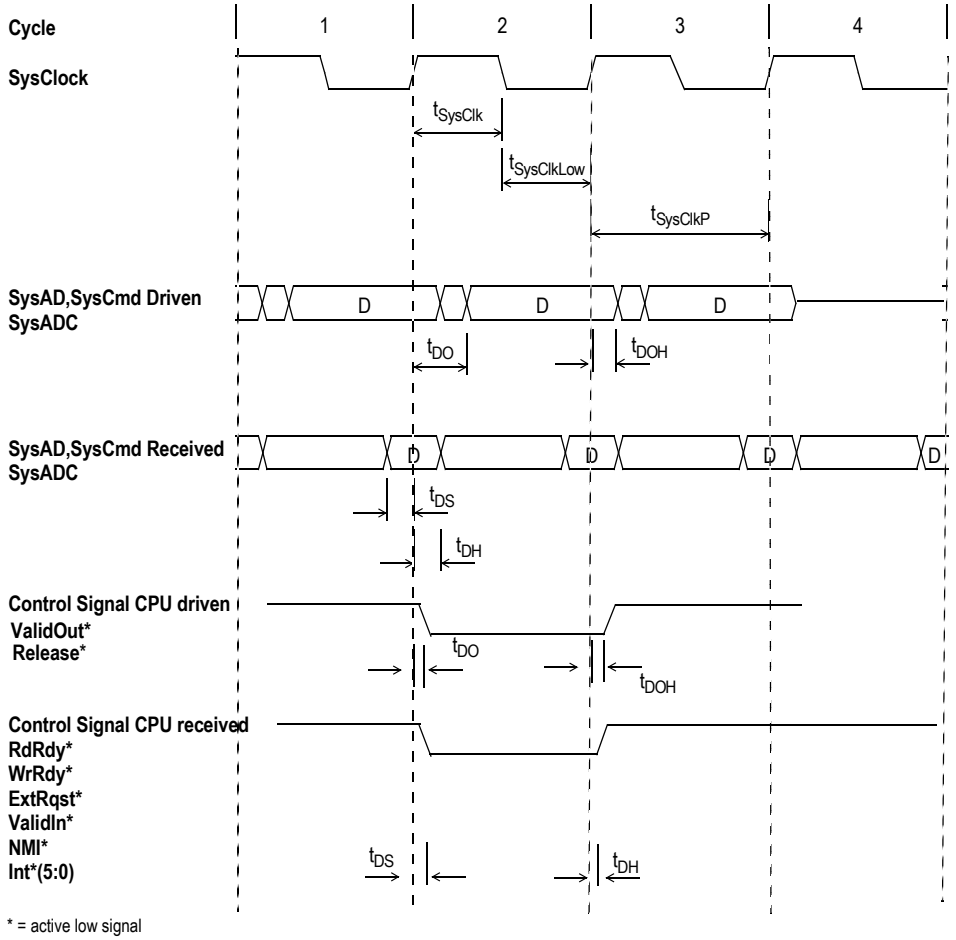


Figure 6 System Clocks Data Setup, Output, and Hold Timing

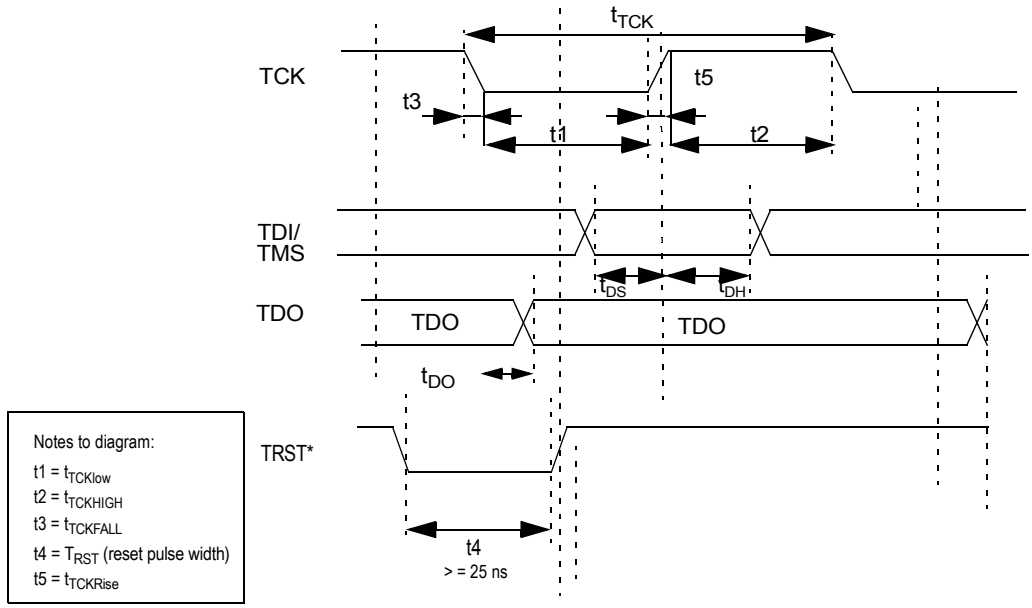


Figure 7 Standard JTAG Timing

System Interface Parameters

Parameter	Symbol	Test Conditions	RC64574/ RC64575 200MHz		RC64574/ RC64575 250MHz		Units
			Min	Max	Min	Max	
Data Output	t_{DO} = Max	$mode_{14..13}$ = 10 (Fastest)	—	5	—	4.3	ns
		$mode_{14..13}$ = 11 (85%)	—	6	—	4.5	ns
		$mode_{14..13}$ = 00 (66%)	—	7	—	5	ns
		$mode_{14..13}$ = 01 (Slowest)	—	8	—	5	ns
Data Output Hold	t_{DOH}[1]	$mode_{14..13}$ = 10	0	—	0	—	ns
		$mode_{14..13}$ = 11	0	—	0	—	ns
		$mode_{14..13}$ = 00	0	—	0	—	ns
		$mode_{14..13}$ = 01	0	—	0	—	ns
Data Input	t_{DS}	t_{rise} = 3ns t_{fall} = 3ns	2	—	2	—	ns
	t_{DH}		1.0	—	1.0	—	ns

1. 50 pf loading on external output signals

Boot-time Interface Parameters

Parameter	Symbol	Test Conditions	RC64574/ RC64575 200MHz		RC64574/ RC64575 250MHz		Conditions
			Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	4	—	4	—	SysClock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	SysClock Cycle

Mode Configuration Interface Reset Sequence

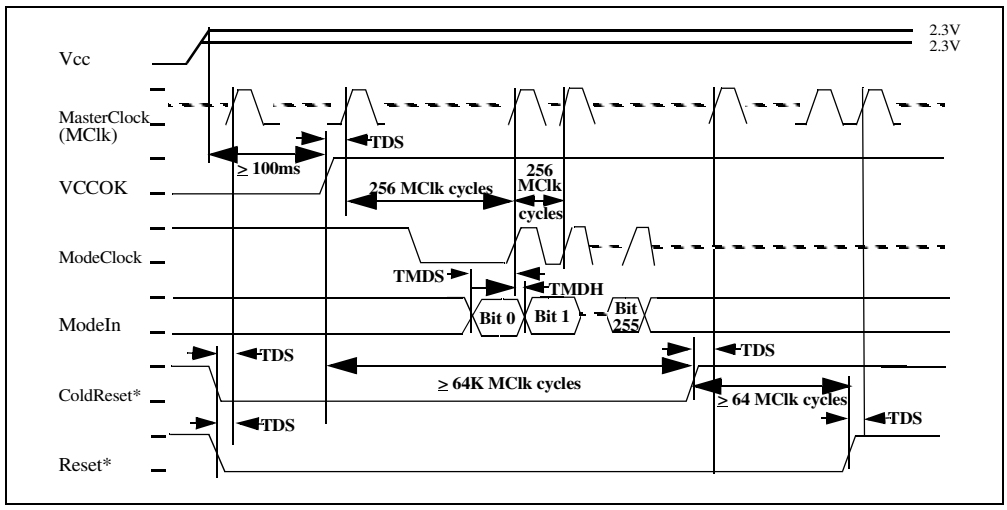


Figure 8 Power-on Reset

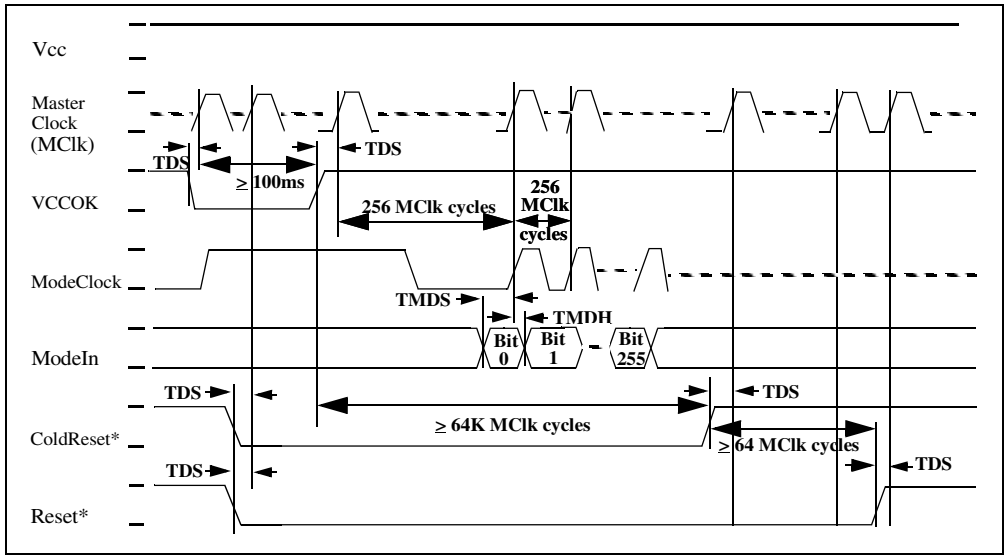


Figure 9 Cold Reset

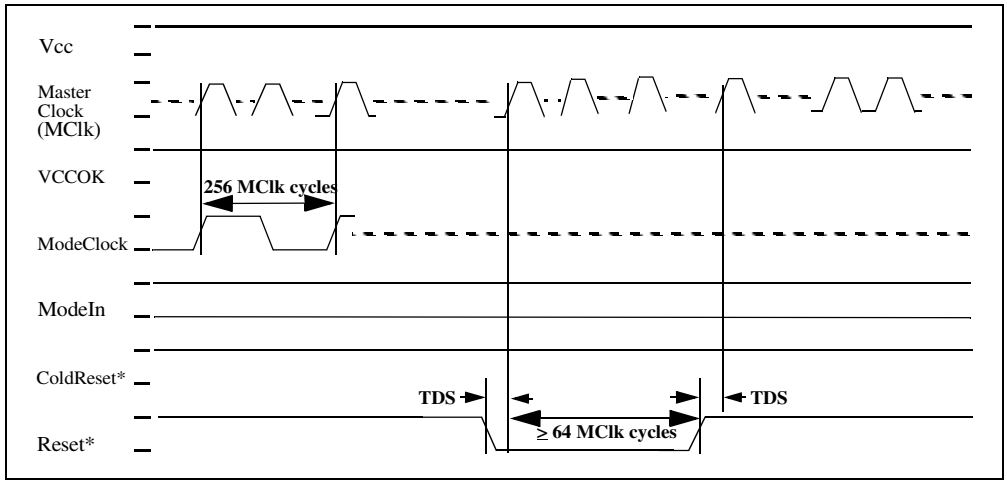
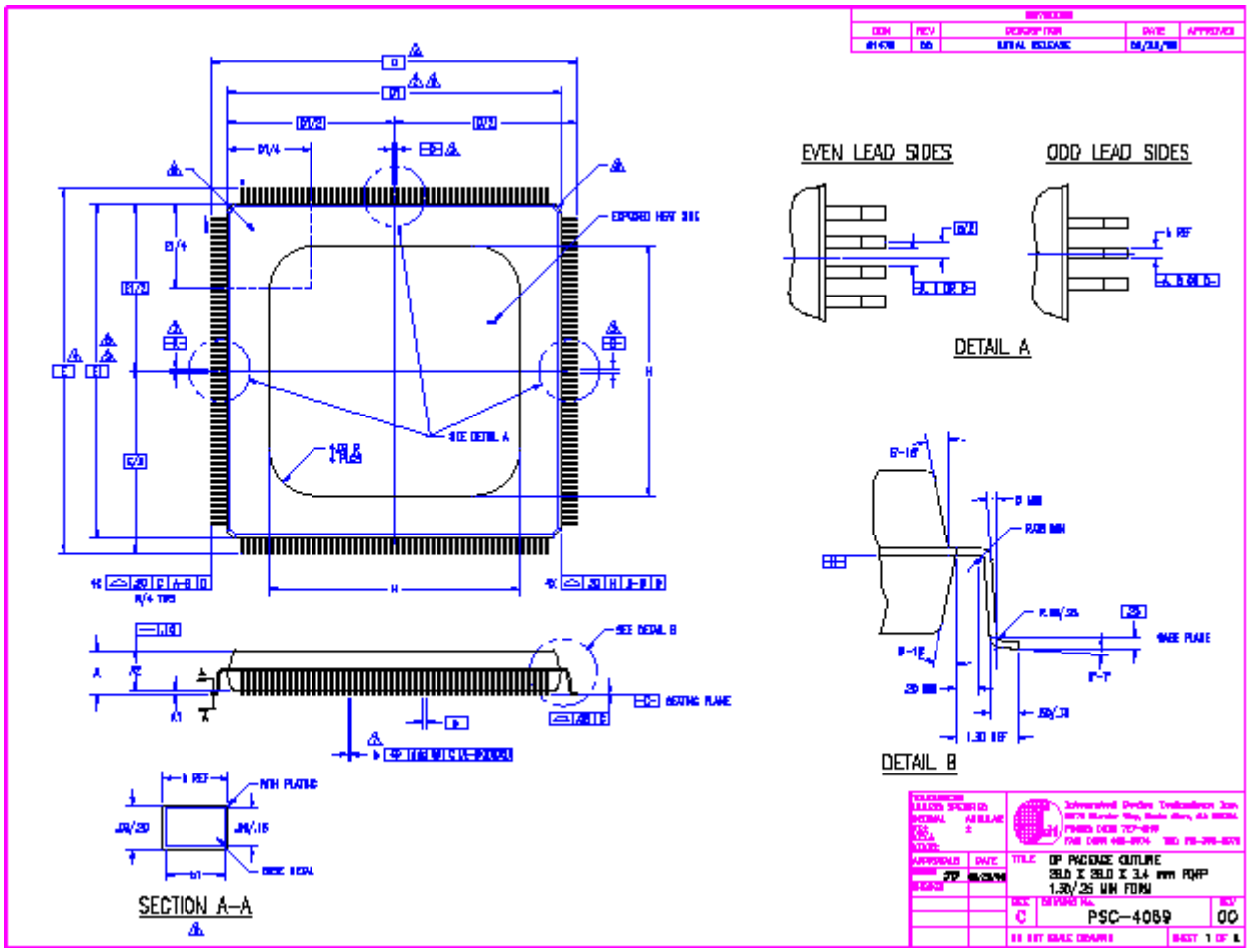


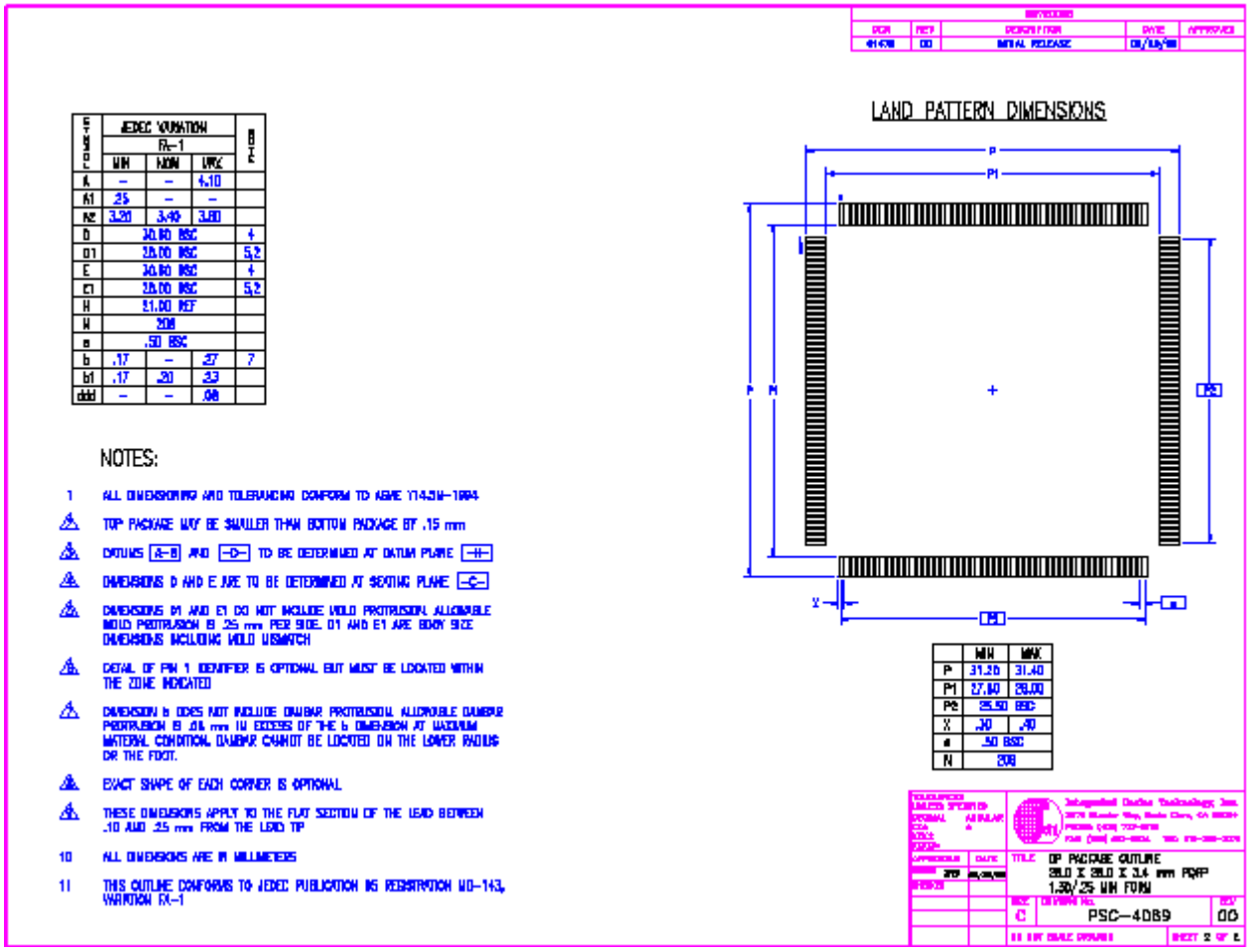
Figure 10 Warm Reset

RC64575 208-pin Package Diagram

The RC64575 is available in a 208-pin QFP package.



RC64575 208-pin Package Diagram (page2)



SYMBOL	JEDEC VARIATION FA-1 MIN	NOM	MAX	NOTE
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D		30.60 BSC		4
D1		28.00 BSC		5,2
E		30.60 BSC		4
E1		28.00 BSC		5,2
H		31.00 REF		
M		208		
e		.50 BSC		
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm.
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP.
10. ALL DIMENSIONS ARE IN MILLIMETERS.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1.

LAND PATTERN DIMENSIONS

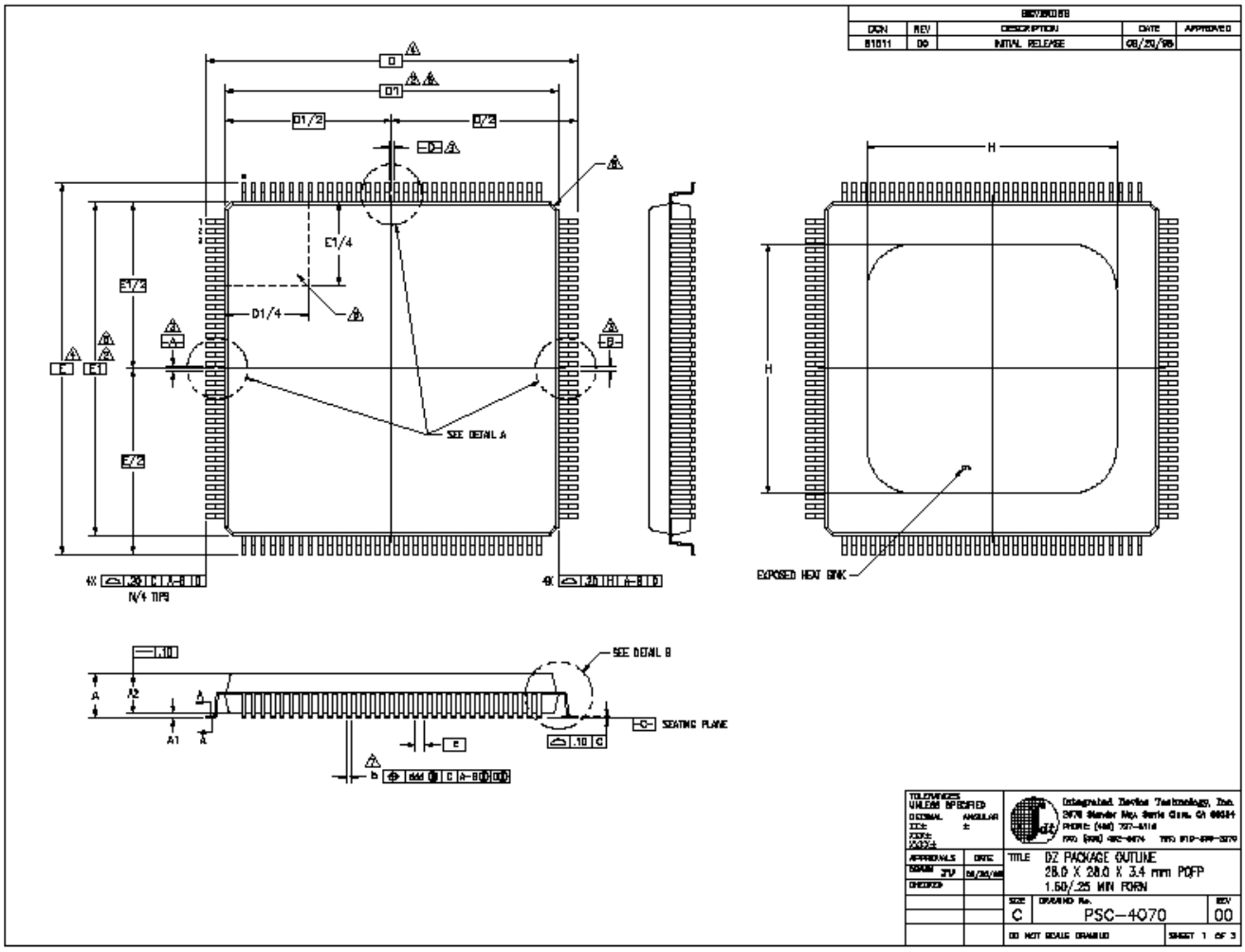
	MIN	MAX
P	31.20	31.40
P1	27.90	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

TITLE: QP PACKAGE OUTLINE
28.0 X 28.0 X 3.4 mm PQFP
1.30/.25 MM FORM

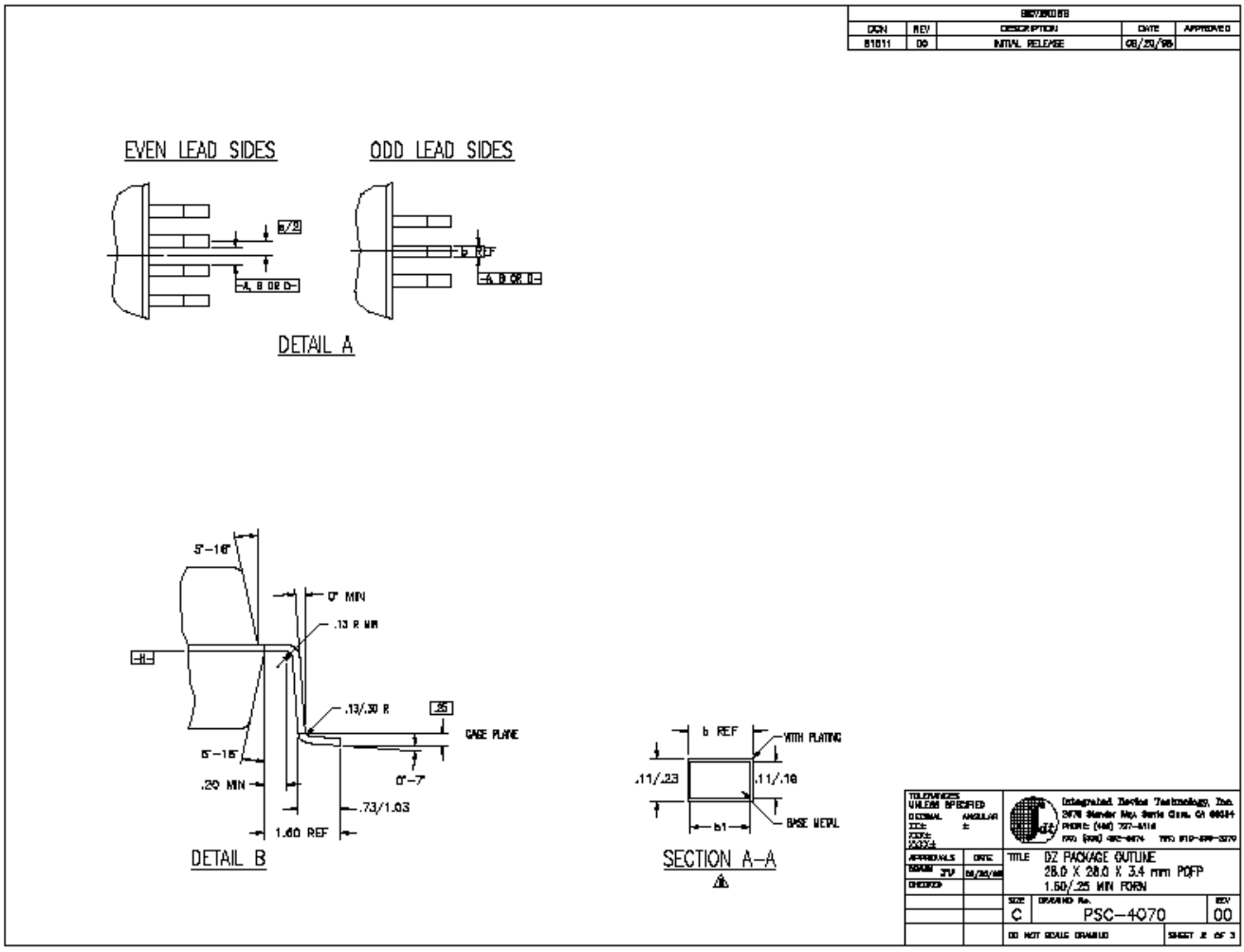
SIZE: C | DRAWING NO.: PSC-4089 | REV: 00

RC64574 128-pin Package Diagram (page 1 of 3)

The RC64574 is available in a 128-pin QFP package.



RC64574 128-pin Package Diagram (page 2 of 3)

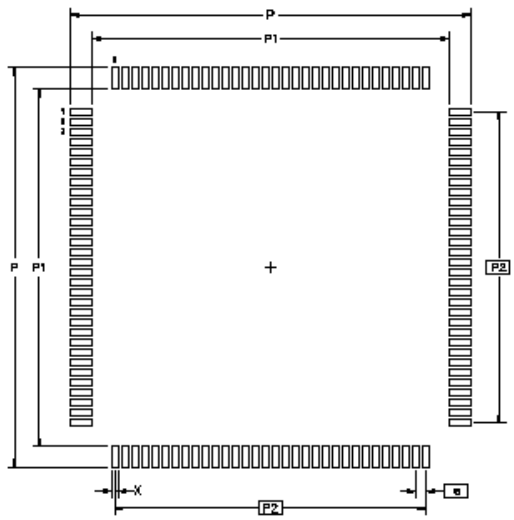


RC64574 128-pin Package Diagram (page 3 of 3)

DCN	REV	DESCRIPTION	DATE	APPROVED
61611	00	INITIAL RELEASE	08/20/98	

SYMBOL	JEDEC VARIATION DB-1 MIN	DB-1 NOM	DB-1 MAX	NOTE
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.80	
D		31.20 BSC		4
D1		28.00 BSC		5,2
E		31.20 BSC		4
E1		28.00 BSC		5,2
H		21.00 REF		
N		128		
e		.80 BSC		
b	.29	–	.45	7
b1	.29	.35	.41	
ddd	–	–	.20	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.80	32.00
P1	28.40	28.60
P2	24.80 BSC	
X	.40	.60
e	.80 BSC	
N	128	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A–B] AND [–D–] TO BE DETERMINED AT DATUM PLANE [–H–]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [–C–]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–022, VARIATION DB–1

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR ± XXX: XX.XX: XX.XXX:

Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070

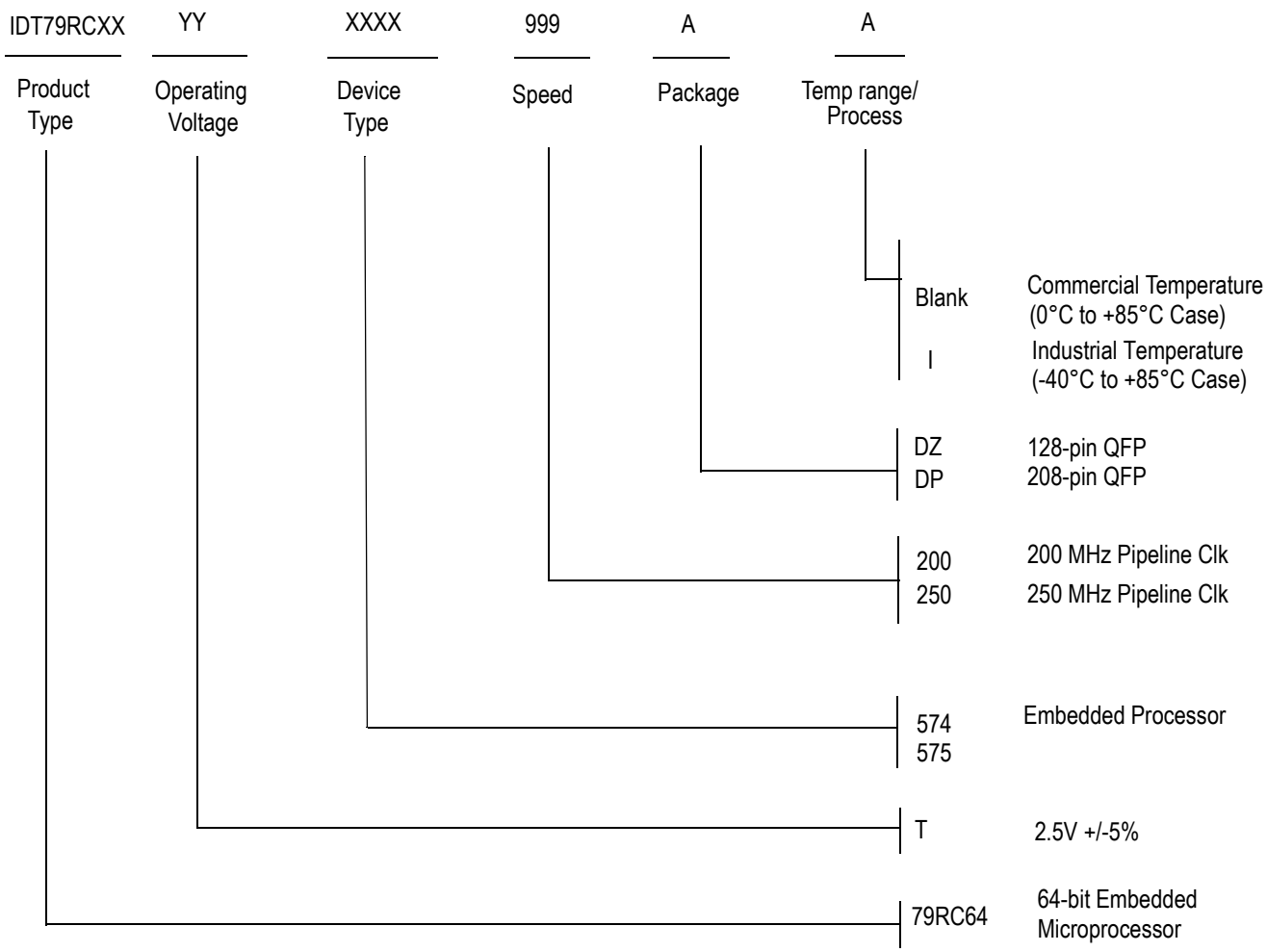
APPROVALS	DATE
ISSUE JV	08/20/98
CHECKED	

TITLE: DZ PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.60/.25 MIN FORM

SIZE	DRAWING No.	REV
C	PSC–4070	00

DO NOT SCALE DRAWING — SHEET 3 OF 3

Ordering Information



Valid Combinations

IDT79RC64T574 - 200, 250, DZ	128-pin QFP package, Commercial Temperature
IDT79RC64T575 - 200, 250, DP	208-pin QFP package, Commercial Temperature
IDT79RC64T574 - 200, 250, DZI	128-pin QFP package, Industrial Temperature
IDT79RC64T575 - 200, 250, DPI	08-pin QFP package, Industrial Temperature

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