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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2A
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	A/D 8x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df72115d160fpv

(6) Delayed Branch Instructions

With the exception of some instructions, unconditional branch instructions, etc., are executed as delayed branch instructions. With a delayed branch instruction, the branch is taken after execution of the instruction immediately following the delayed branch instruction. This reduces disturbance of the pipeline control when a branch is taken.

In a delayed branch, the actual branch operation occurs after execution of the slot instruction. However, instruction execution such as register updating excluding the actual branch operation, is performed in the order of delayed branch instruction → delay slot instruction. For example, even though the contents of the register holding the branch destination address are changed in the delay slot, the branch destination address remains as the register contents prior to the change.

Table 2.3 Delayed Branch Instructions

SH-2A CPU		Description	Example of Other CPU	
BRA	TRGET	Executes the ADD before branching to TRGET.	ADD.W	R1,R0
ADD	R1,R0		BRA	TRGET

(7) Unconditional Branch Instructions with No Delay Slot

The SH-2A additionally features unconditional branch instructions in which a delay slot instruction is not executed. This eliminates unnecessary NOP instructions, and so reduces the code size.

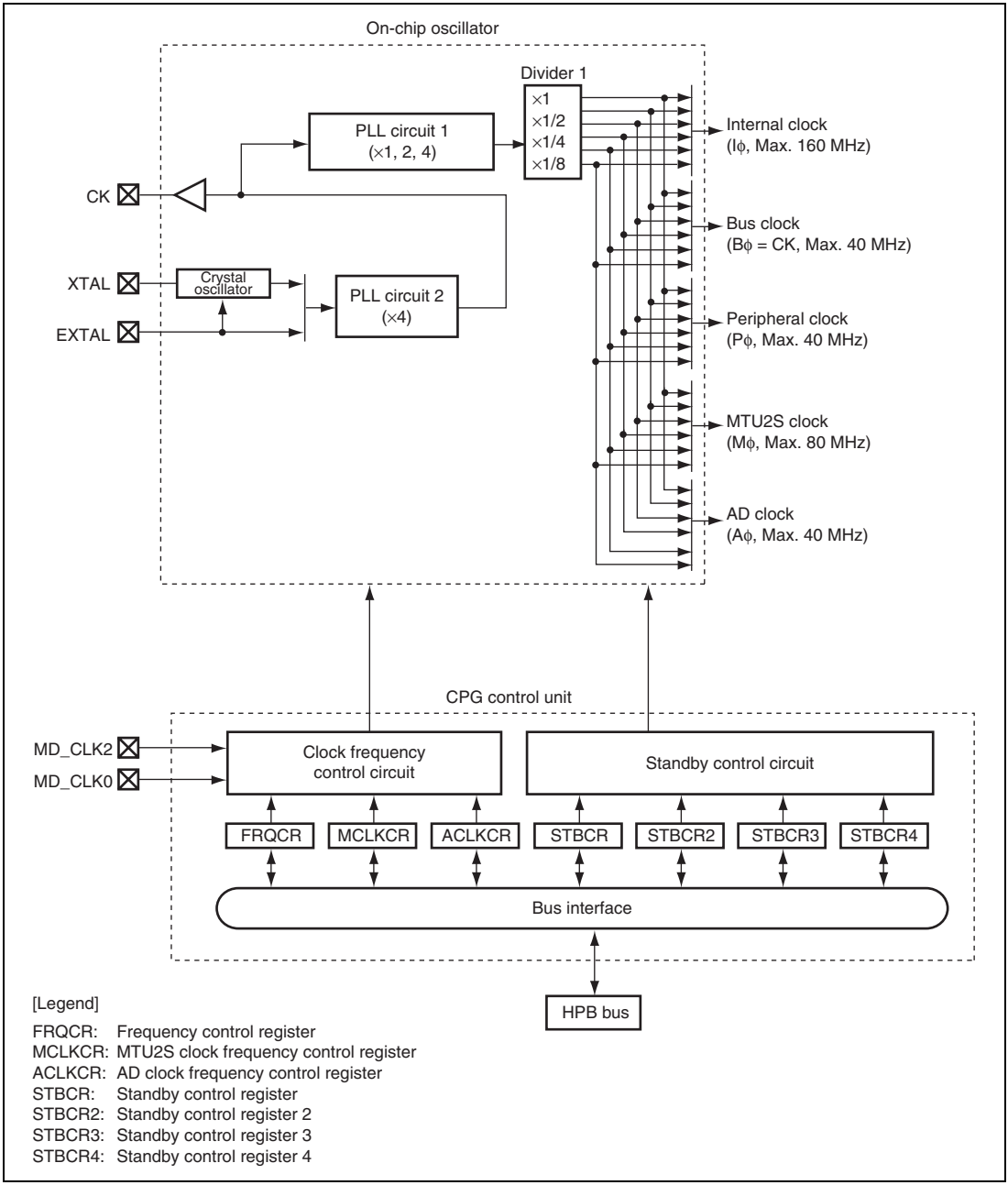
(8) Multiply/Multiply-and-Accumulate Operations

16-bit × 16-bit → 32-bit multiply operations are executed in one to two cycles. 16-bit × 16-bit + 64-bit → 64-bit multiply-and-accumulate operations are executed in two to three cycles. 32-bit × 32-bit → 64-bit multiply and 32-bit × 32-bit + 64-bit → 64-bit multiply-and-accumulate operations are executed in two to four cycles.

(9) T Bit

The T bit in the status register (SR) changes according to the result of the comparison. Whether a conditional branch is taken or not taken depends upon the T bit condition (true/false). The number of instructions that change the T bit is kept to a minimum to improve the processing speed.

Instruction		Instruction Code	Operation	Execution Cycles	T Bit	Compatibility		
						SH2, SH2E	SH4	SH-2A
MOVRT	Rn	0000nnnn00111001	~T → Rn	1	—			Yes
MOVT	Rn	0000nnnn00101001	T → Rn	1	—	Yes	Yes	Yes
MOVU.B	@(disp12,Rm),Rn	0011nnnnmmmm0001 1000ddddddddddd	(disp + Rm) → zero extension → Rn	1	—			Yes
MOVU.W	@(disp12,Rm),Rn	0011nnnnmmmm0001 1001ddddddddddd	(disp × 2 + Rm) → zero extension → Rn	1	—			Yes
NOTT		0000000001101000	~T → T	1	Operation result			Yes
PREF	@Rn	0000nnnn10000011	(Rn) → operand cache	1	—		Yes	Yes
SWAP.B	Rm,Rn	0110nnnnmmmm1000	Rm → swap lower 2 bytes → Rn	1	—	Yes	Yes	Yes
SWAP.W	Rm,Rn	0110nnnnmmmm1001	Rm → swap upper and lower words → Rn	1	—	Yes	Yes	Yes
XTRCT	Rm,Rn	0010nnnnmmmm1101	Middle 32 bits of Rm:Rn → Rn	1	—	Yes	Yes	Yes



[Legend]

FRQCR: Frequency control register
MCLKCR: MTU2S clock frequency control register
ACLKCR: AD clock frequency control register
STBCR: Standby control register
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4

Figure 4.1 Block Diagram of Clock Pulse Generator

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	BN[3:0]	0000	R	Bank Number These bits indicate the bank number to which saving is performed next. When an interrupt using register banks is accepted, saving is performed to the register bank indicated by these bits, and BN is incremented by 1. After BN is decremented by 1 due to execution of a RESBANK (restore from register bank) instruction, restoration from the register bank is performed.

- CS1WCR, CS7WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	BAS	-	WW[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	SW[1:0]		WR[3:0]				WM	-	-	-	-	HW[1:0]	
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BAS	0	R/W	SRAM with Byte Selection Byte Access Select Specifies the $\overline{WEn}$ and RD/$\overline{WR}$ signal timing when the SRAM interface with byte selection is used. 0: Asserts the $\overline{WEn}$ signal at the read/write timing and asserts the RD/$\overline{WR}$ signal during the write access cycle. 1: Asserts the $\overline{WEn}$ signal during the read/write access cycle and asserts the RD/$\overline{WR}$ signal at the write timing.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	WW[2:0]	000	R/W	Number of Write Access Wait Cycles Specify the number of cycles that are necessary for write access. 000: The same cycles as WR[3:0] setting (number of read access wait cycles) 001: No cycle 010: 1 cycle 011: 2 cycles 100: 3 cycles 101: 4 cycles 110: 5 cycles 111: 6 cycles

9.5 Usage Note

9.5.1 Half-End Flag Setting and Half-End Interrupt

When monitoring the half-end flag status in CHCR or using the half-end interrupt together with the reload function, the following precautions must be observed.

For the reload transfer count in RDMATCR, always set a value equal to the initial transfer count (the value in DMATCR).

If the first setting of DMATCR differs from the RDMATCR setting used in the second and following DMA transfer, the half-end flag setting timing may be earlier than half of the transfer count or the half-end flag may not be set. The same is true for the half-end interrupt.

Table 10.23 TIOR_2 (Channel 2)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_2 Function**	**TIOC2A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

Bit	Bit Name	Initial Value	R/W	Description
1	SCH3S	0	R/(W)*	Synchronous Start Controls synchronous start of TCNT_3S in the MTU2S. 0: Does not specify synchronous start for TCNT_3S in the MTU2S 1: Specifies synchronous start for TCNT_3S in the MTU2S [Clearing condition] • When 1 is set to the CST3 bit of TSTRS in MTU2S while SCH3S = 1
0	SCH4S	0	R/(W)*	Synchronous Start Controls synchronous start of TCNT_4S in the MTU2S. 0: Does not specify synchronous start for TCNT_4S in the MTU2S 1: Specifies synchronous start for TCNT_4S in the MTU2S [Clearing condition] • When 1 is set to the CST4 bit of TSTRS in MTU2S while SCH4S = 1

Note: Only 1 can be written to set the register.

(j) Complementary PWM Mode PWM Output Generation Method

In complementary PWM mode, 3-phase output is performed of PWM waveforms with a non-overlap time between the positive and negative phases. This non-overlap time is called the dead time.

A PWM waveform is generated by output of the output level selected in the timer output control register in the event of a compare-match between a counter and data register. While TCNTS is counting, data register and temporary register values are simultaneously compared to create consecutive PWM pulses from 0 to 100%. The relative timing of on and off compare-match occurrence may vary, but the compare-match that turns off each phase takes precedence to secure the dead time and ensure that the positive phase and negative phase on times do not overlap. Figures 10.46 to 10.48 show examples of waveform generation in complementary PWM mode.

The positive phase/negative phase off timing is generated by a compare-match with the solid-line counter, and the on timing by a compare-match with the dotted-line counter operating with a delay of the dead time behind the solid-line counter. In the T1 period, compare-match **a** that turns off the negative phase has the highest priority, and compare-matches occurring prior to **a** are ignored. In the T2 period, compare-match **c** that turns off the positive phase has the highest priority, and compare-matches occurring prior to **c** are ignored.

In normal cases, compare-matches occur in the order **a** → **b** → **c** → **d** (or **c** → **d** → **a'** → **b'**), as shown in figure 10.46.

If compare-matches deviate from the **a** → **b** → **c** → **d** order, since the time for which the negative phase is off is less than twice the dead time, the figure shows the positive phase is not being turned on. If compare-matches deviate from the **c** → **d** → **a'** → **b'** order, since the time for which the positive phase is off is less than twice the dead time, the figure shows the negative phase is not being turned on.

If compare-match **c** occurs first following compare-match **a**, as shown in figure 10.47, compare-match **b** is ignored, and the negative phase is turned off by compare-match **d**. This is because turning off of the positive phase has priority due to the occurrence of compare-match **c** (positive phase off timing) before compare-match **b** (positive phase on timing) (consequently, the waveform does not change since the positive phase goes from off to off).

Similarly, in the example in figure 10.48, compare-match **a'** with the new data in the temporary register occurs before compare-match **c**, but other compare-matches occurring up to **c**, which turns off the positive phase, are ignored. As a result, the negative phase is not turned on.

Thus, in complementary PWM mode, compare-matches at turn-off timings take precedence, and turn-on timing compare-matches that occur before a turn-off timing compare-match are ignored.

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
2	Serial mode register_2	SCSMR_2	R/W	H'0000	H'FFFE9000	16
	Bit rate register_2	SCBRR_2	R/W	H'FF	H'FFFE9004	8
	Serial control register_2	SCSCR_2	R/W	H'0000	H'FFFE9008	16
	Transmit FIFO data register_2	SCFTDR_2	W	Undefined	H'FFFE900C	8
	Serial status register_2	SCFSR_2	R/(W)*1	H'0060	H'FFFE9010	16
	Receive FIFO data register_2	SCFRDR_2	R	Undefined	H'FFFE9014	8
	FIFO control register_2	SCFCR_2	R/W	H'0000	H'FFFE9018	16
	FIFO data count register_2	SCFDR_2	R	H'0000	H'FFFE901C	16
	Serial port register_2	SCSPTR_2	R/W	H'0050	H'FFFE9020	16
	Line status register_2	SCLSR_2	R/(W)*2	H'0000	H'FFFE9024	16
	Serial extended mode register_2	SCSEMR_2	R/W	H'00	H'FFFE9100	8
3	Serial mode register_3	SCSMR_3	R/W	H'0000	H'FFFE9800	16
	Bit rate register_3	SCBRR_3	R/W	H'FF	H'FFFE9804	8
	Serial control register_3	SCSCR_3	R/W	H'0000	H'FFFE9808	16
	Transmit FIFO data register_3	SCFTDR_3	W	Undefined	H'FFFE980C	8
	Serial status register_3	SCFSR_3	R/(W)*1	H'0060	H'FFFE9810	16
	Receive FIFO data register_3	SCFRDR_3	R	Undefined	H'FFFE9814	8
	FIFO control register_3	SCFCR_3	R/W	H'0000	H'FFFE9818	16
	FIFO data count register_3	SCFDR_3	R	H'0000	H'FFFE981C	16
	Serial port register_3	SCSPTR_3	R/W	H'0050	H'FFFE9820	16
	Line status register_3	SCLSR_3	R/(W)*2	H'0000	H'FFFE9824	16

Notes: 1. Only 0 can be written to clear the flag. Bits 15 to 8, 3, and 2 are read-only bits that cannot be modified.

2. Only 0 can be written to clear the flag. Bits 15 to 1 are read-only bits that cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
5	PE	0	R/W	Parity Enable Selects whether to add a parity bit to transmit data and to check the parity of receive data, in asynchronous mode. In clocked synchronous mode, a parity bit is neither added nor checked, regardless of the PE setting. 0: Parity bit not added or checked 1: Parity bit added and checked* Note: * When PE is set to 1, an even or odd parity bit is added to transmit data, depending on the parity mode (O/$\overline{E}$) setting. Receive data parity is checked according to the even/odd (O/$\overline{E}$) mode setting.
4	O/$\overline{E}$	0	R/W	Parity mode Selects even or odd parity when parity bits are added and checked. The O/$\overline{E}$ setting is used only in asynchronous mode and only when the parity enable bit (PE) is set to 1 to enable parity addition and checking. The O/$\overline{E}$ setting is ignored in clocked synchronous mode, or in asynchronous mode when parity addition and checking is disabled. 0: Even parity*[1] 1: Odd parity*[2] Notes:1. If even parity is selected, the parity bit is added to transmit data to make an even number of 1s in the transmitted character and parity bit combined. Receive data is checked to see if it has an even number of 1s in the received character and parity bit combined. 2. If odd parity is selected, the parity bit is added to transmit data to make an odd number of 1s in the transmitted character and parity bit combined. Receive data is checked to see if it has an odd number of 1s in the received character and parity bit combined.

Figure 15.10 shows a sample flowchart for initializing the SCIF.

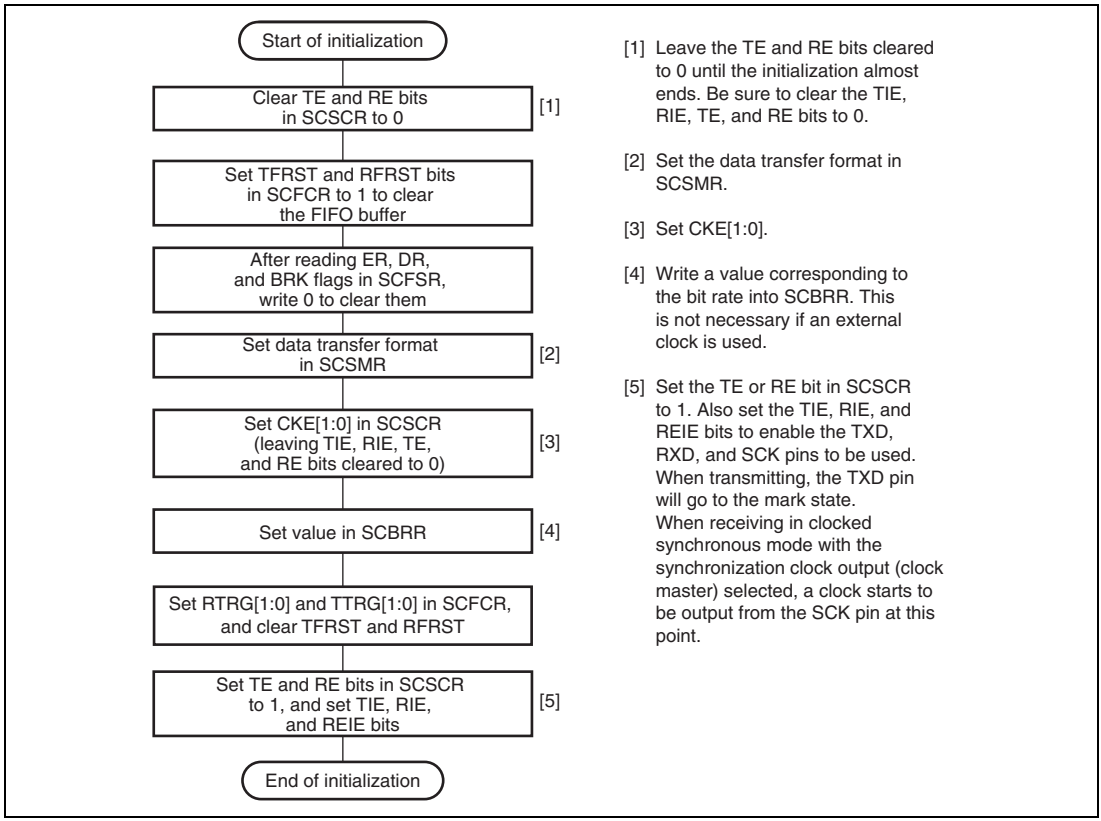


Figure 15.10 Sample Flowchart for SCIF Initialization

19.1.3 Port B I/O Registers H, L (PBIORH, PBIORL)

PBIORH and PBIORL are 16-bit readable/writable registers that are used to set the pins on port B as inputs or outputs. Bits PB30IOR to PB0IOR correspond to pins PB30 to PB0, respectively. PBIOR is enabled when the port B pins are functioning as general-purpose inputs/outputs (PB9, PB5, and PB4). In other states, PBIOR is disabled. A given pin on port B will be an output pin if the corresponding bit in PBIORH and PBIORL is set to 1, and an input pin if the bit is cleared to 0.

Bit 15 of PBIORH is reserved. This bit is always read as 0. The write value should always be 0.

PBIORH and PBIORL are initialized to H'0000 by a power-on reset; but are not initialized by a manual reset or in sleep mode or software standby mode.

(1) Port B I/O Register H (PBIORH)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PB30 IOR	PB29 IOR	PB28 IOR	PB27 IOR	PB26 IOR	PB25 IOR	PB24 IOR	PB23 IOR	PB22 IOR	PB21 IOR	PB20 IOR	PB19 IOR	PB18 IOR	PB17 IOR	PB16 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(2) Port B I/O Register L (PBIORL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PB15 IOR	PB14 IOR	PB13 IOR	PB12 IOR	PB11 IOR	PB10 IOR	PB9 IOR	PB8 IOR	PB7 IOR	PB6 IOR	PB5 IOR	PB4 IOR	PB3 IOR	PB2 IOR	PB1 IOR	PB0 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(4) Port B Control Register H1 (PBCRH1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PB19MD[2:0]			-	PB18MD[2:0]			-	PB17MD[2:0]			-	PB16MD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	PB19MD[2:0]	000	R/W	PB19 Mode Select the function of the PB19/$\overline{\text{CS6}}$/IRQ6/TIOC3D pin. 000: PB19 I/O (port) 001: $\overline{\text{CS6}}$ output (BSC) 010: Setting prohibited 011: IRQ6 input (INTC) 100: TIOC3D I/O (MTU2) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	PB18MD[2:0]	000	R/W	PB18 Mode Select the function of the PB18/$\overline{\text{CS4}}$/IRQ4/TIOC3B pin. 000: PB18 I/O (port) 001: $\overline{\text{CS4}}$ output (BSC) 010: Setting prohibited 011: IRQ4 input (INTC) 100: TIOC3B I/O (MTU2) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

23.3.4 Standby Control Register 4 (STBCR4)

STBCR4 is an 8-bit readable/writable register that controls the operation of modules in power-down modes. STBCR4 is initialized to H'F4 by a power-on reset but retains its previous value by a manual reset or in software standby mode. Only byte access is possible.

Bit:	7	6	5	4	3	2	1	0
	MSTP47	MSTP46	MSTP45	MSTP44	-	MSTP42	MSTP41	-
Initial value:	1	1	1	1	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP47	1	R/W	Module Stop 47 When the MSTP47 bit is set to 1, the supply of the clock to the SCIF0 is halted. 0: SCIF0 runs. 1: Clock supply to SCIF0 halted.
6	MSTP46	1	R/W	Module Stop 46 When the MSTP46 bit is set to 1, the supply of the clock to the SCIF1 is halted. 0: SCIF1 runs. 1: Clock supply to SCIF1 halted.
5	MSTP45	1	R/W	Module Stop 45 When the MSTP45 bit is set to 1, the supply of the clock to the SCIF2 is halted. 0: SCIF2 runs. 1: Clock supply to SCIF2 halted.
4	MSTP44	1	R/W	Module Stop 44 When the MSTP44 bit is set to 1, the supply of the clock to the SCIF3 is halted. 0: SCIF3 runs. 1: Clock supply to SCIF3 halted.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU2S	TOCR1S	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
	TOCR2S	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
	TGCRS	—	BDC	N	P	FB	WF	VF	UF
	TCDRS								
	TDDRS								
	TCNTSS								
	TCBRS								
	TITCRS	T3AEN	3ACOR[2:0]			T4VEN	4VCOR[2:0]		
	TITCNTS	—	3ACNT[2:0]			—	4VCNT[2:0]		
	TBTERS	—	—	—	—	—	—	BTE[1:0]	
	TDERS	—	—	—	—	—	—	—	TDER
	TSYCRS	CE0A	CE0B	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
	TWCRS	CCE	—	—	—	—	—	SCC	WRE
	TOLBRS	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
POE2	ICSR1	POE3F	—	POE1F	POE0F	—	—	—	PIE1
		POE3M[1:0]		POE2M[1:0]		POE1M[1:0]		POE0M[1:0]	
	OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1
		—	—	—	—	—	—	—	—
	ICSR2	POE7F	—	—	POE4F	—	—	—	PIE2
		POE7M[1:0]		—	—	—	—	POE4M[1:0]	
	OCSR2	OSF2	—	—	—	—	—	OCE2	OIE2
		—	—	—	—	—	—	—	—
	ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3
		—	—	—	—	—	—	POE8M[1:0]	
	SPOER	—	—	—	—	—	MTU2S HIZ	MTU2 CH0HIZ	MTU2 CH34HIZ

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
UBC	BBR_2	Initialized	Retained	Retained	Retained	Retained
	BAR_3	Initialized	Retained	Retained	Retained	Retained
	BAMR_3	Initialized	Retained	Retained	Retained	Retained
	BBR_3	Initialized	Retained	Retained	Retained	Retained
	BRCR	Initialized	Retained	Retained	Retained	Retained
BSC	CMNCR	Initialized	Retained	Retained	—	Retained
	CS0BCR	Initialized	Retained	Retained	—	Retained
	CS1BCR	Initialized	Retained	Retained	—	Retained
	CS2BCR	Initialized	Retained	Retained	—	Retained
	CS3BCR	Initialized	Retained	Retained	—	Retained
	CS4BCR	Initialized	Retained	Retained	—	Retained
	CS5BCR	Initialized	Retained	Retained	—	Retained
	CS6BCR	Initialized	Retained	Retained	—	Retained
	CS7BCR	Initialized	Retained	Retained	—	Retained
	CS0WCR	Initialized	Retained	Retained	—	Retained
	CS1WCR	Initialized	Retained	Retained	—	Retained
	CS2WCR	Initialized	Retained	Retained	—	Retained
	CS3WCR	Initialized	Retained	Retained	—	Retained
	CS4WCR	Initialized	Retained	Retained	—	Retained
	CS5WCR	Initialized	Retained	Retained	—	Retained
	CS6WCR	Initialized	Retained	Retained	—	Retained
	CS7WCR	Initialized	Retained	Retained	—	Retained
	SDCR	Initialized	Retained	Retained	—	Retained
	RTCSR	Initialized	Retained (Flag processing continued)	Retained	—	Retained (Flag processing continued)
	RTCNT	Initialized	Retained (Count-up continued)	Retained	—	Retained (Count-up continued)
	RTCOR	Initialized	Retained	Retained	—	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TCRU_5	Initialized	Retained	Retained	Initialized	Retained
	TCRV_5	Initialized	Retained	Retained	Initialized	Retained
	TCRW_5	Initialized	Retained	Retained	Initialized	Retained
	TIORU_5	Initialized	Retained	Retained	Initialized	Retained
	TIORV_5	Initialized	Retained	Retained	Initialized	Retained
	TIORW_5	Initialized	Retained	Retained	Initialized	Retained
	TIER_5	Initialized	Retained	Retained	Initialized	Retained
	TSR_5	Initialized	Retained	Retained	Initialized	Retained
	TSTR_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTU_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTV_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTW_5	Initialized	Retained	Retained	Initialized	Retained
	TGRU_5	Initialized	Retained	Retained	Initialized	Retained
	TGRV_5	Initialized	Retained	Retained	Initialized	Retained
	TGRW_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTCMPCLR	Initialized	Retained	Retained	Initialized	Retained
	TSTR	Initialized	Retained	Retained	Initialized	Retained
	TSYR	Initialized	Retained	Retained	Initialized	Retained
	TCSYSTR	Initialized	Retained	Retained	Initialized	Retained
	TRWER	Initialized	Retained	Retained	Initialized	Retained
	TOER	Initialized	Retained	Retained	Initialized	Retained
	TOCR1	Initialized	Retained	Retained	Initialized	Retained
	TOCR2	Initialized	Retained	Retained	Initialized	Retained
	TGCR	Initialized	Retained	Retained	Initialized	Retained
	TCDR	Initialized	Retained	Retained	Initialized	Retained
	TDDR	Initialized	Retained	Retained	Initialized	Retained
	TCNTS	Initialized	Retained	Retained	Initialized	Retained
	TCBR	Initialized	Retained	Retained	Initialized	Retained
	TITCR	Initialized	Retained	Retained	Initialized	Retained
	TITCNT	Initialized	Retained	Retained	Initialized	Retained
	TBTER	Initialized	Retained	Retained	Initialized	Retained

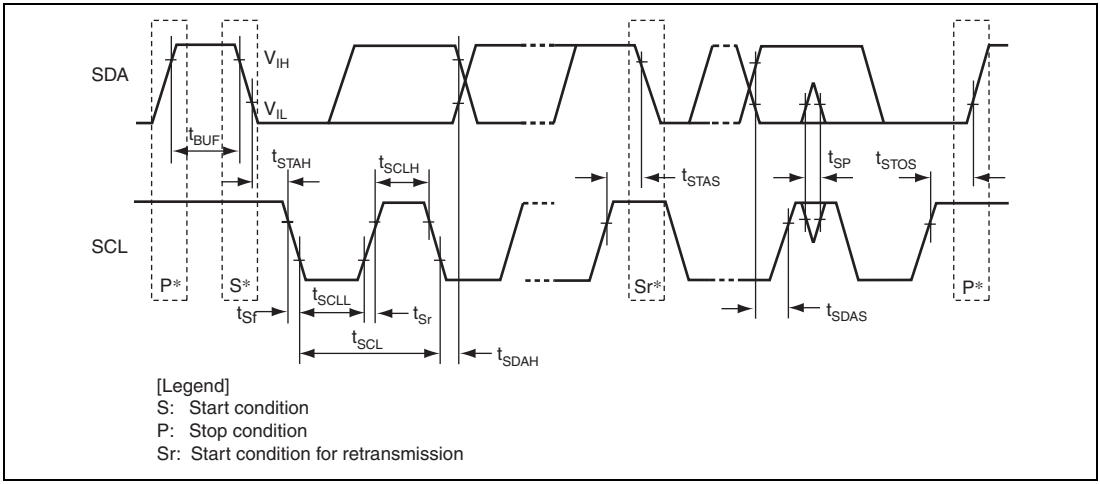


Figure 27.48 I²C Bus Interface 3 Input/Output Timing

27.4.11 A/D Trigger Input Timing

Table 27.16 A/D Trigger Input Timing

Conditions: Vcc = PLLVcc = 1.4 V to 1.6 V, VccQ = 3.0 V to 3.6 V,
Vss = PLLVss = VssQ = 0 V, Ta = –40°C to +85°C

Module	Item		Symbol	Min.	Max.	Unit	Figure
A/D converter	Trigger input setup time	B:P clock ratio = 1:1	t_{TRGS}	20	—	ns	Figure 27.49
		B:P clock ratio = 2:1		t_{cyc} + 20	—		
		B:P clock ratio = 4:1		3 × t_{cyc} + 20	—		

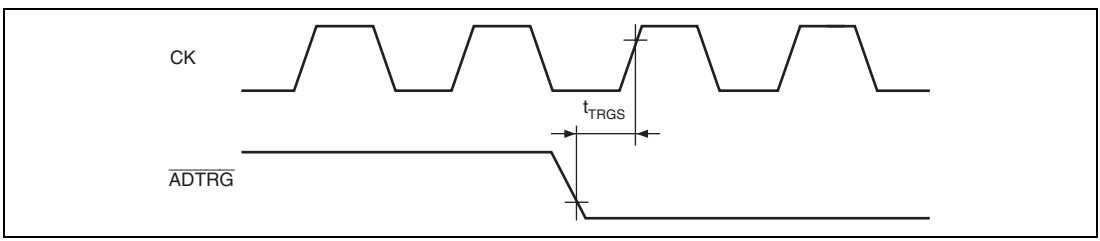
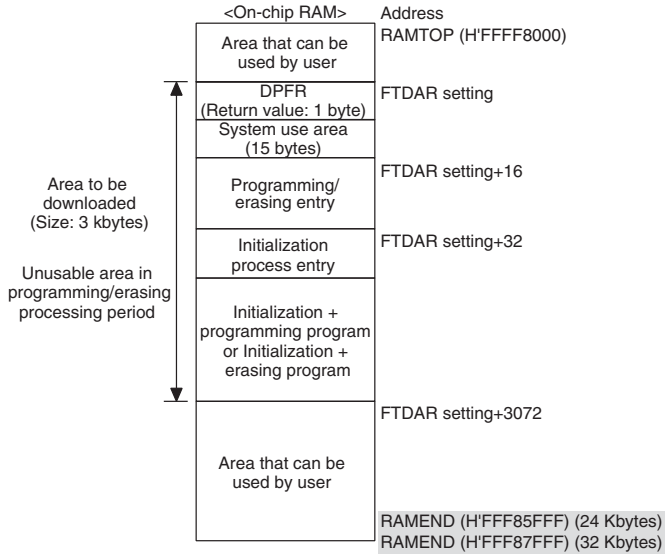


Figure 27.49 A/D Converter External Trigger Input Timing

Item	Page	Revision (See Manual for Details)
21.5.2 User Program Mode (1) On-Chip RAM Address Map when Programming/Erasing is Executed Figure 21.10 RAM Map after Download	925	Figure amended 
21.7.2 Interrupts during Programming/Erasing (2) Interrupts during Programming/Erasing	946	Description amended Ensure that NMI, IRQ, and all other interrupts are not generated during programming or erasing of on-chip program code.
21.8.2 Areas for Storage of the Procedural Program and Data for Programming	980	Description amended 5. The flash memory is not accessible during programming and erasing, so programs must be loaded into the on-chip RAM to perform these operations. Space in on-chip RAM other than flash memory, or external bus space, must be available for each procedure program for initiating programming or erasing, and for user programs at user branch destinations during programming or erasing.
Table 21.17 (1) Usable Area for Programming in User Program Mode	981	Table amended

	Storable/Executable Area			Selected MAT	
Item	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT
Initialization error processing	√	√	√	√	
Writing H'5A to key register	√	√	√	√	