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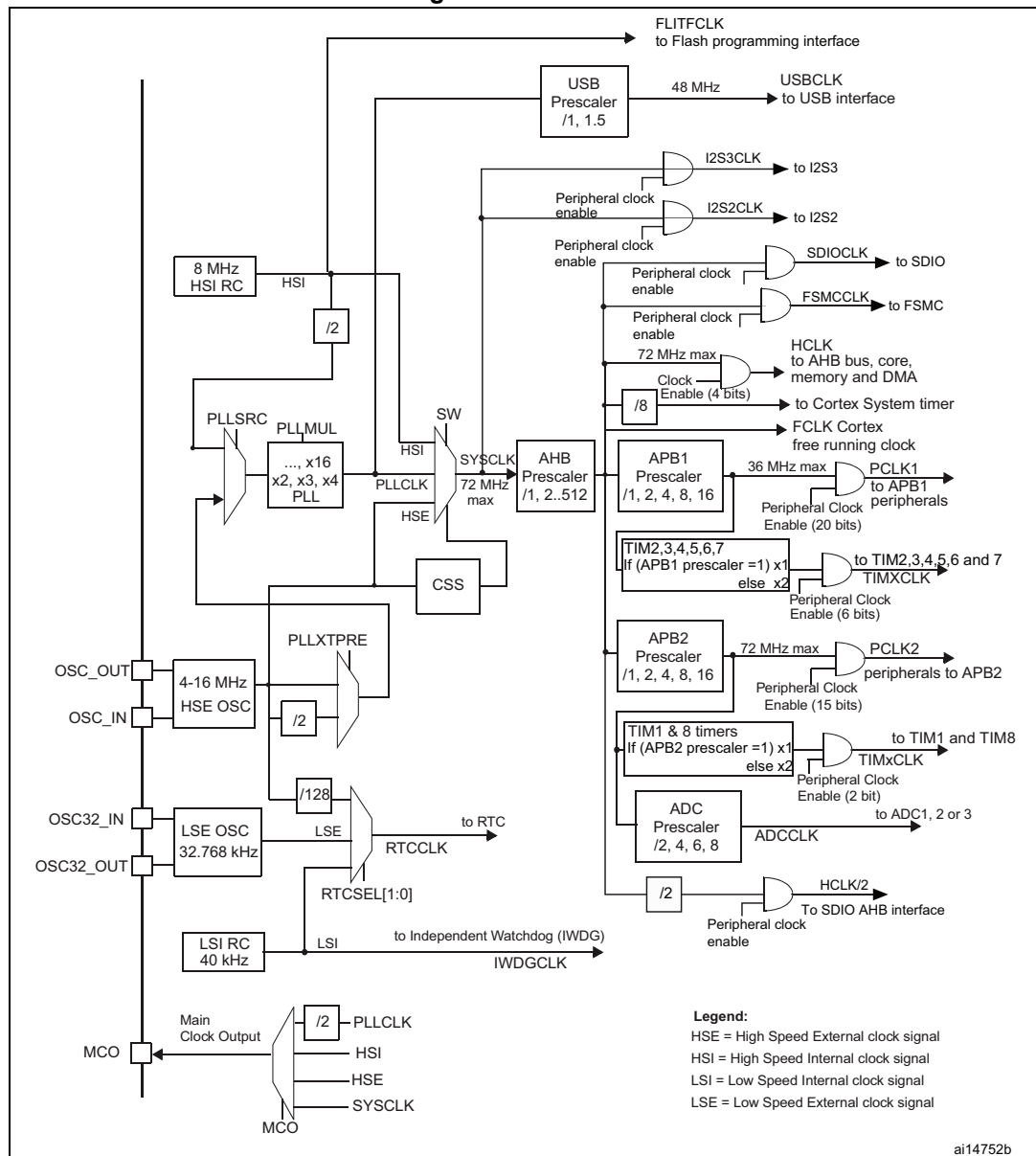
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rct7

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the USBCLK at 48 MHz.
3. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See [Figure 2](#) for details on the clock tree.

2.3.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.11 Power supply schemes

- $V_{DD} = 2.0$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 2.0$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.8$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 12: Power supply scheme](#).

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to [Table 12: Embedded reset and power control block characteristics](#) for the values of $V_{POR/PDR}$ and V_{PVD} .

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type ⁽¹⁾	I / O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
L4	J4	H4	26	35	46	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	F4	27	36	47	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4 ⁽⁹⁾ TIM8_CH3N	TIM1_CH3N
J5	G5	H3	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	-	-	51	V _{SS_6}	S	-	V _{SS_6}	-	-
G5	-	-	-	-	52	V _{DD_6}	S	-	V _{DD_6}	-	-
K5	-	-	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	H5	-	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	-	-	61	V _{SS_7}	S	-	V _{SS_7}	-	-
G6	-	-	-	-	62	V _{DD_7}	S	-	V _{DD_7}	-	-
J7	G6	-	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	G3	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX ⁽⁹⁾	TIM2_CH3
M10	K7	F3	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX ⁽⁹⁾	TIM2_CH4
H7	E7	H2	31	49	71	V _{SS_1}	S	-	V _{SS_1}	-	-
G7	F7	H1	32	50	72	V _{DD_1}	S	-	V _{DD_1}	-	-

Table 6. FSMC pin definition

Pins	FSMC					LQFP100 BGA100 ⁽¹⁾
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 14. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max ⁽¹⁾		Unit
				$T_A = 85\text{ }^{\circ}\text{C}$	$T_A = 105\text{ }^{\circ}\text{C}$	
I_{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled	72 MHz	69	70	mA
			48 MHz	50	50.5	
			36 MHz	39	39.5	
			24 MHz	27	28	
			16 MHz	20	20.5	
			8 MHz	11	11.5	
		External clock ⁽²⁾ , all peripherals disabled	72 MHz	37	37.5	
			48 MHz	28	28.5	
			36 MHz	22	22.5	
			24 MHz	16.5	17	
			16 MHz	12.5	13	
			8 MHz	8	8	

1. Guaranteed by characterization results.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8\text{ MHz}$.

Table 15. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max ⁽¹⁾		Unit
				$T_A = 85\text{ }^{\circ}\text{C}$	$T_A = 105\text{ }^{\circ}\text{C}$	
I_{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled	72 MHz	66	67	mA
			48 MHz	43.5	45.5	
			36 MHz	33	35	
			24 MHz	23	24.5	
			16 MHz	16	18	
			8 MHz	9	10.5	
		External clock ⁽²⁾ , all peripherals disabled	72 MHz	33	33.5	
			48 MHz	23	23.5	
			36 MHz	18	18.5	
			24 MHz	13	13.5	
			16 MHz	10	10.5	
			8 MHz	6	6.5	

1. Guaranteed by characterization results at V_{DD} max, f_{HCLK} max.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8\text{ MHz}$.

Figure 19. Typical current consumption in Standby mode versus temperature at different V_{DD} values

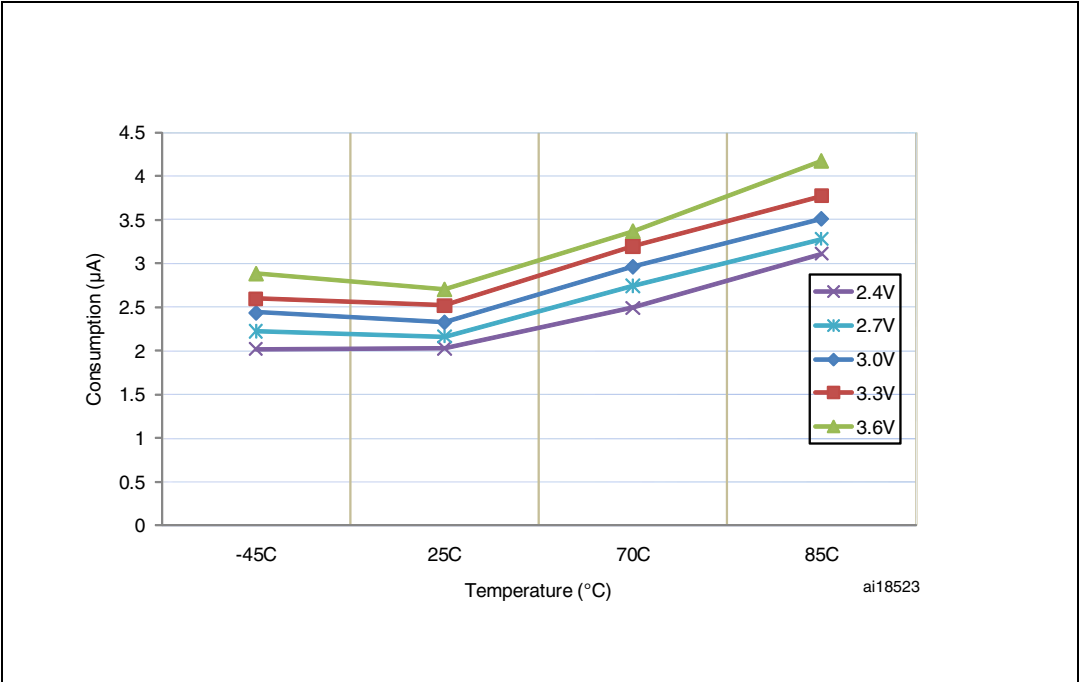


Figure 20. High-speed external clock source AC timing diagram

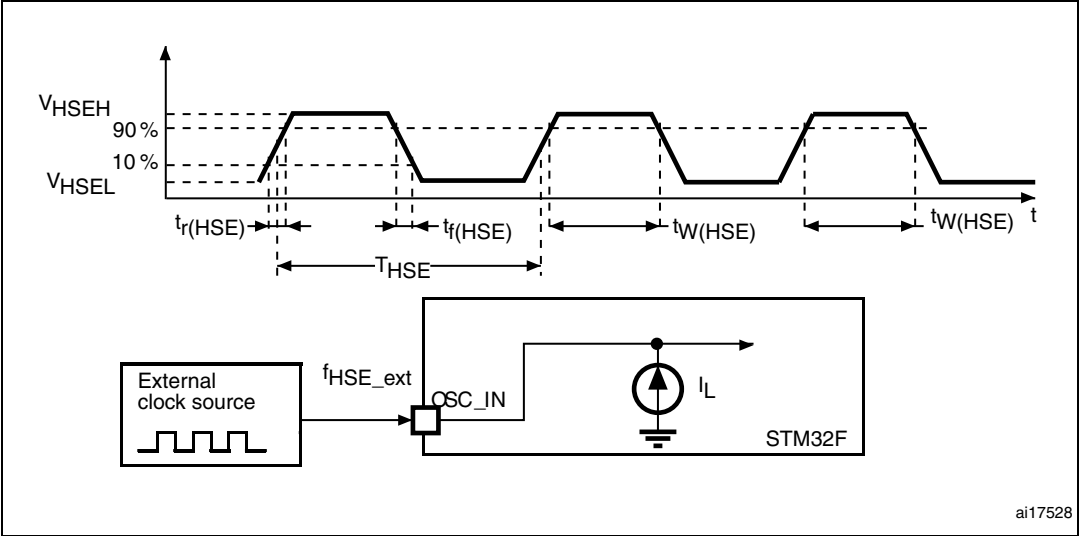


Figure 21. Low-speed external clock source AC timing diagram

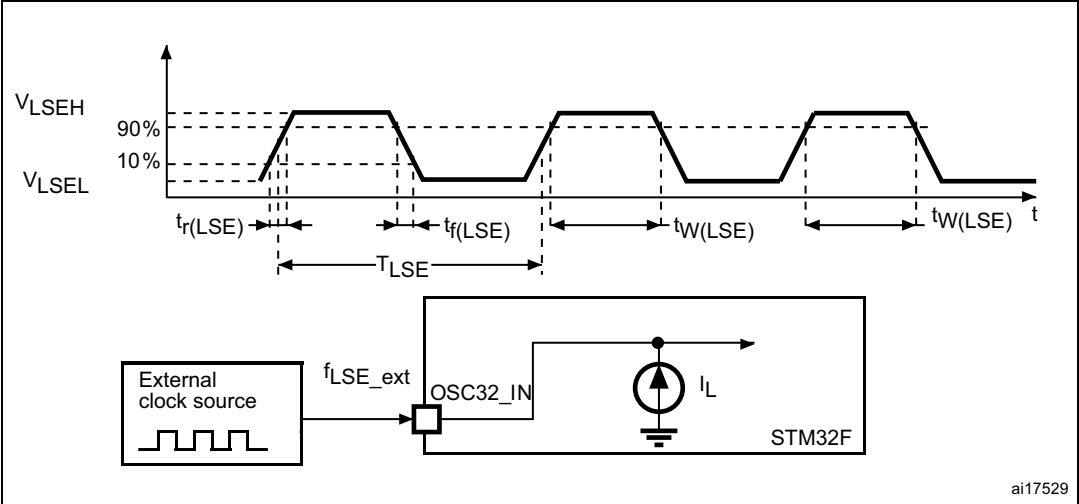
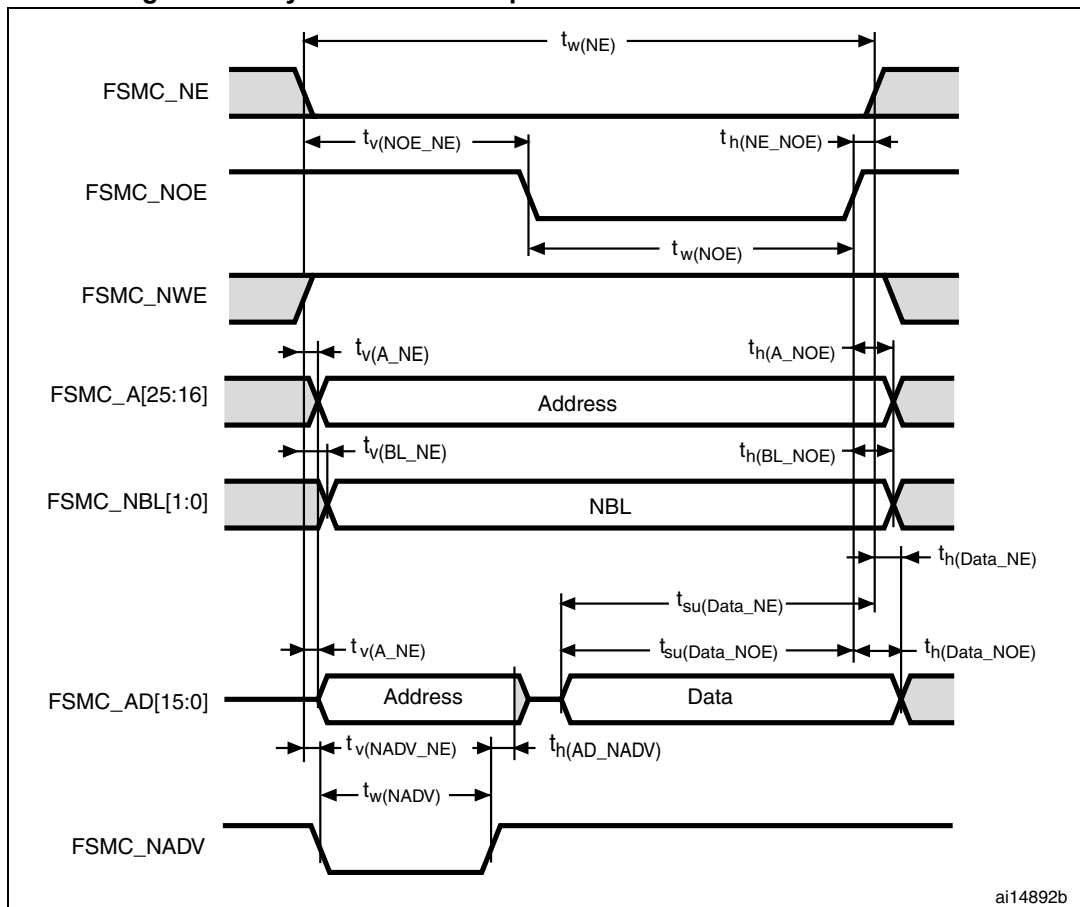


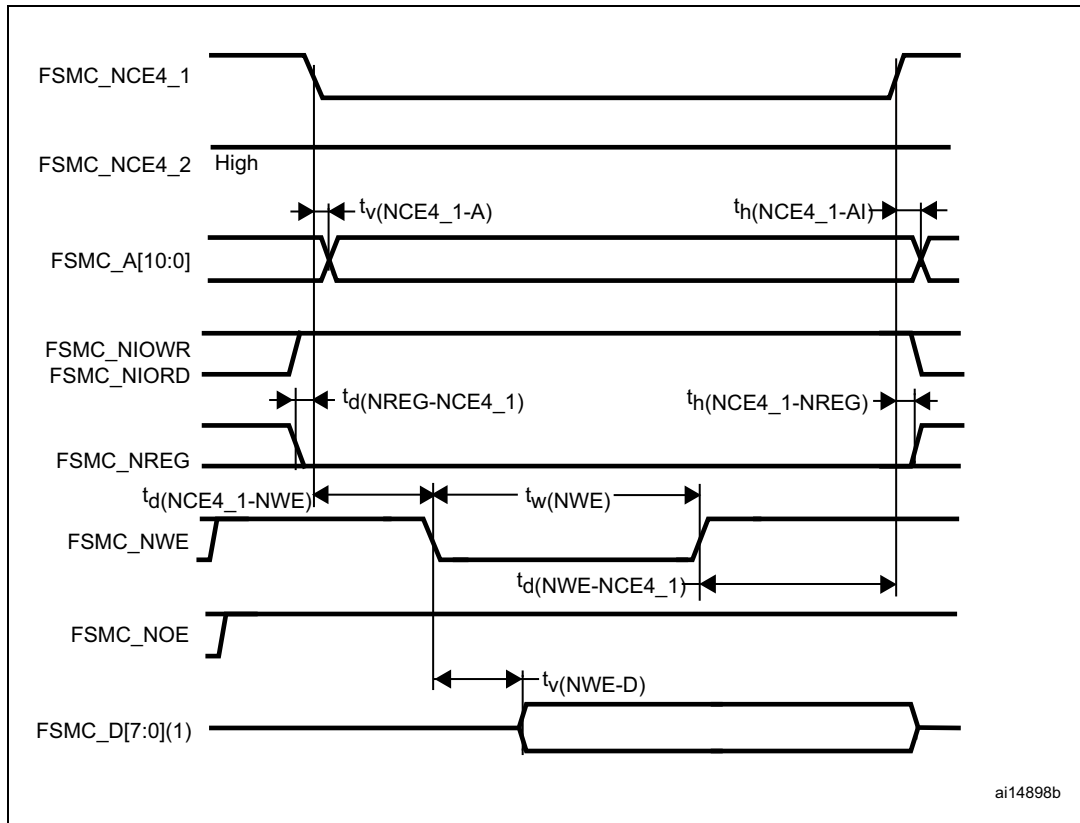
Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms



ai14892b

Table 33. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FSMC_NE low time	$7t_{HCLK} - 2$	$7t_{HCLK} + 2$	ns
$t_v(NOE_NE)$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1.5$	ns
$t_w(NOE)$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 2$	ns
$t_h(NE_NOE)$	FSMC_NOE high to FSMC_NE high hold time	-1	-	ns
$t_v(A_NE)$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_v(NADV_NE)$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_w(NADV)$	FSMC_NADV low time	$t_{HCLK} - 1.5$	$t_{HCLK} + 1.5$	ns
$t_h(AD_NADV)$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_h(A_NOE)$	Address hold time after FSMC_NOE high	$t_{HCLK} - 2$	-	ns
$t_h(BL_NOE)$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_v(BL_NE)$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su}(Data_NE)$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 24$	-	ns
$t_{su}(Data_NOE)$	Data to FSMC_NOE high setup time	$2t_{HCLK} + 25$	-	ns

Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access

1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

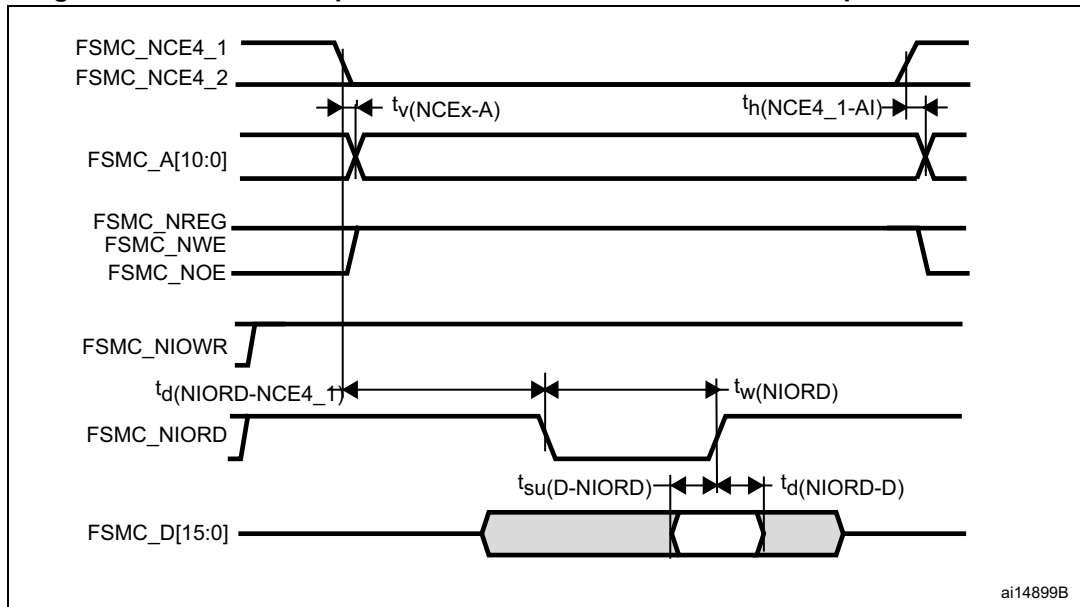
Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access

Figure 42. Standard I/O input characteristics - CMOS port

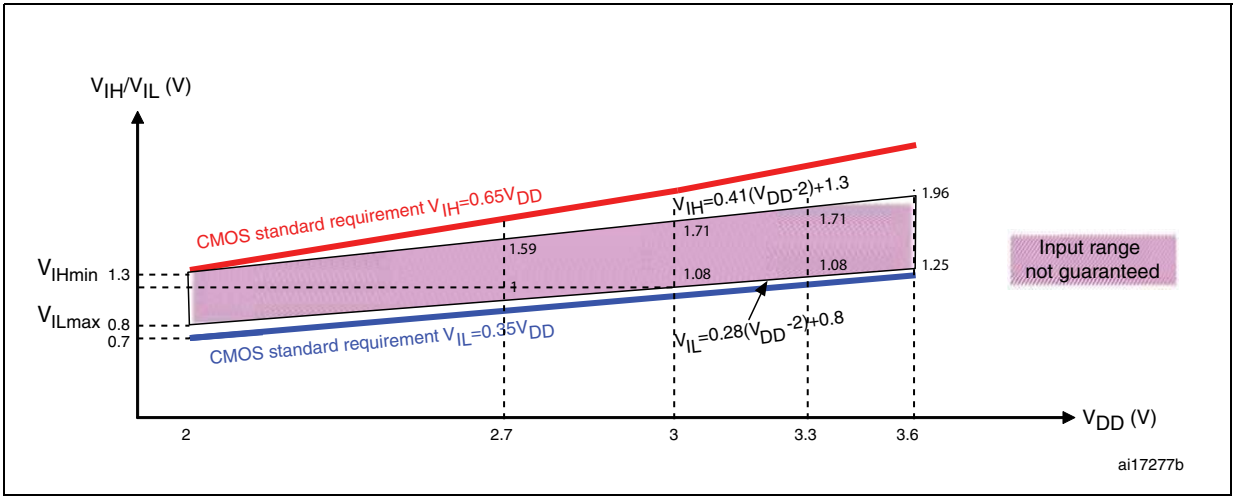


Figure 43. Standard I/O input characteristics - TTL port

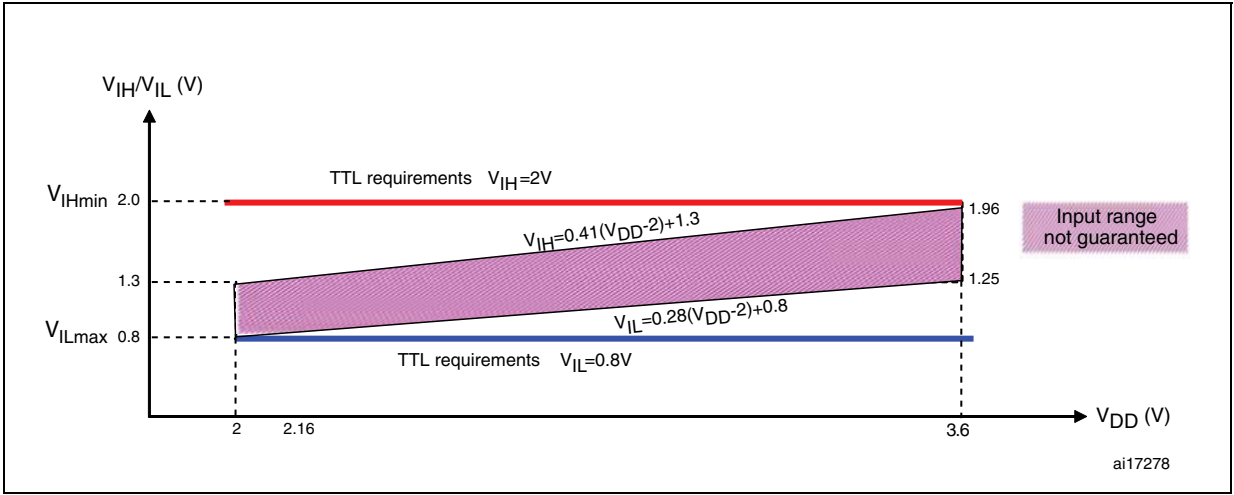


Figure 44. 5 V tolerant I/O input characteristics - CMOS port

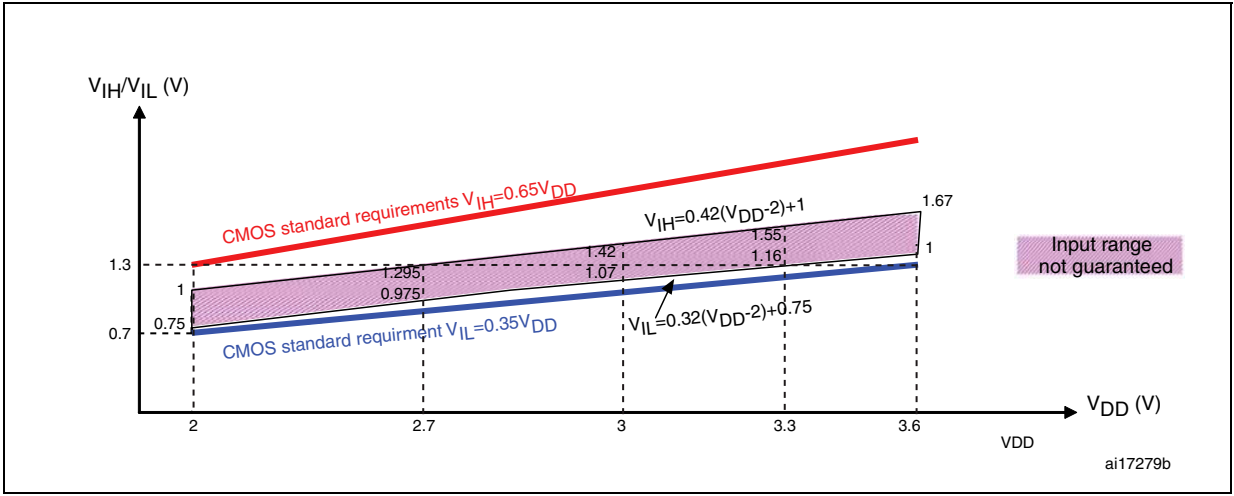


Table 47. Output voltage characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(2)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(2)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 8](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 8](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results.

5.3.18 CAN (controller area network) interface

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 10](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 59. ADC characteristics

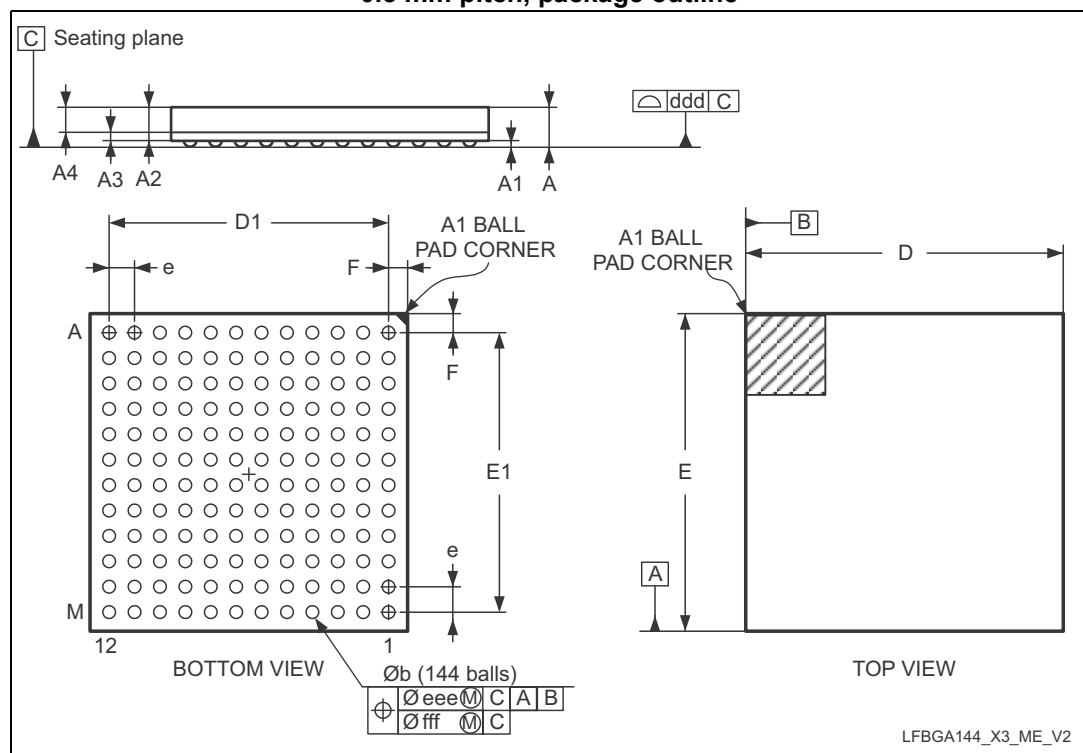
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Current on the V_{REF} input pin	-	-	160 ⁽¹⁾	220	μ A
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_S^{(2)}$	Sampling rate	-	0.05	-	1	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 14$ MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range ⁽³⁾	-	0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
$R_{AIN}^{(2)}$	External input impedance	See Equation 1 and Table 60 for details	-	-	50	$\kappa\Omega$
$R_{ADC}^{(2)}$	Sampling switch resistance	-	-	-	1	$\kappa\Omega$
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{CAL}^{(2)}$	Calibration time	$f_{ADC} = 14$ MHz	5.9			μ s
		-	83			$1/f_{ADC}$
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.214	μ s
		-	-	-	3 ⁽⁴⁾	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.143	μ s
		-	-	-	2 ⁽⁴⁾	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 14$ MHz	0.107	-	17.1	μ s
		-	1.5	-	239.5	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time	-	0	0	1	μ s
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 14$ MHz	1	-	18	μ s
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

6.1 LFBGA144 package information

Figure 62. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline



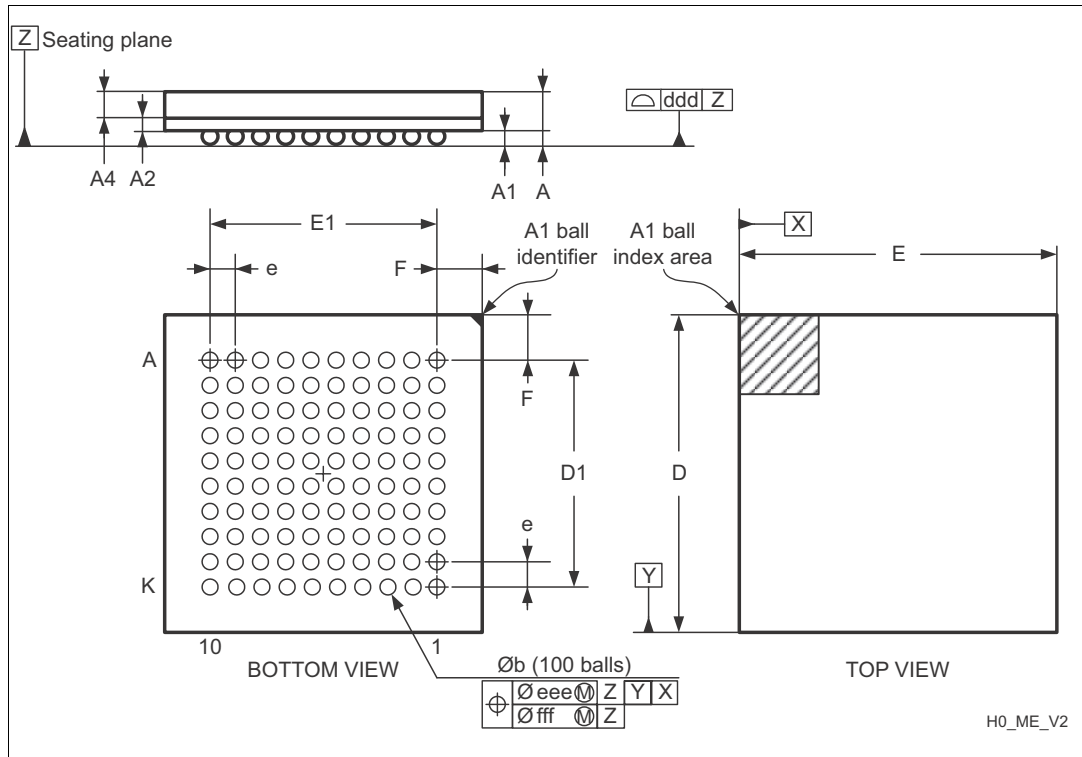
1. Drawing is not to scale.

Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Typ	Min	Max
A ⁽²⁾	-	-	1.700	-	-	0.0669
A1	0.250	0.300	0.350	0.098	0.0118	0.0138
A2	0.810	0.910	1.010	0.0319	0.0358	0.0398
A3	0.225	0.26	0.295	0.0089	0.0102	0.0116
A4	0.585	0.650	0.715	0.0230	0.0256	0.0281

6.2 LFBGA100 package information

Figure 65. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline



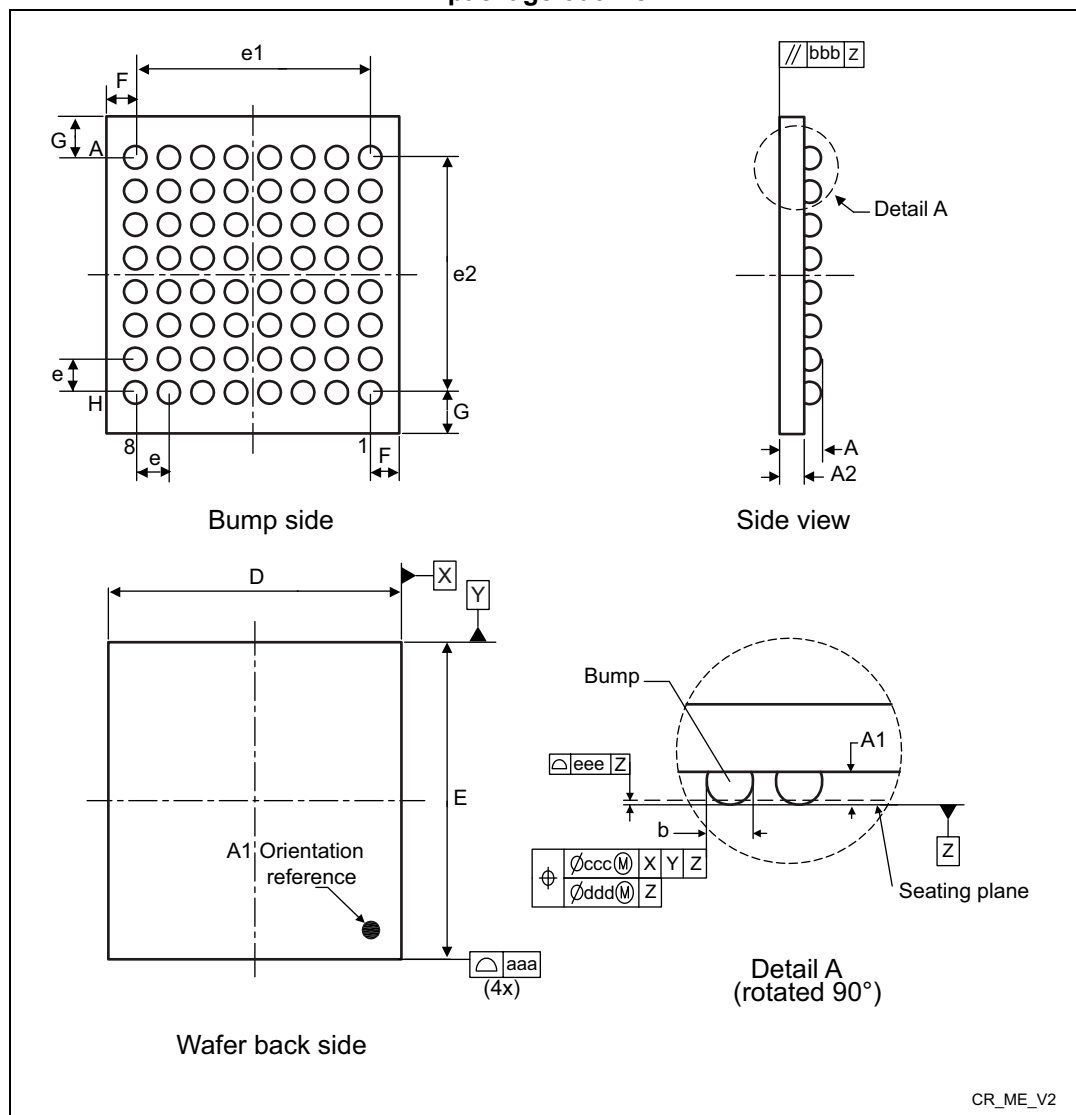
1. Drawing is not to scale.

Table 67. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.700	-	-	0.0669
A1	0.270	-	-	0.0106	-	-
A2	-	0.300	-	-	0.0118	-
A4	-	-	0.800	-	-	0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	7.200	-	-	0.2835	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	1.400	-	-	0.0551	-
ddd	-	-	0.120	-	-	0.0047

6.3 WLCSP64 package information

Figure 68. WLCSP, 64-ball 4.466×4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline



1. Drawing is not to scale.
2. Primary datum Z and seating plane are defined by the spherical crowns of the ball.

Table 69. WLCSP, 64-ball 4.466×4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data

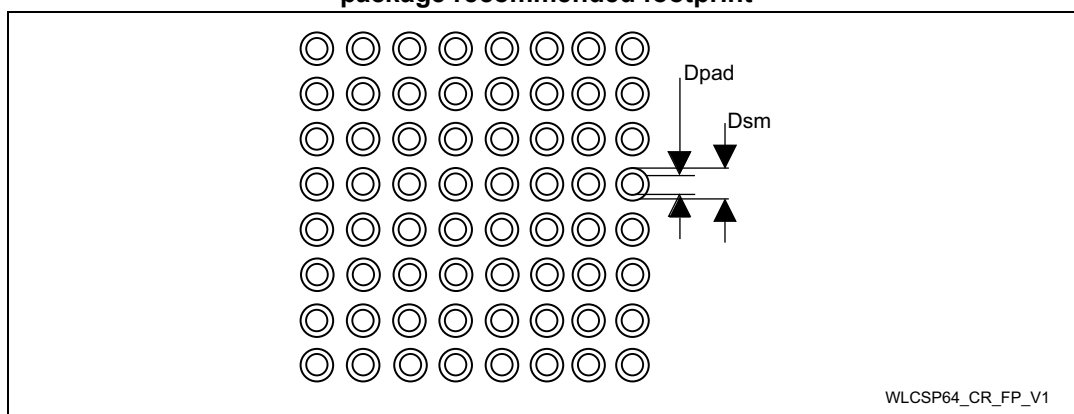
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.535	0.585	0.635	0.0211	0.0230	0.0250
A1	0.205	0.230	0.255	0.0081	0.0091	0.0100
A2	0.330	0.355	0.380	0.0130	0.0140	0.0150
b ⁽²⁾	0.290	0.320	0.350	0.0114	0.0126	0.0138

Table 69. WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
e1	-	3.500	-	-	0.1378	-
F	-	0.447	-	-	0.0176	-
G	-	0.483	-	-	0.0190	-
D	4.446	4.466	4.486	0.1750	0.1758	0.1766
E	4.375	4.395	4.415	0.1722	0.1730	0.1738
H	-	0.250	-	-	0.0098	-
L	-	0.200	-	-	0.0079	-
eee	-	0.05	-	-	0.0020	-
aaa	-	0.10	-	-	0.0039	-
Number of balls	64					

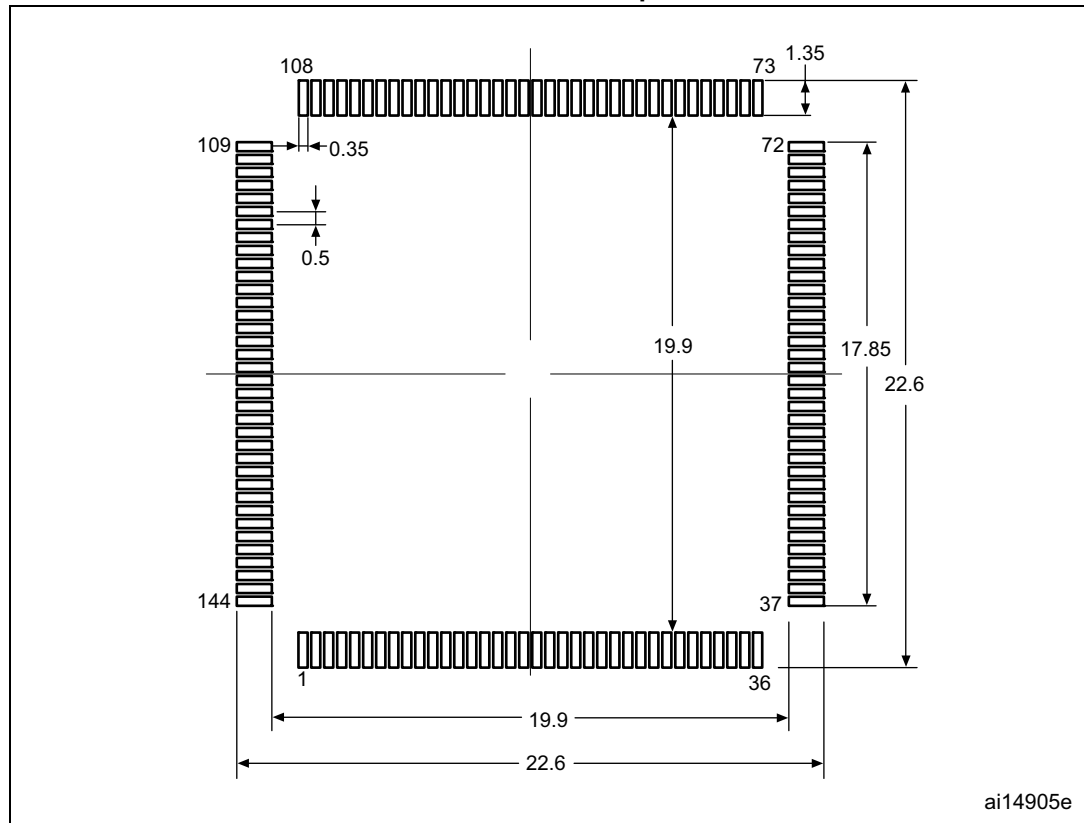
1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Dimension is measured at the maximum ball diameter parallel to primary datum Z.

Figure 69. WLCSP64 - 64-ball, 4.4757 x 4.4049 mm, 0.5 mm pitch wafer level chip scale package recommended footprint**Table 70. WLCSP64 recommended PCB design rules (0.5 mm pitch)**

Dimension	Recommended values
Pitch	0.5
Dpad	250 µm
Dsm	300 µm
Stencil Opening	320 µm
Stencil Thickness	Between 100 µm to 125 µm
Pad trace width	100 µm
Ball Diameter	320 µm

Figure 71. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

1. Dimensions are in millimeters.

6.7 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 10: General operating conditions on page 44](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LFBGA144 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	30	
	Thermal resistance junction-ambient LFBGA100 - 10 × 10 mm / 0.8 mm pitch	40	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient WLCSP64	50	

6.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org