



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (4.4x4.4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rcy6ctr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rcy6ctr</a>

---

5.3.20	DAC electrical specifications .....	112
5.3.21	Temperature sensor characteristics .....	114
<b>6</b>	<b>Package information .....</b>	<b>115</b>
6.1	LFBGA144 package information .....	115
6.2	LFBGA100 package information .....	118
6.3	WLCSP64 package information .....	121
6.4	LQFP144 package information .....	123
6.5	LQFP100 package information .....	127
6.6	LQFP64 package information .....	130
6.7	Thermal characteristics .....	133
6.7.1	Reference document .....	133
6.7.2	Selecting the product temperature range .....	134
<b>7</b>	<b>Part numbering .....</b>	<b>136</b>
<b>8</b>	<b>Revision history .....</b>	<b>137</b>

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xC, STM32F103xD and STM32F103xE high-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xC/D/E family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The high-density STM32F103xC/D/E datasheet should be read in conjunction with the STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website at the following address:  
<http://infocenter.arm.com>.



### Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

### Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 2.3.27 DAC (digital-to-analog converter)

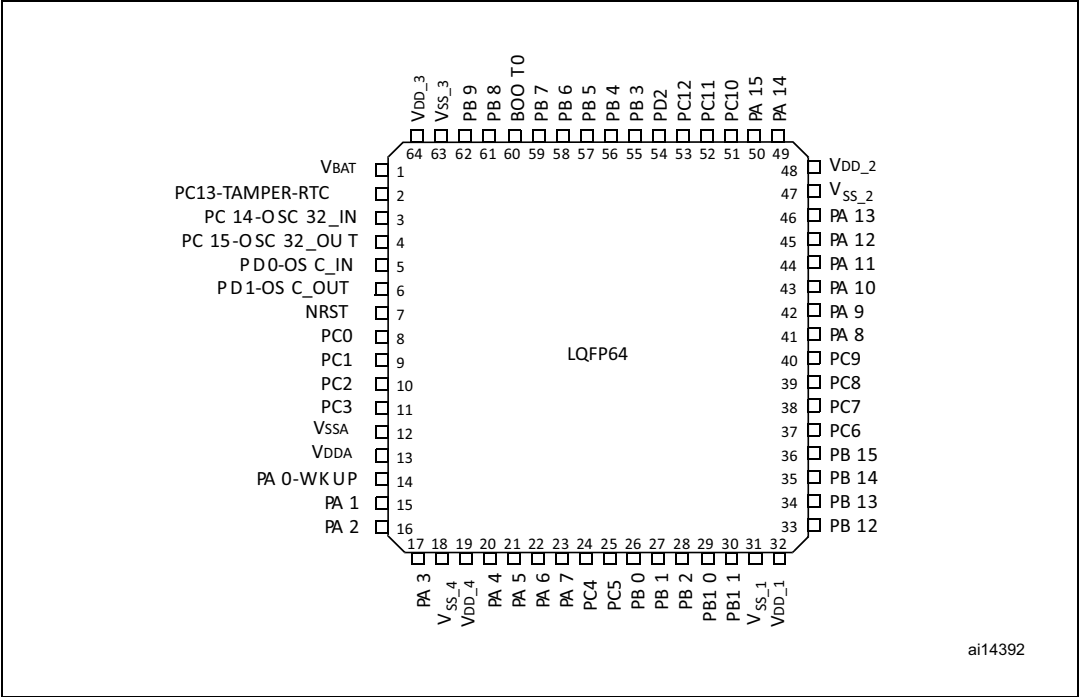
The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference  $V_{REF+}$

Eight DAC trigger inputs are used in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

Figure 7. STM32F103xC/D/E performance line LQFP64 pinout



1. The above figure shows the package top view.

### 5.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 11](#) are derived from tests performed under the ambient temperature condition summarized in [Table 10](#).

**Table 11. Operating conditions at power-up / power-down**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	-	0	$\infty$	$\mu\text{s/V}$
	$V_{DD}$ fall time rate		20	$\infty$	

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 12](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 10](#).

**Table 12. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(1)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}^{(2)}$	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

2. Guaranteed by design.

Figure 17. Typical current consumption in Stop mode with regulator in run mode versus temperature at different  $V_{DD}$  values

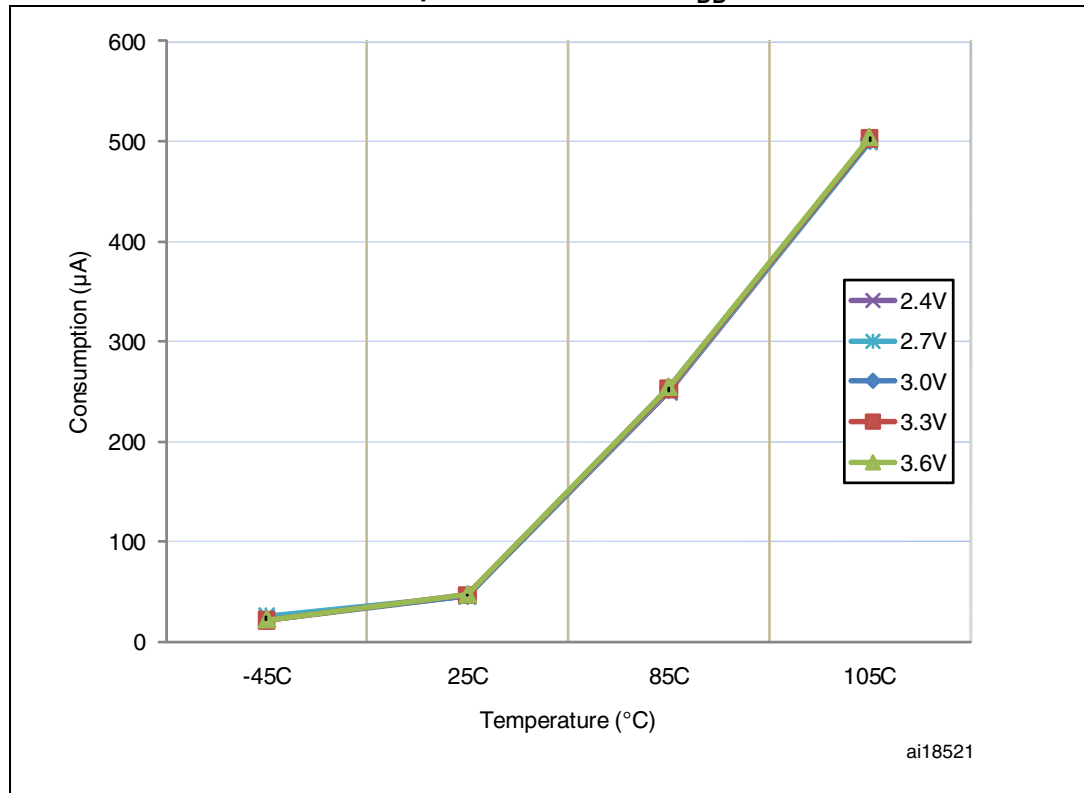
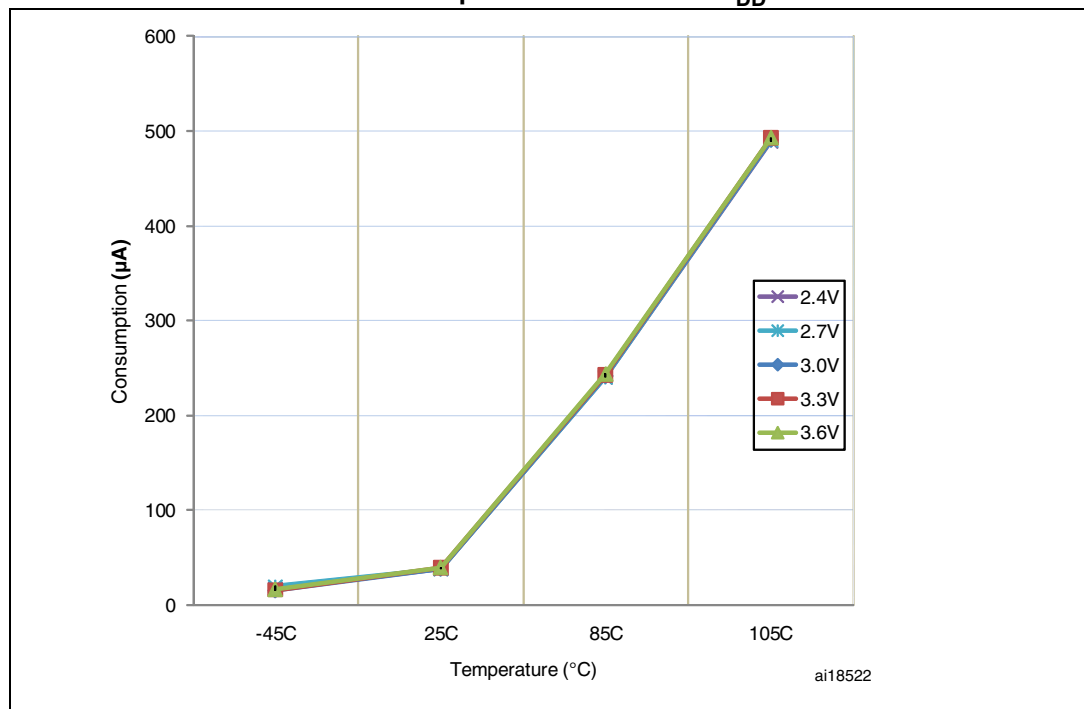


Figure 18. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different  $V_{DD}$  values





### Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 10](#).
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)

When the peripherals are enabled  $f_{PCLK1} = f_{HCLK}/4$ ,  $f_{PCLK2} = f_{HCLK}/2$ ,  $f_{ADCCLK} = f_{PCLK2}/4$

**Table 18. Typical current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	$f_{HCLK}$	Typ <sup>(1)</sup>		Unit
				All peripherals enabled <sup>(2)</sup>	All peripherals disabled	
$I_{DD}$	Supply current in Run mode	External clock <sup>(3)</sup>	72 MHz	51	30.5	mA
			48 MHz	34.6	20.7	
			36 MHz	26.6	16.2	
			24 MHz	18.5	11.4	
			16 MHz	12.8	8.2	
			8 MHz	7.2	5	
			4 MHz	4.2	3.1	
			2 MHz	2.7	2.1	
			1 MHz	2	1.7	
			500 kHz	1.6	1.4	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45	27	mA
			48 MHz	34	20.1	
			36 MHz	26	15.6	
			24 MHz	17.9	10.8	
			16 MHz	12.2	7.6	
			8 MHz	6.6	4.4	
			4 MHz	3.6	2.5	
			2 MHz	2.1	1.5	
			1 MHz	1.4	1.1	
			500 kHz	1	0.8	
			125 kHz	0.7	0.6	

1. Typical values are measures at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ .

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC\_CR2 register).

3. External clock is 8 MHz and PLL is on when  $f_{HCLK} > 8\text{ MHz}$ .

Figure 20. High-speed external clock source AC timing diagram

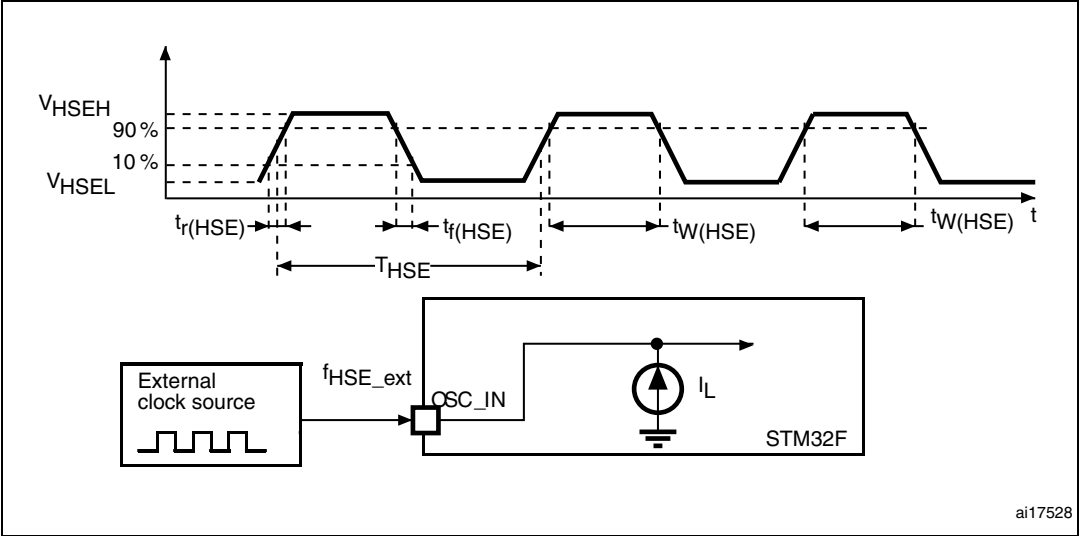


Figure 21. Low-speed external clock source AC timing diagram

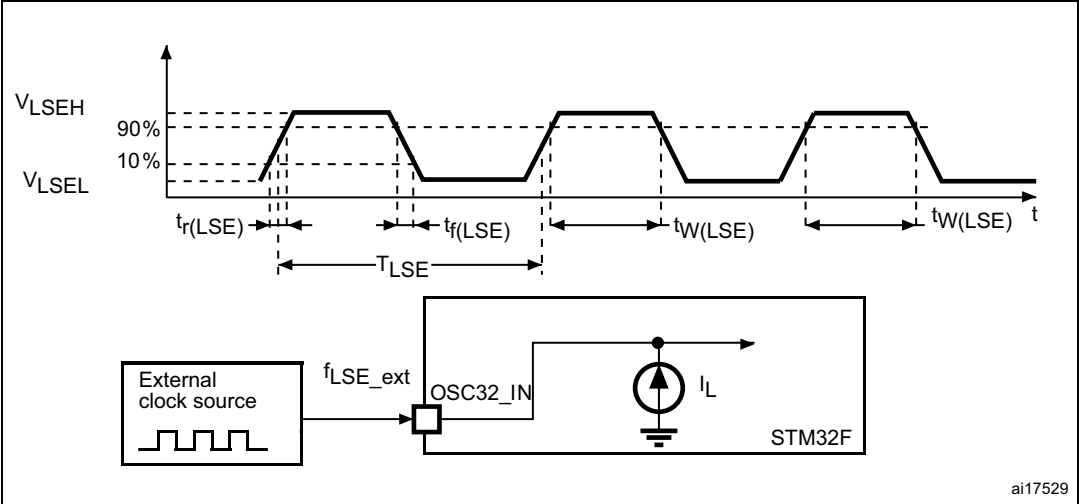
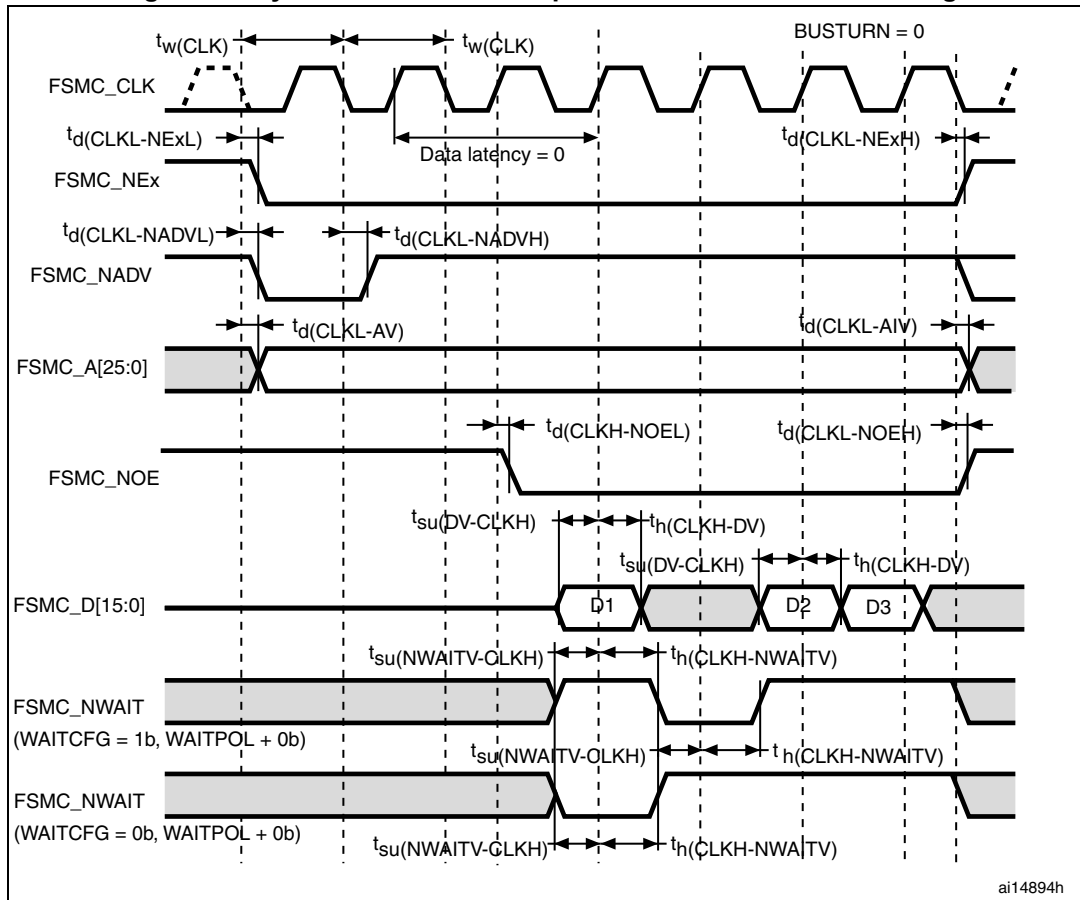


Figure 30. Synchronous non-multiplexed NOR/PSRAM read timings

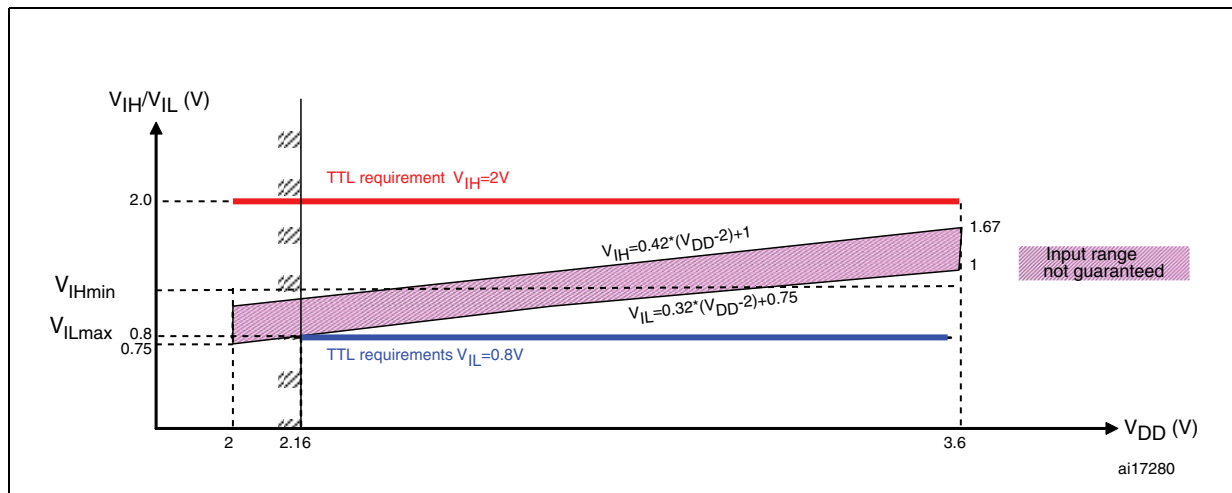
Table 37. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup>

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FSMC_CLK period	27.7	-	ns
$t_d(\text{CLKL-NExL})$	FSMC_CLK low to FSMC_NEx low ( $x = 0 \dots 2$ )	-	1.5	ns
$t_d(\text{CLKL-NExH})$	FSMC_CLK low to FSMC_NEx high ( $x = 0 \dots 2$ )	2	-	ns
$t_d(\text{CLKL-NADV})$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_d(\text{CLKL-NADVH})$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_d(\text{CLKL-AV})$	FSMC_CLK low to FSMC_Ax valid ( $x = 0 \dots 25$ )	-	0	ns
$t_d(\text{CLKL-AIV})$	FSMC_CLK low to FSMC_Ax invalid ( $x = 0 \dots 25$ )	4	-	ns
$t_d(\text{CLKL-NOEL})$	FSMC_CLK low to FSMC_NOE low	-	1.5	ns
$t_d(\text{CLKL-NOEH})$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su}(\text{DV-CLKH})$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5	-	ns
$t_h(\text{CLKH-DV})$	FSMC_D[15:0] valid data after FSMC_CLK high	7	-	ns
$t_{su}(\text{NWAITV-CLKH})$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_h(\text{CLKH-NWAITV})$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1.  $C_L = 15 \text{ pF}$ .

2. Guaranteed by characterization results.

Figure 45. 5 V tolerant I/O input characteristics - TTL port



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ) except PC13, PC14 and PC15 which can sink or source up to  $\pm 3$  mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $I_{VDD}$  (see [Table 8](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $I_{VSS}$  (see [Table 8](#)).

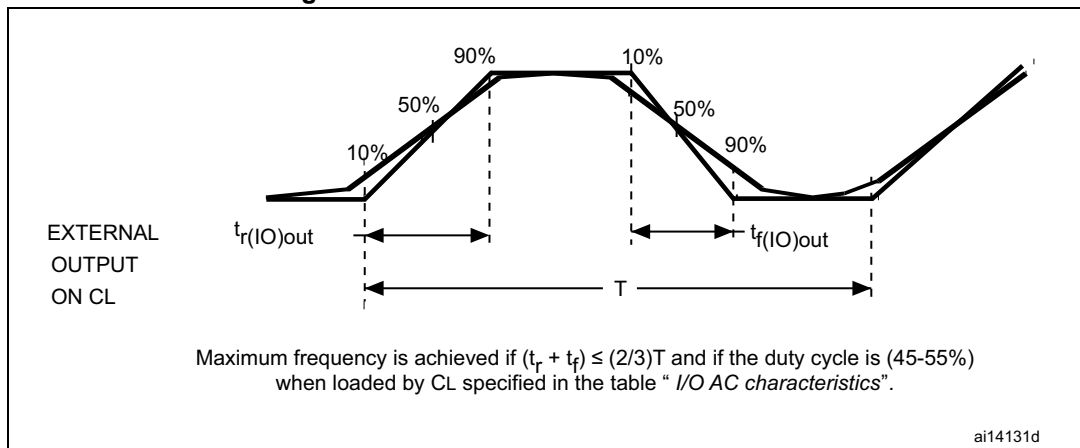
### Output voltage levels

Unless otherwise specified, the parameters given in [Table 47](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 10](#). All I/Os are CMOS and TTL compliant.

Table 47. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port <sup>(3)</sup> $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port <sup>(3)</sup> $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	

Figure 46. I/O AC characteristics definition



### 5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 46](#)).

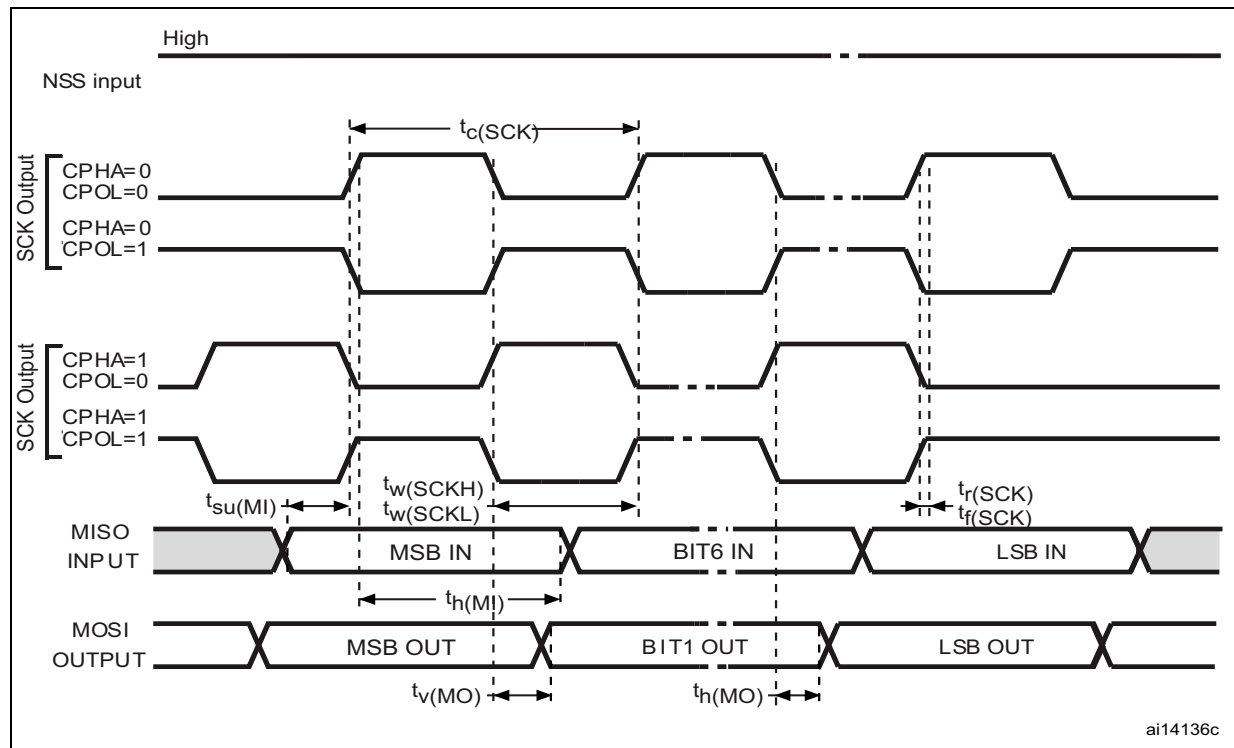
Unless otherwise specified, the parameters given in [Table 49](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 10](#).

Table 49. NRST pin characteristics

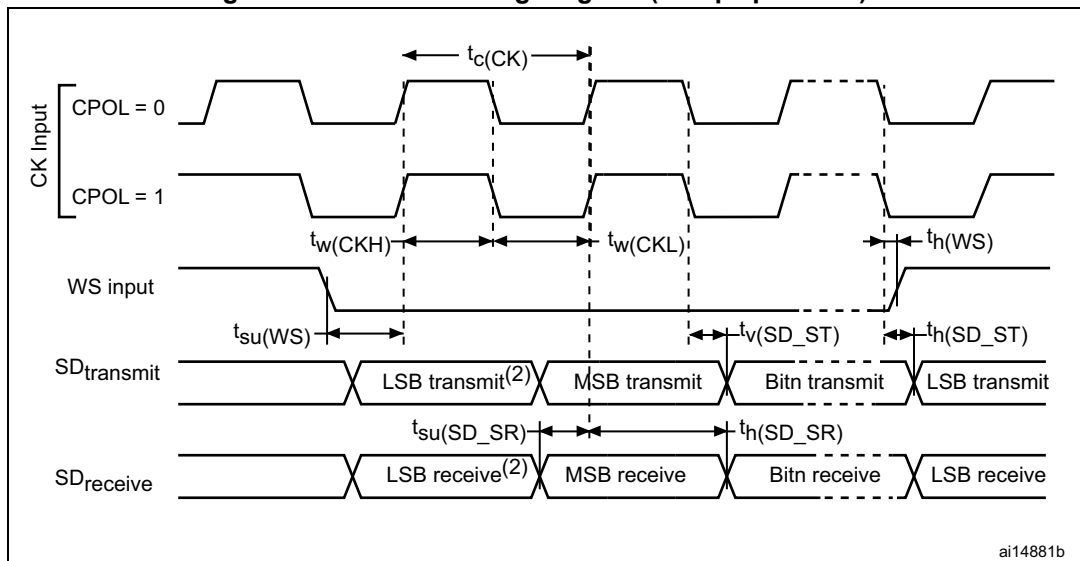
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	-	2	-	$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
$R_{PU}$	Weak pull-up equivalent resistor <sup>(2)</sup>	$V_{IN} = V_{SS}$	30	40	50	k $\Omega$
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design.

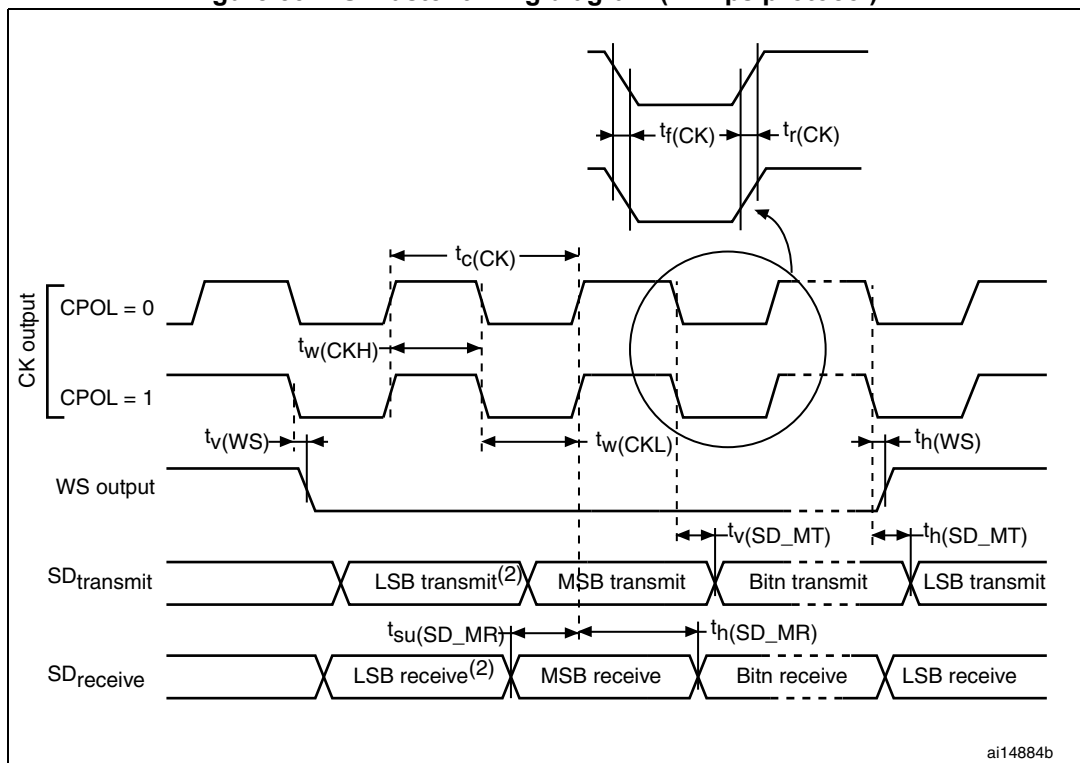
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 51. SPI timing diagram - master mode<sup>(1)</sup>

1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

Figure 52. I<sup>2</sup>S slave timing diagram (Philips protocol)<sup>(1)</sup>

1. Measurement points are done at CMOS levels:  $0.3 \times V_{DD}$  and  $0.7 \times V_{DD}$ .
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 53. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>

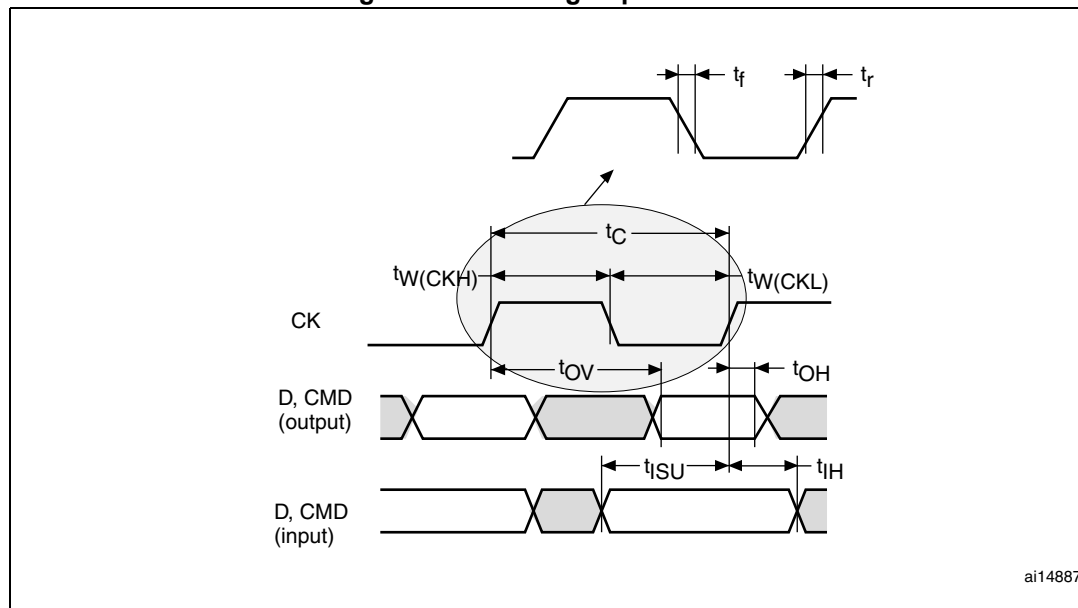
1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### SD/SDIO MMC card host interface (SDIO) characteristics

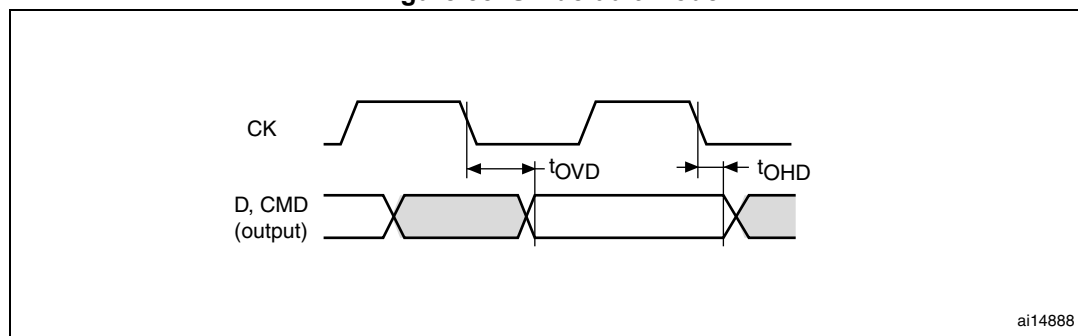
Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 10](#).

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

**Figure 54. SDIO high-speed mode**



**Figure 55. SD default mode**



**Table 55. SD / MMC characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{PP}$	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
$t_W(CKL)$	Clock low time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	32	-	ns
$t_W(CKH)$	Clock high time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	30	-	
$t_r$	Clock rise time	$C_L \leq 30$ pF	-	4	
$t_f$	Clock fall time	$C_L \leq 30$ pF	-	5	

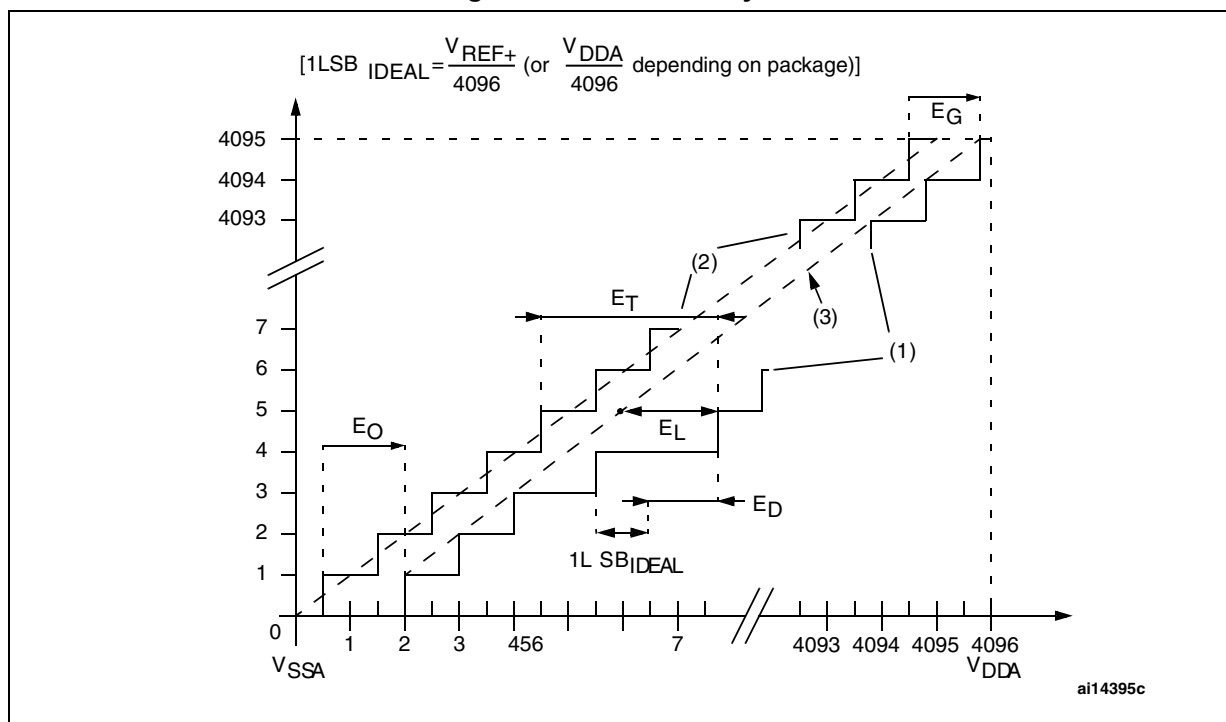


Table 62. ADC accuracy<sup>(1) (2)(3)</sup>

Symbol	Parameter	Test conditions	Typ	Max <sup>(4)</sup>	Unit
ET	Total unadjusted error	f <sub>PCLK2</sub> = 56 MHz, f <sub>ADC</sub> = 14 MHz, R <sub>AIN</sub> < 10 kΩ, V <sub>DDA</sub> = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V<sub>DD</sub>, frequency, V<sub>REF</sub> and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.  
Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and ΣI<sub>INJ(PIN)</sub> in [Section 5.3.14](#) does not affect the ADC accuracy.
4. Guaranteed by characterization results.

Figure 57. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.  
EO = Offset Error: deviation between the first actual transition and the first ideal one.  
EG = Gain Error: deviation between the last ideal transition and the last actual one.  
ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.  
EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

## 5.3.20 DAC electrical specifications

Table 63. DAC characteristics

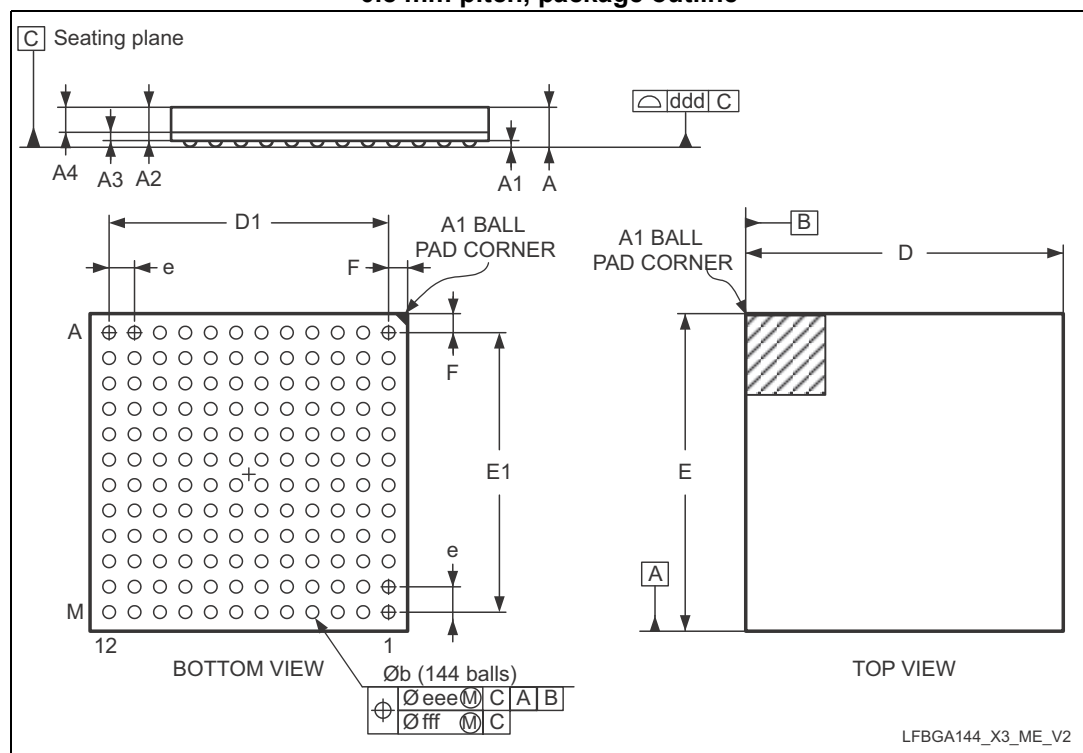
Symbol	Parameter	Min	Typ	Max	Unit	Comments
$V_{DDA}$	Analog supply voltage	2.4	-	3.6	V	-
$V_{REF+}$	Reference supply voltage	2.4	-	3.6	V	$V_{REF+}$ must always be below $V_{DDA}$
$V_{SSA}$	Ground	0	-	0	V	-
$R_{LOAD}^{(1)}$	Resistive load with buffer ON	5	-	-	k $\Omega$	-
$R_O^{(2)}$	Impedance output with buffer OFF	-	-	15	k $\Omega$	When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 M $\Omega$
$C_{LOAD}^{(1)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
$DAC\_OUT_{min}^{(1)}$	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x155) and (0xEAB) at $V_{REF+} = 2.4$ V
$DAC\_OUT_{max}^{(1)}$	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	
$DAC\_OUT_{min}^{(1)}$	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
$DAC\_OUT_{max}^{(1)}$	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{REF+} - 1LSB$	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	$\mu$ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
$I_{DDA}$	DAC DC current consumption in quiescent mode <sup>(3)</sup>	-	-	380	$\mu$ A	With no load, middle code (0x800) on the inputs
		-	-	480	$\mu$ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
$DNL^{(4)}$	Differential non linearity Difference between two consecutive code-1LSB)	-	-	$\pm 0.5$	LSB	Given for the DAC in 10-bit configuration
		-	-	$\pm 2$	LSB	Given for the DAC in 12-bit configuration
$INL^{(3)}$	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	$\pm 1$	LSB	Given for the DAC in 10-bit configuration
		-	-	$\pm 4$	LSB	Given for the DAC in 12-bit configuration

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 6.1 LFBGA144 package information

**Figure 62. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline**



1. Drawing is not to scale.

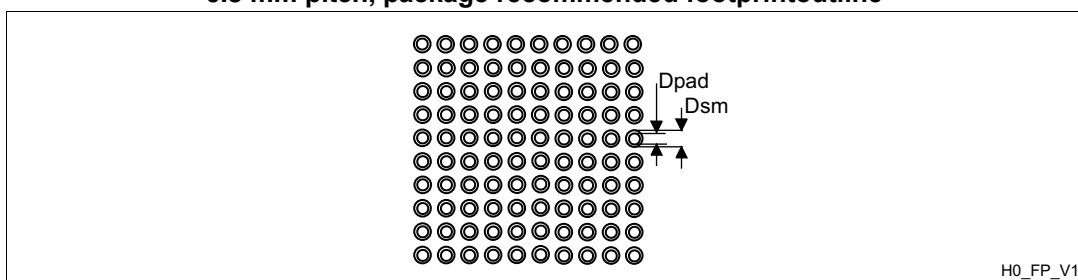
**Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Typ	Min	Max
A <sup>(2)</sup>	-	-	1.700	-	-	0.0669
A1	0.250	0.300	0.350	0.098	0.0118	0.0138
A2	0.810	0.910	1.010	0.0319	0.0358	0.0398
A3	0.225	0.26	0.295	0.0089	0.0102	0.0116
A4	0.585	0.650	0.715	0.0230	0.0256	0.0281

**Table 67. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 66. LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprintoutline****Table 68. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved