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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (4.47×4.4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rcy6tr

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.3.22 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.
The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.24 Universal serial bus (USB)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.3.25 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

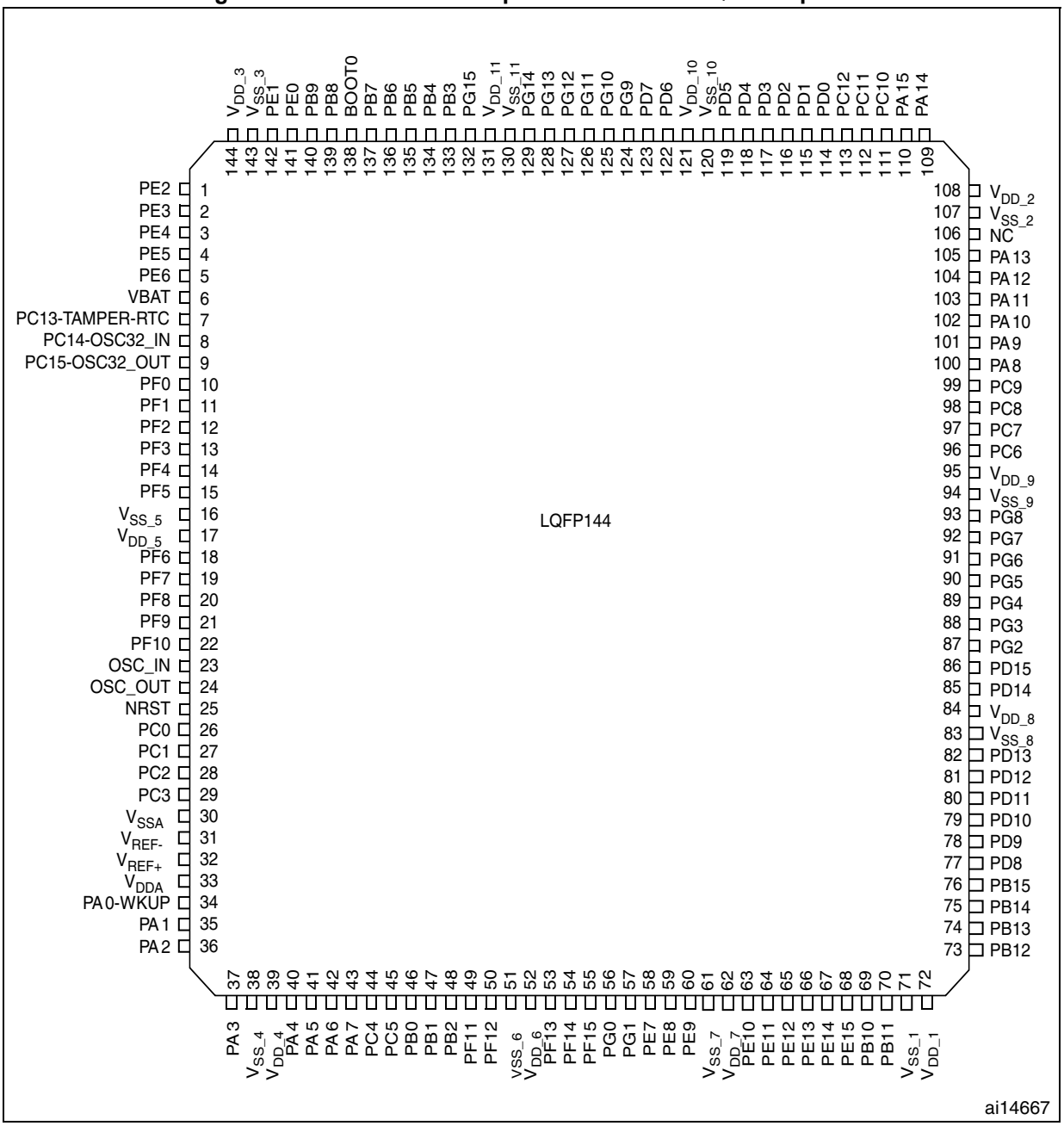
2.3.26 ADC (analog to digital converter)

Three 12-bit analog-to-digital converters are embedded into STM32F103xC, STM32F103xD and STM32F103xE performance line devices and each ADC shares up to 21 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

Figure 5. STM32F103xC/D/E performance line LQFP144 pinout



1. The above figure shows the package top view.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
C9	D7	-	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	B6	-	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	-	-	120	V_{SS_10}	S	-	V_{SS_10}	-	-
F7	-	-	-	-	121	V_{DD_10}	S	-	V_{DD_10}	-	-
A8	C6	-	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
A9	D6	-	-	88	123	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK
E8	-	-	-	-	124	PG9	I/O	FT	PG9	FSMC_NE2/FSMC_NCE3	-
D8	-	-	-	-	125	PG10	I/O	FT	PG10	FSMC_NCE4_1/ FSMC_NE3	-
C8	-	-	-	-	126	PG11	I/O	FT	PG11	FSMC_NCE4_2	-
B8	-	-	-	-	127	PG12	I/O	FT	PG12	FSMC_NE4	-
D7	-	-	-	-	128	PG13	I/O	FT	PG13	FSMC_A24	-
C7	-	-	-	-	129	PG14	I/O	FT	PG14	FSMC_A25	-
E6	-	-	-	-	130	V_{SS_11}	S	-	V_{SS_11}	-	-
F6	-	-	-	-	131	V_{DD_11}	S	-	V_{DD_11}	-	-
B7	-	-	-	-	132	PG15	I/O	FT	PG15	-	-
A7	A7	A4	55	89	133	PB3	I/O	FT	JTDO	SPI3_SCK / I2S3_CK/	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
A6	A6	B4	56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
B6	C5	A5	57	91	135	PB5	I/O	-	PB5	I2C1_SMBA/ SPI3_MOSI I2S3_SD	TIM3_CH2 / SPI1_MOSI
C6	B5	B5	58	92	136	PB6	I/O	FT	PB6	I2C1_SCL(9)/ TIM4_CH1(9)	USART1_TX
D6	A5	C5	59	93	137	PB7	I/O	FT	PB7	I2C1_SDA(9) / FSMC_NADV / TIM4_CH2(9)	USART1_RX
D5	D5	A6	60	94	138	BOOT0	I	-	BOOT0	-	-
C5	B4	D5	61	95	139	PB8	I/O	FT	PB8	TIM4_CH3(9)/SDIO_D4	I2C1_SCL/ CAN_RX
B5	A4	B6	62	96	140	PB9	I/O	FT	PB9	TIM4_CH4(9)/SDIO_D5	I2C1_SDA / CAN_TX

Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	45	46	mA
			48 MHz	31	32	
			36 MHz	24	25	
			24 MHz	17	17.5	
			16 MHz	12.5	13	
			8 MHz	8	8	
		External clock(2), all peripherals disabled	72 MHz	8.5	9	
			48 MHz	7	7.5	
			36 MHz	6	6.5	
			24 MHz	5	5.5	
			16 MHz	4.5	5	
			8 MHz	4	4	

1. Guaranteed by characterization results at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 17. Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values

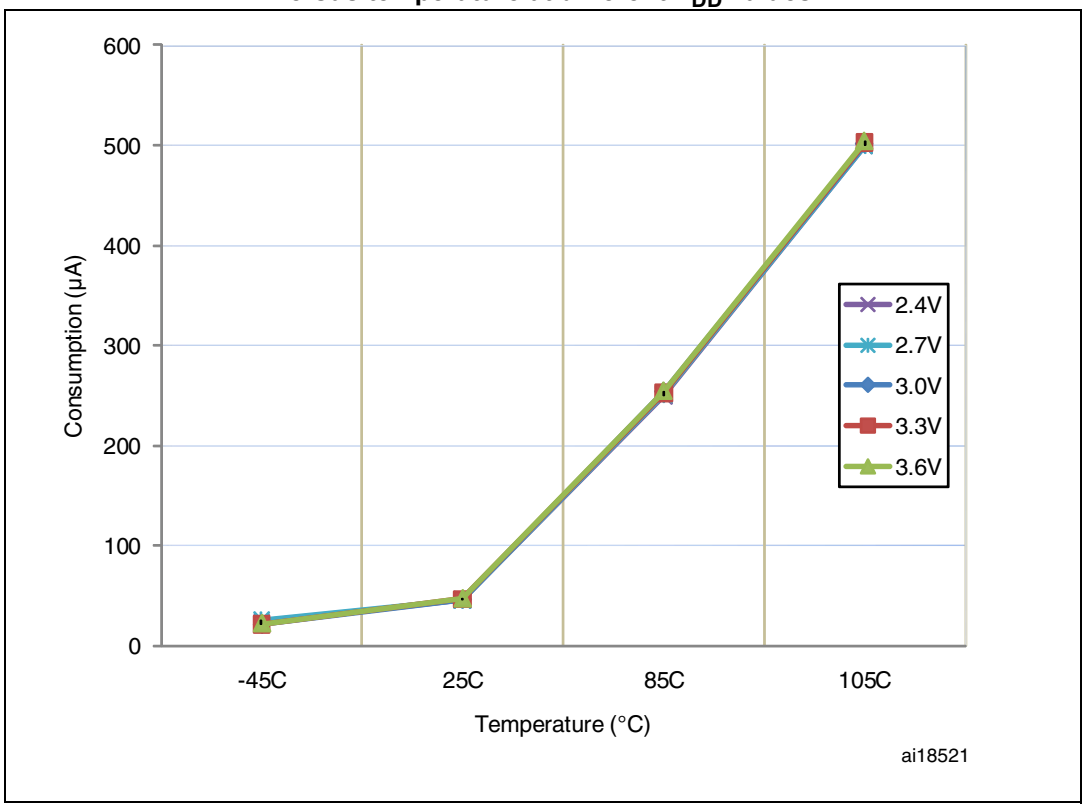


Figure 18. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

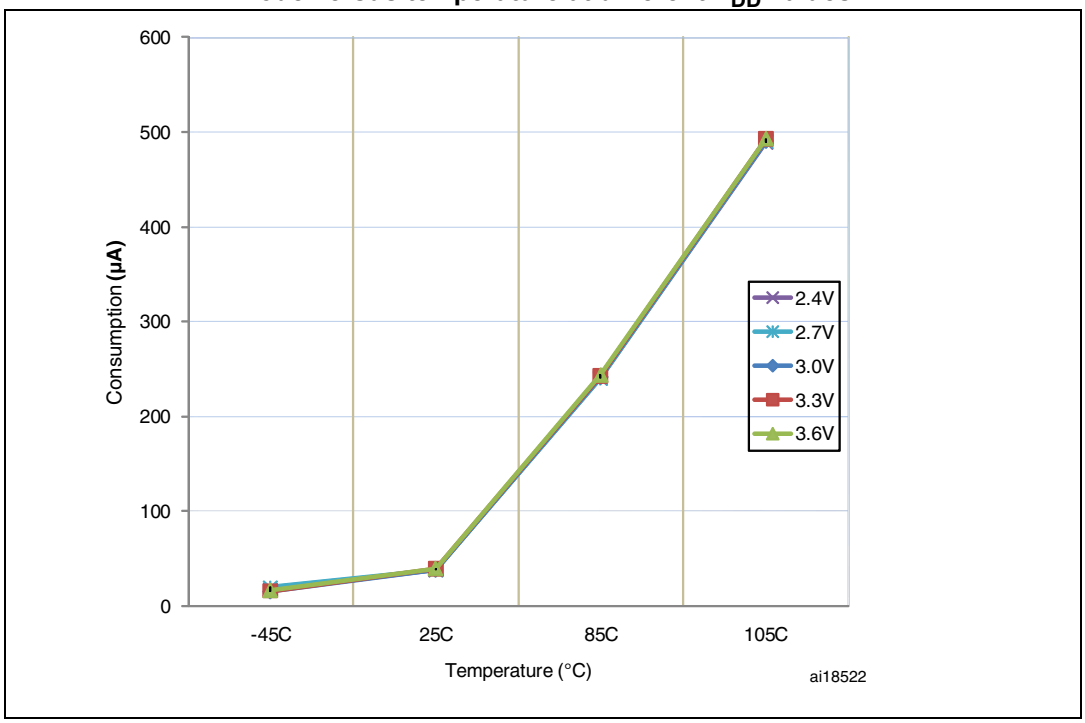


Table 20. Peripheral current consumption (continued)

Peripheral		Current consumption	Unit
APB2 (up to 72 MHz)	APB2-Bridge	4,17	µA/MHz
	GPIOA	8,47	
	GPIOB	8,47	
	GPIOC	6,53	
	GPIOD	8,47	
	GPIOE	6,53	
	GPIOF	6,53	
	GPIOG	6,11	
	SPI1	4,72	
	USART1	12,50	
	TIM1	22,92	
	TIM8	22,92	
	ADC1(4)	17,32	
	ADC2(4)	15,18	
	ADC3(4)	14,82	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1 or DMA2).
2. When the I2S is enabled, a current consumption equal to 0.02 mA must be added.
3. When DAC_OU1 or DAC_OUT2 is enabled, a current consumption equal to 0.36 mA must be added.
4. Specific conditions for measuring ADC current consumption: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADCx_CR2 register is set to 1, a current consumption of analog part equal to 0.54 mA must be added for each ADC.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 21. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

The characteristics given in *Table 22* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 22. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

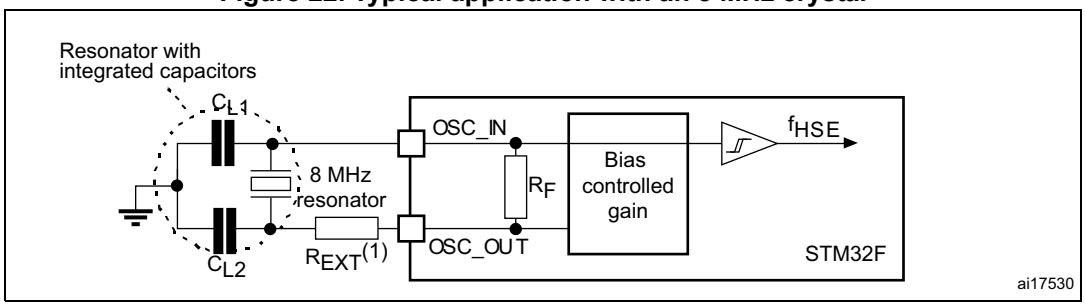
Table 23. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 22*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Table 39. Switching characteristics for PC Card/CF read and write cycles(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8t_{HCLK}$ + 3	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5t_{HCLK}$ +1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5t_{HCLK}$+3ns	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5t_{HCLK}$ – 5	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	$5t_{HCLK}$ + 2.5	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5t_{HCLK}$ – 5	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8t_{HCLK}$ + 2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Table 44. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*

Table 45. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 46* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 46*.
3. Guaranteed by design.

5.3.17 Communications interfaces

I²C interface characteristics

The STM32F103xC, STM32F103xD and STM32F103xESTM32F103xF and STM32F103xG performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 51*. Refer also to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 51. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	0	50(4)	0	50(4)	µs

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve the fast mode I²C frequencies and it must be a multiple of 10 MHz in order to reach the I2C fast mode maximum clock speed of 400 kHz.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

I^2S - SPI characteristics

Unless otherwise specified, the parameters given in *Table 53* for SPI or in *Table 54* for I^2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 53. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

1. Guaranteed by characterization results.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 59*.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 60. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

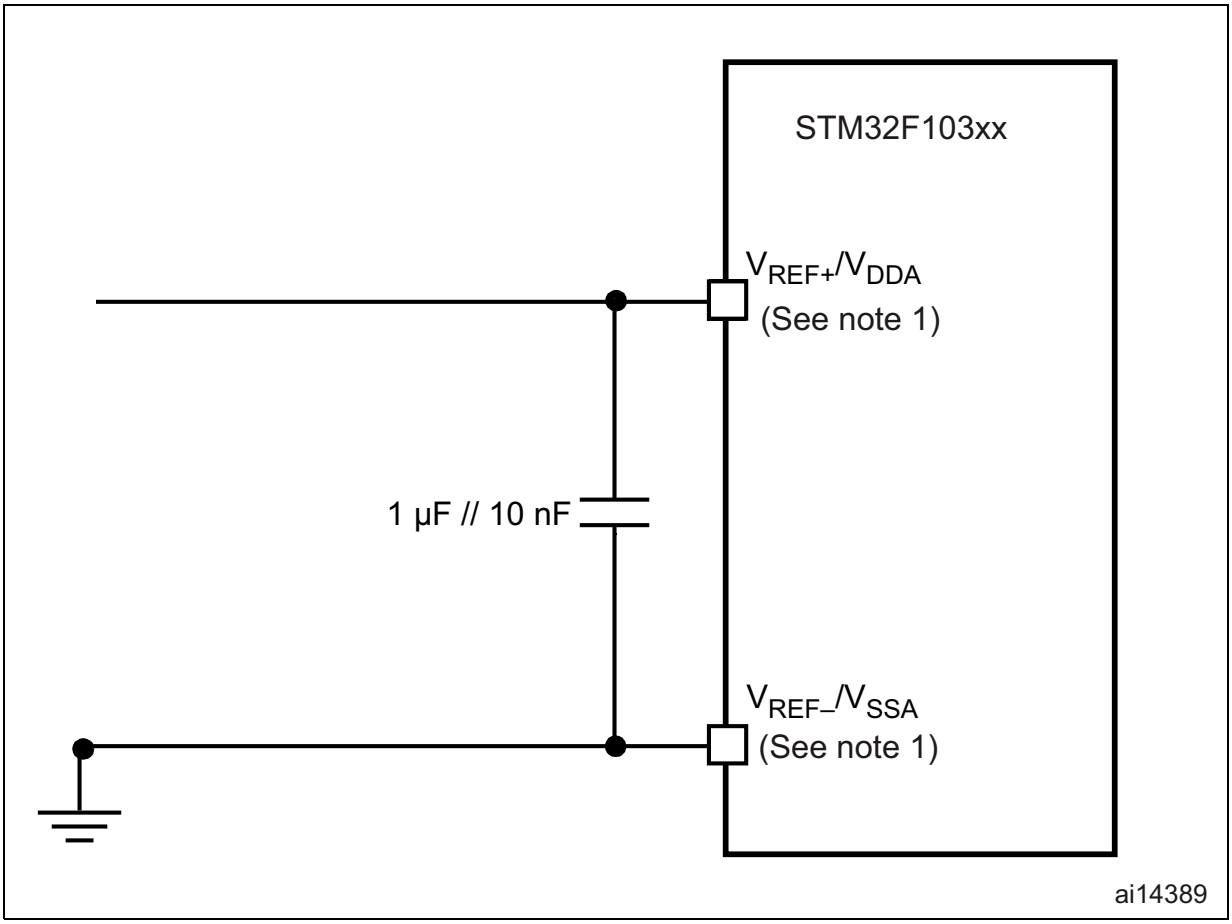
1. Guaranteed by design.

Table 61. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration V_{REF+} = V_{DDA}	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



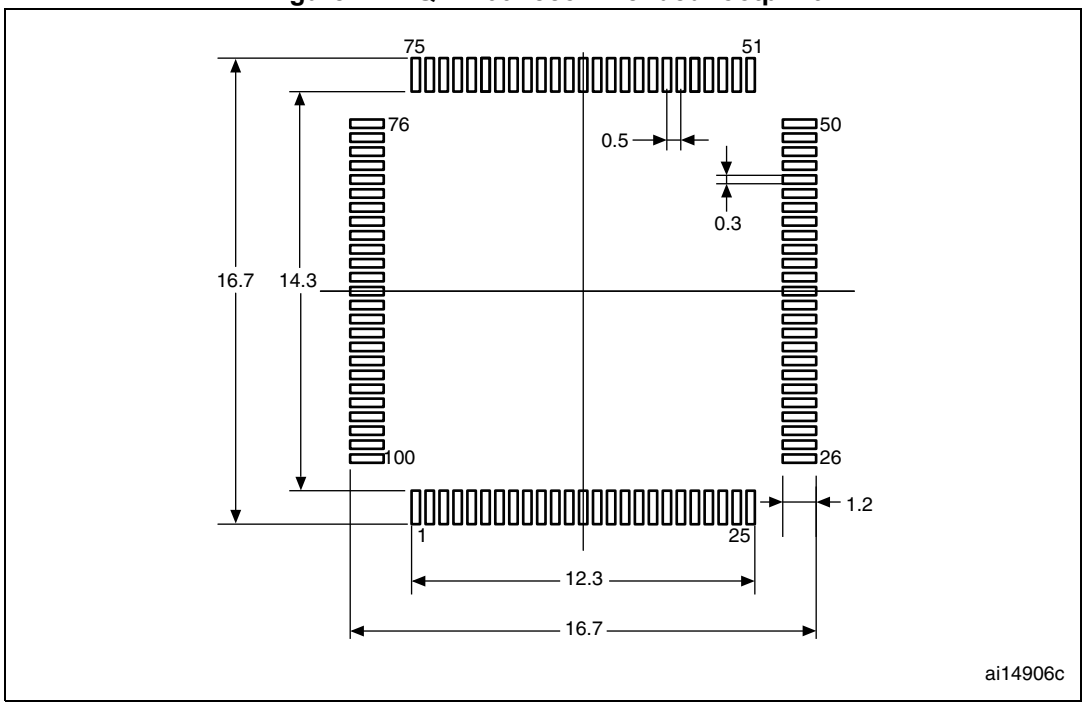
1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

Table 72. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 74. LQFP100 recommended footprint

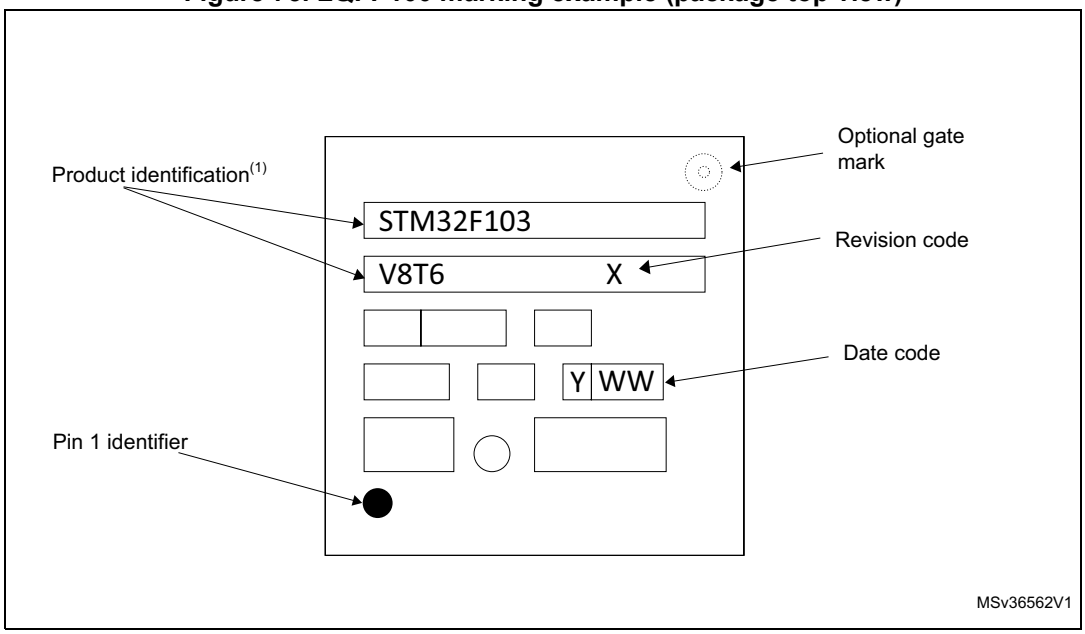


1. Dimensions are in millimeters.

Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

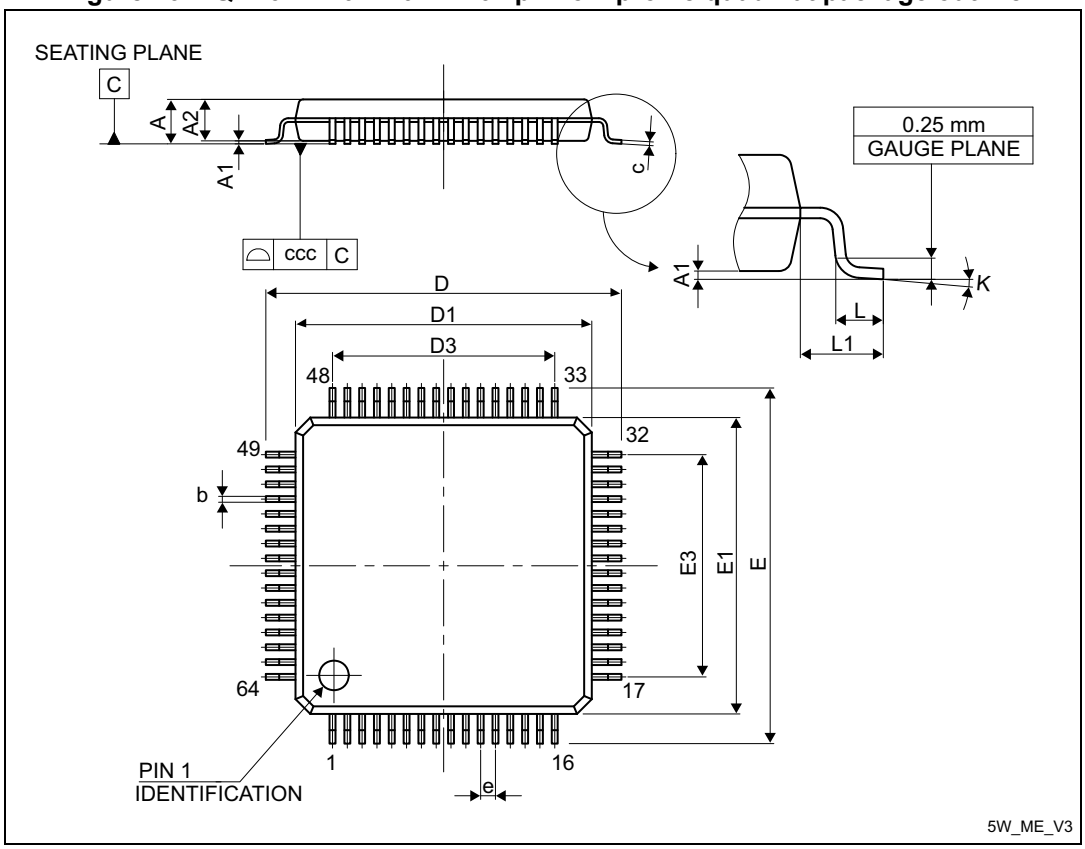
Figure 75. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.6 LQFP64 package information

Figure 76. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 73. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-