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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rdt6

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.17 Timers and watchdogs

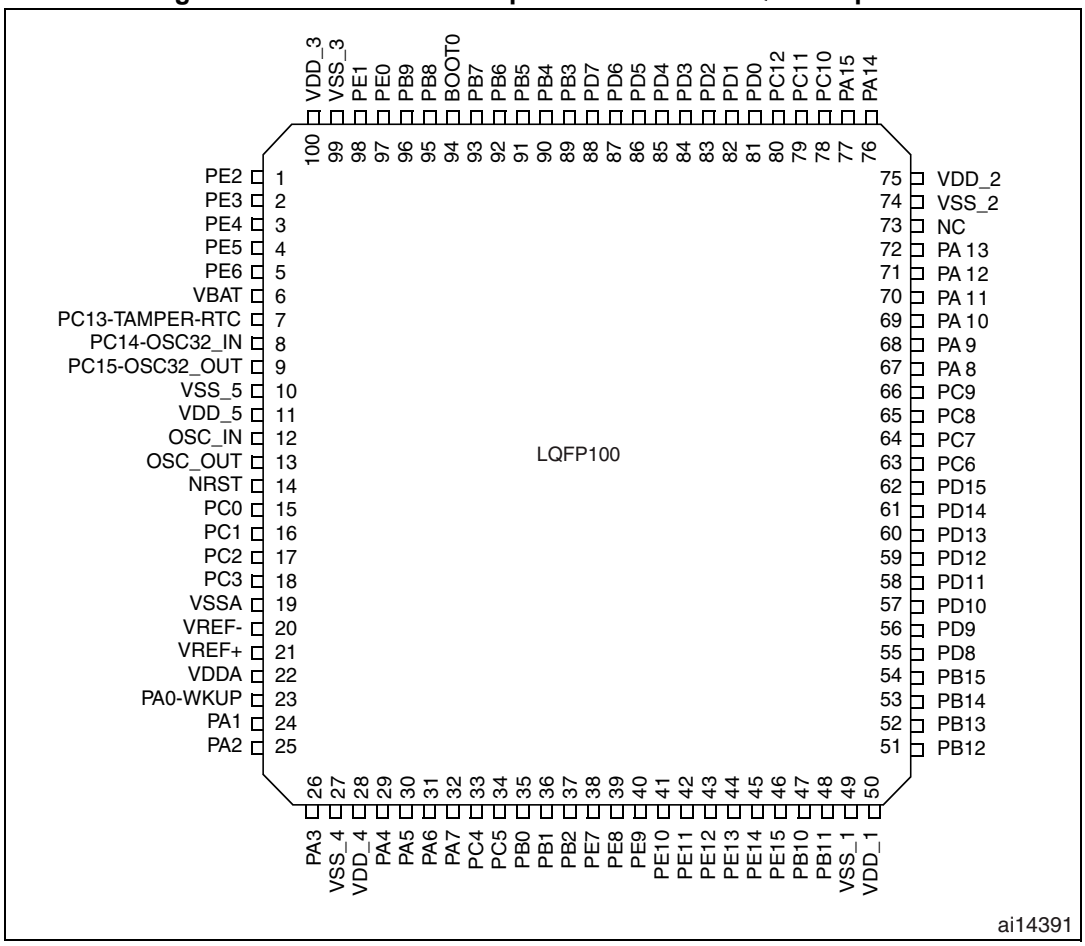
The high-density STM32F103xC/D/E performance line devices include up to two advanced-control timers, up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. High-density timer feature comparison

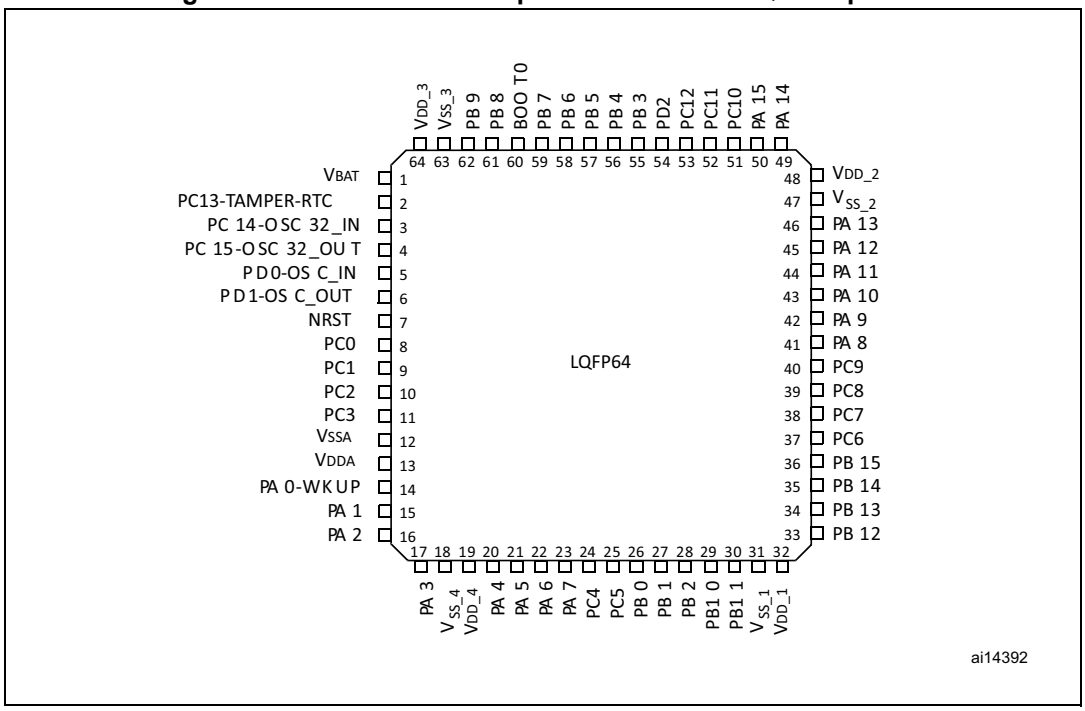
Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Figure 6. STM32F103xC/D/E performance line LQFP100 pinout



1. The above figure shows the package top view.

Figure 7. STM32F103xC/D/E performance line LQFP64 pinout



1. The above figure shows the package top view.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	-
E5	E5	A7	63	99	143	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	F5	A8	64	100	144	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. In the WCLSP64 package, the PC3 I/O pin is not bonded and it must be configured by software to output mode (Push-pull) and writing 0 to the data register in order to avoid an extra consumption during low-power modes.
8. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
10. For the WCLSP64/LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
11. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100 BGA100(1)
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18	-	Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

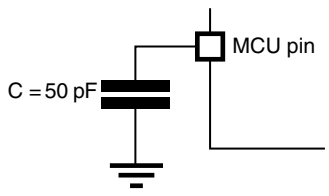


Figure 11. Pin input voltage

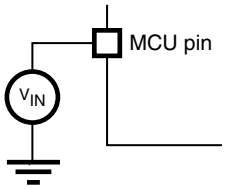


Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	45	46	mA
			48 MHz	31	32	
			36 MHz	24	25	
			24 MHz	17	17.5	
			16 MHz	12.5	13	
			8 MHz	8	8	
		External clock(2), all peripherals disabled	72 MHz	8.5	9	
			48 MHz	7	7.5	
			36 MHz	6	6.5	
			24 MHz	5	5.5	
			16 MHz	4.5	5	
			8 MHz	4	4	

1. Guaranteed by characterization results at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

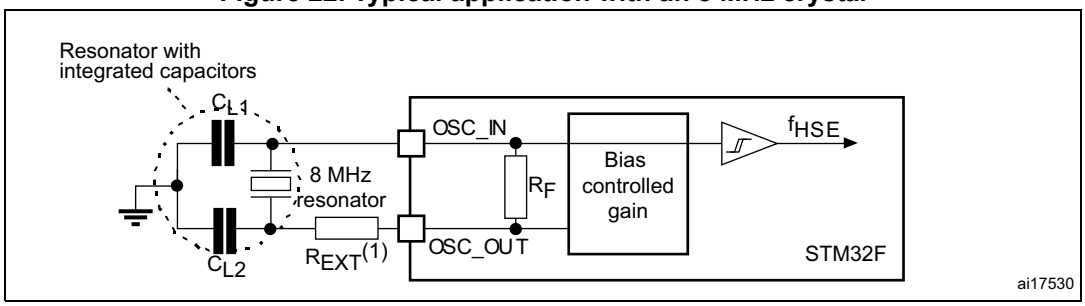
Table 23. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 22*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Table 33. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms

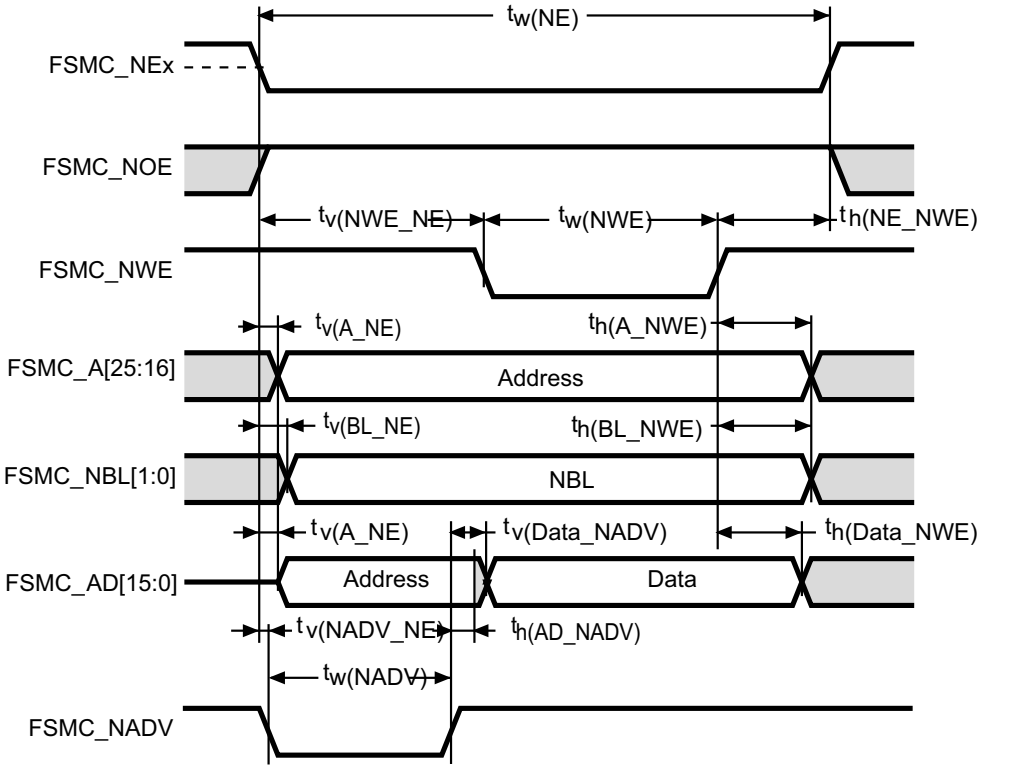


Table 34. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

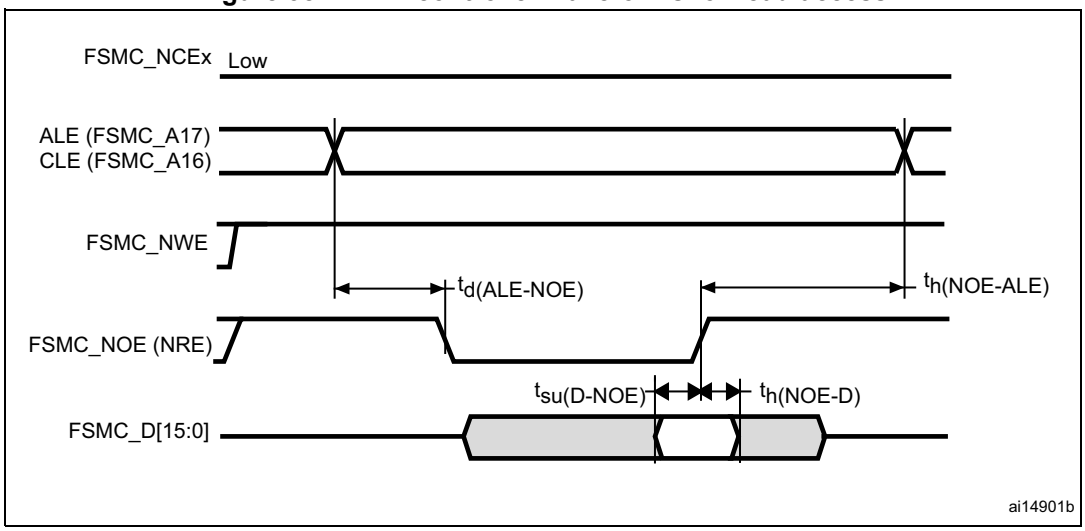
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1$	$5t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$2t_{HCLK}$	$2t_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2t_{HCLK} - 1$	$2t_{HCLK} + 2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$t_{HCLK} - 1$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	ns

NAND controller waveforms and timings

Figure 38 through *Figure 41* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 38. NAND controller waveforms for read access



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 46* and *Table 48*, respectively.

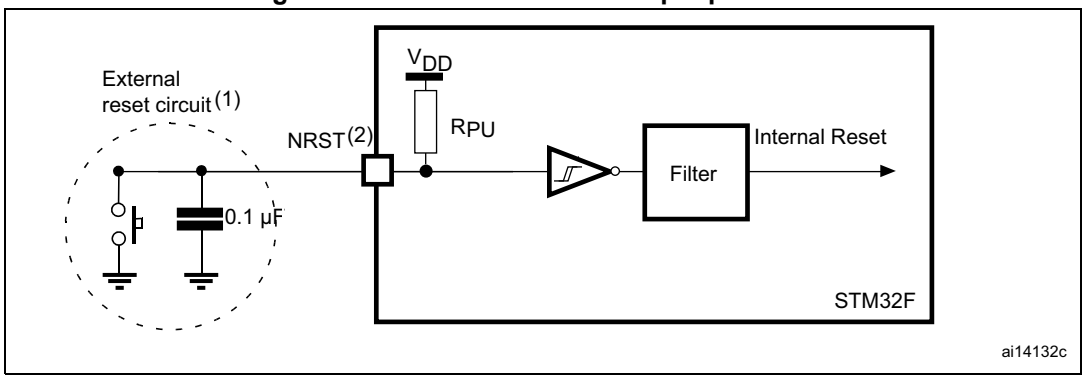
Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 46*.
3. Guaranteed by design.

Figure 47. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 49*. Otherwise the reset will not be taken into account by the device.

5.3.16 TIM timer characteristics

The parameters given in *Table 50* are guaranteed by design.

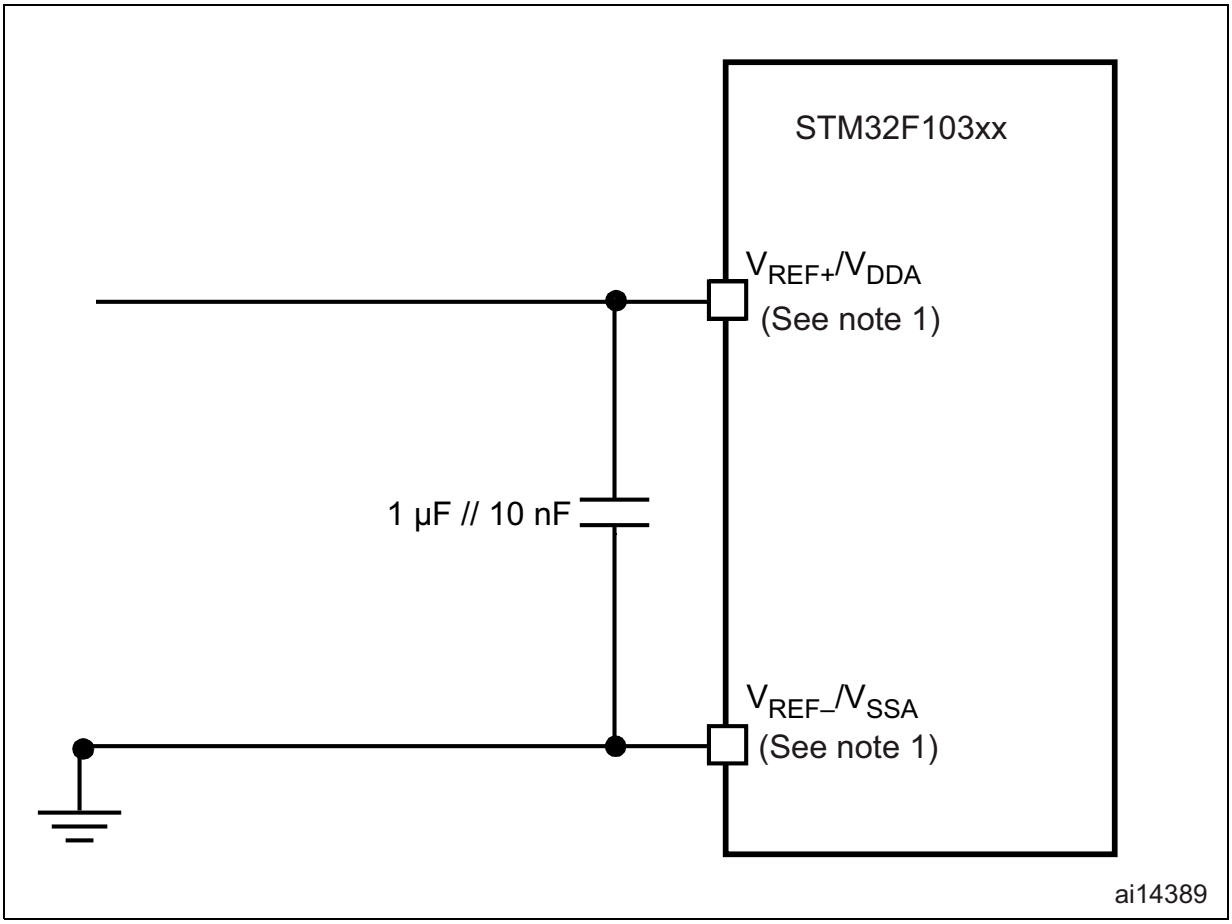
Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 50. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

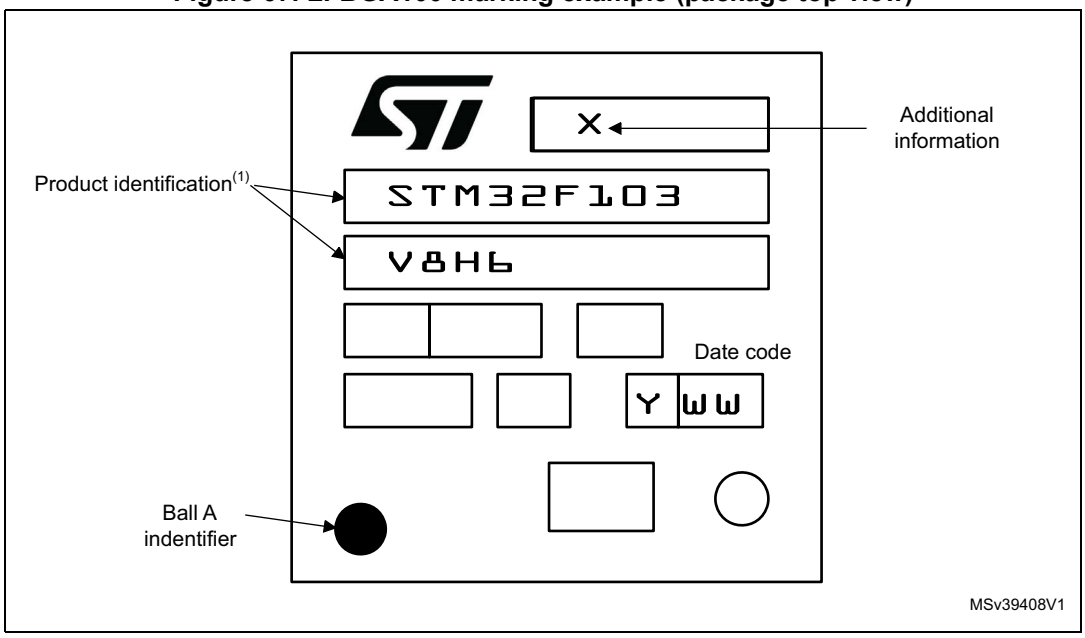


1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

Device marking for LFBGA100 package

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 67. LFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 69. WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
e1	-	3.500	-	-	0.1378	-
F	-	0.447	-	-	0.0176	-
G	-	0.483	-	-	0.0190	-
D	4.446	4.466	4.486	0.1750	0.1758	0.1766
E	4.375	4.395	4.415	0.1722	0.1730	0.1738
H	-	0.250	-	-	0.0098	-
L	-	0.200	-	-	0.0079	-
eee	-	0.05	-	-	0.0020	-
aaa	-	0.10	-	-	0.0039	-
Number of balls	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum ball diameter parallel to primary datum Z.

Figure 69. WLCSP64 - 64-ball, 4.4757 x 4.4049 mm, 0.5 mm pitch wafer level chip scale package recommended footprint

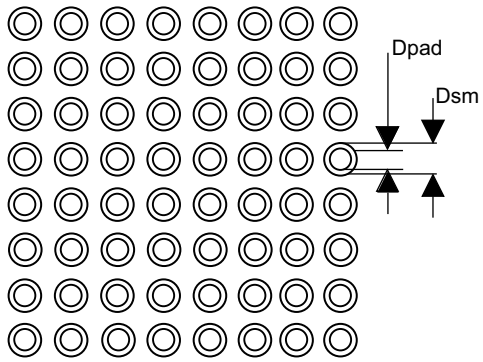


Table 70. WLCSP64 recommended PCB design rules (0.5 mm pitch)

Dimension	Recommended values
Pitch	0.5
Dpad	250 µm
Dsm	300 µm
Stencil Opening	320 µm
Stencil Thickness	Between 100 µm to 125 µm
Pad trace width	100 µm
Ball Diameter	320 µm

Table 76.Document revision history

Date	Revision	Changes
12-Dec-2008	4	Timers specified *on page 1* (motor control capability mentioned). *Section 2.2: Full compatibility throughout the family* updated. *Table 6: High-density timer feature comparison* added. *General-purpose timers (TIMx)* and *Advanced-control timers (TIM1 and TIM8) on page 27* updated. *Figure 1: STM32F103xF, STM32F103xD and STM32F103xGSTM32F103xF and STM32F103xG performance line block diagram* modified. *Note 10* added, main function after reset and *Note 5 on page 44* updated in *Table 8: High-density STM32F103xx pin definitions*. *Note 2* modified below *Table 11: Voltage characteristics on page 58*, $\|DV_{DDx}\|$ min and $\|DV_{DDx}\|$ min removed. *Note 2* and P_D values for LQFP144 and LFBGA144 packages added to *Table 14: General operating conditions on page 59*. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 62*. Max values at T_A = 85 °C and T_A = 105 °C updated in *Table 21: Typical and maximum current consumptions in Stop and Standby modes on page 68*. *Section 5.3.10: FSMC characteristics on page 87* updated. Data added to *Table 50: EMI characteristics on page 111*. I_{VREF} added to *Table 67: ADC characteristics on page 130*. *Table 81: Package thermal characteristics on page 146* updated. Small text changes.

Table 76.Document revision history

Date	Revision	Changes
21-Jul-2009	6	*Figure 1: STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram* updated. *Note 5* updated and *Note 4* added in *Table 5: High-density STM32F103xC/D/E pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 13: Embedded internal reference voltage*. *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM* modified. f_{HSE_ext} min modified in *Table 21: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 23: HSE 4-16 MHz oscillator characteristics* and *Table 24: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 29: Synchronous multiplexed PSRAM write timings*. *Table 25: HSI oscillator characteristics* modified. Conditions removed from *Table 27: Low-power mode wakeup timings*. Jitter added to *Table 28: PLL characteristics*. *Figure 47: Recommended NRST pin protection* modified. In *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings*: $t_{h(BL\_NOE)}$ and $t_{h(A\_NOE)}$ modified. In *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*: $t_{h(A\_NWE)}$ and $t_{h(Data\_NWE)}$ modified. In *Table 33: Asynchronous multiplexed PSRAM/NOR read timings*: $t_{h(AD\_NADV)}$ and $t_{h(A\_NOE)}$ modified. In *Table 34: Asynchronous multiplexed PSRAM/NOR write timings*: $t_{h(A\_NWE)}$ modified. In *Table 35: Synchronous multiplexed NOR/PSRAM read timings*: $t_{h(CLKH-NWAITV)}$ modified. In *Table 40: Switching characteristics for NAND Flash read and write cycles*: $t_{h(NOE-D)}$ modified. *Table 53: SPI characteristics* modified. Values added to *Table 54: I2S characteristics* and *Table 55: SD / MMC characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 59: ADC characteristics*. R_{AIN} max values modified in *Table 60: RAIN max for fADC = 14 MHz*. *Table 71: DAC characteristics* modified. *Figure 61: 12-bit buffered /non-buffered DAC* added. *Figure 63: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline* and *Table 75: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data* updated.
24-Sep-2009	7	Number of DACs corrected in *Table 3: STM32F103xx family*. I_{DD_VBAT} updated in *Table 17: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 16: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* added. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.11: EMC characteristics on page 87*. *Table 63: DAC characteristics* modified. Small text changes.