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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (4.47×4.4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rdy6tr

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the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

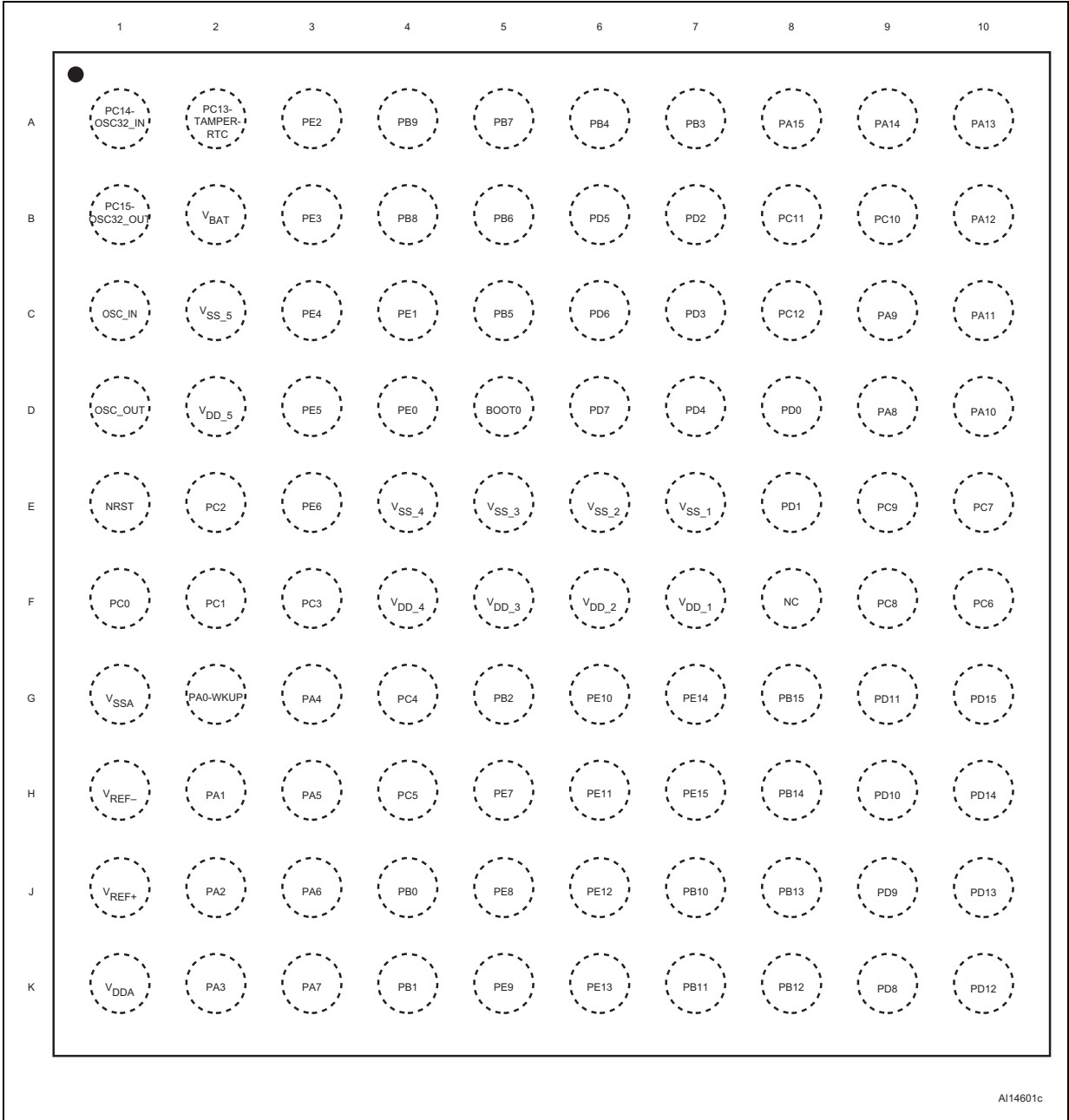
Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.21 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I²S interfaces is/are configured in master

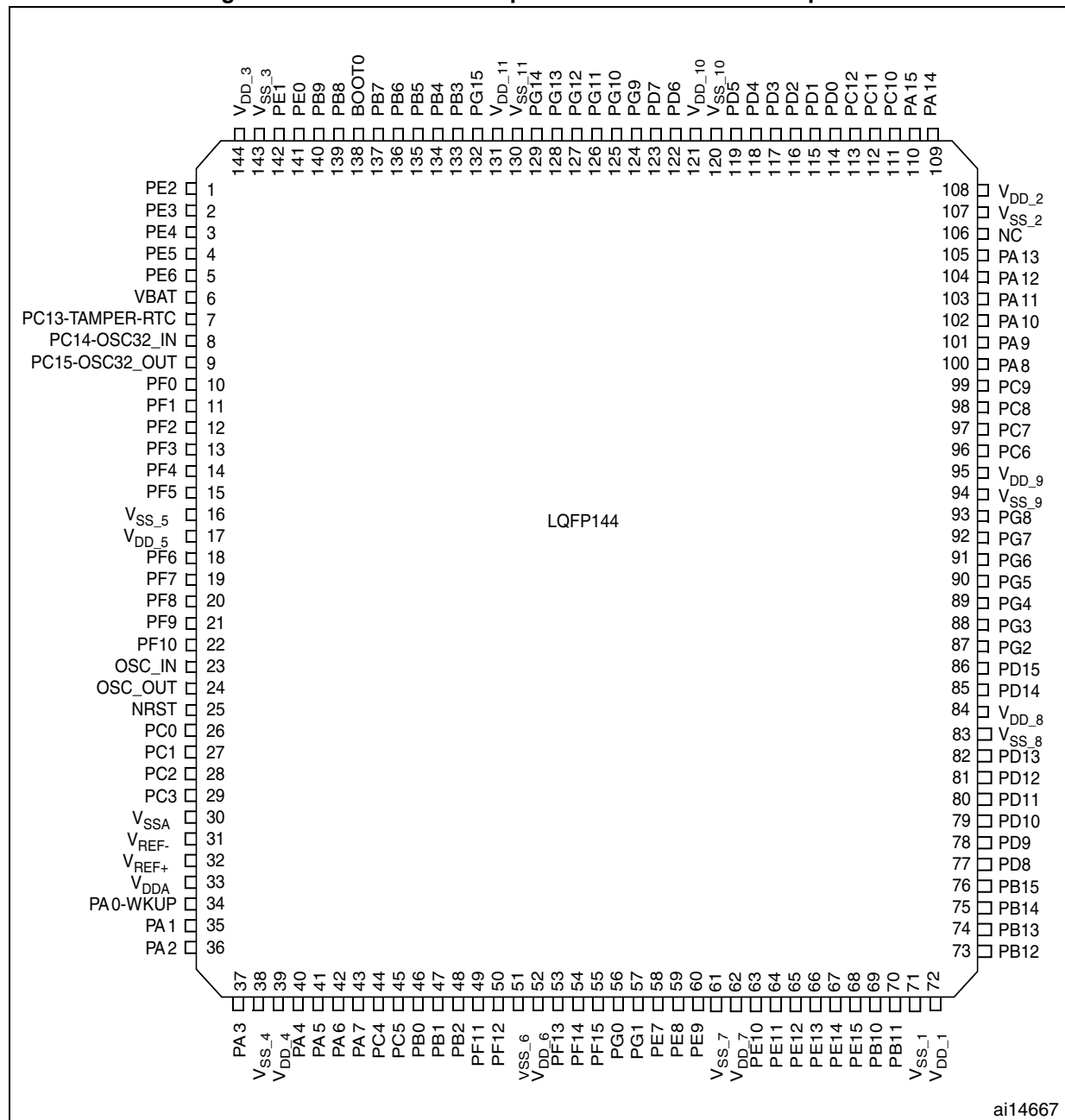
Figure 4. STM32F103xC/D/E performance line BGA100 ballout



AI14601c

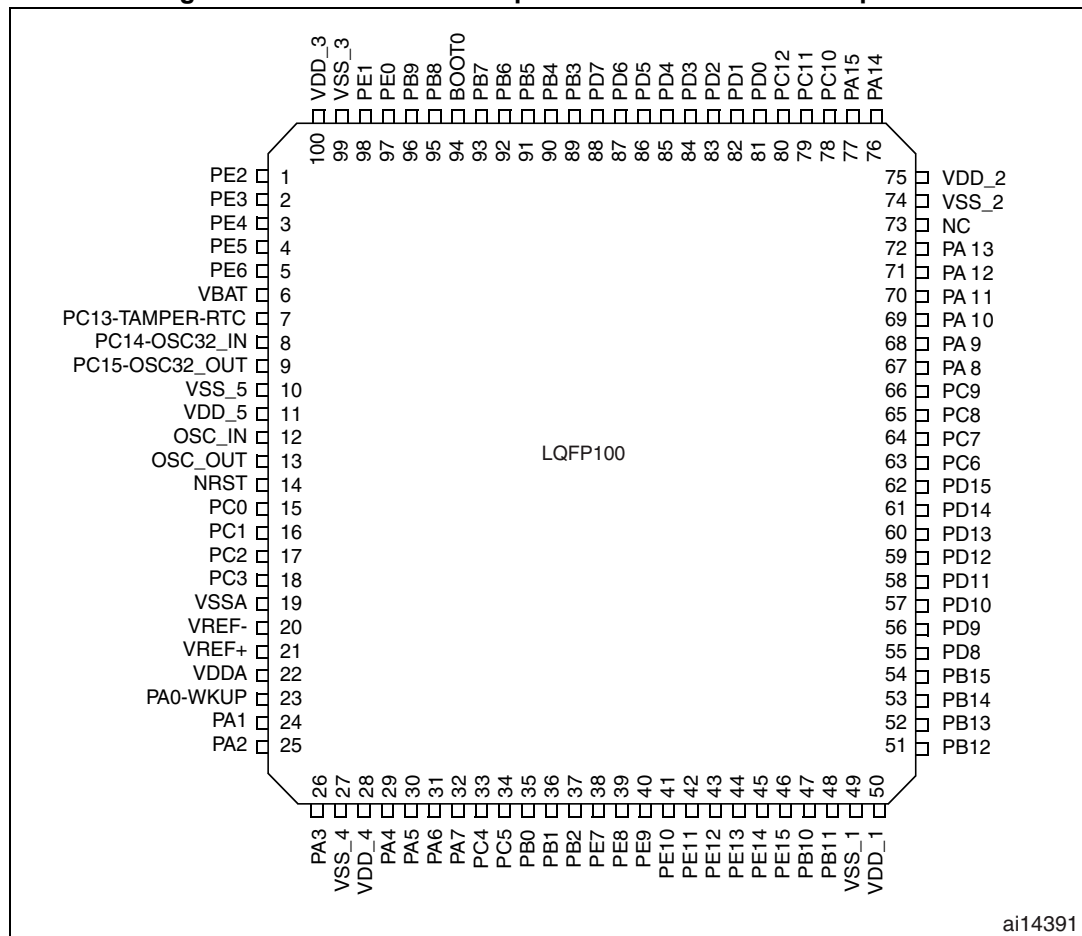
1. The above figure shows the package top view.

Figure 5. STM32F103xC/D/E performance line LQFP144 pinout



1. The above figure shows the package top view.

Figure 6. STM32F103xC/D/E performance line LQFP100 pinout



1. The above figure shows the package top view.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\Sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ (for the $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\Sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 11](#).

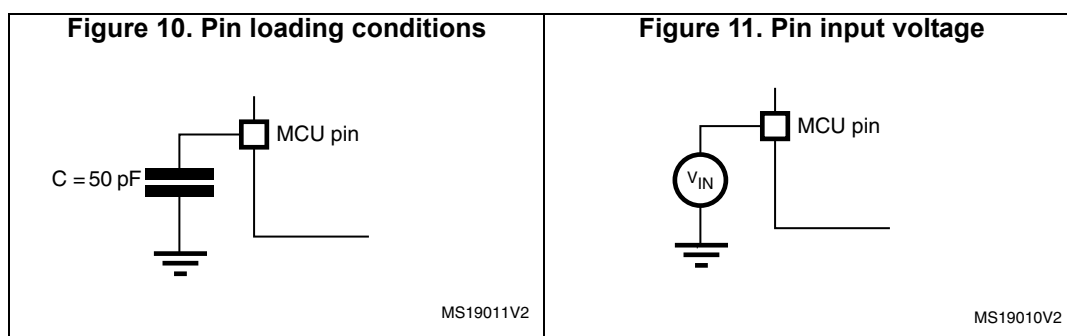
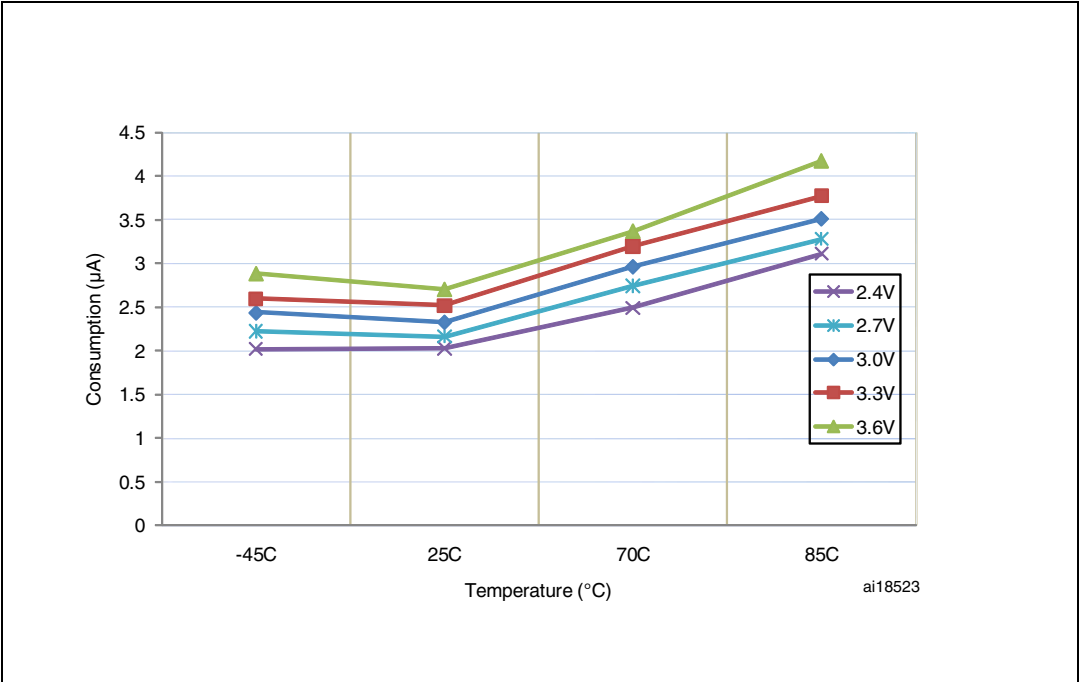


Figure 19. Typical current consumption in Standby mode versus temperature at different V_{DD} values



Synchronous waveforms and timings

Figure 28 through Figure 31 represent synchronous waveforms and Table 36 through Table 38 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 28. Synchronous multiplexed NOR/PSRAM read timings

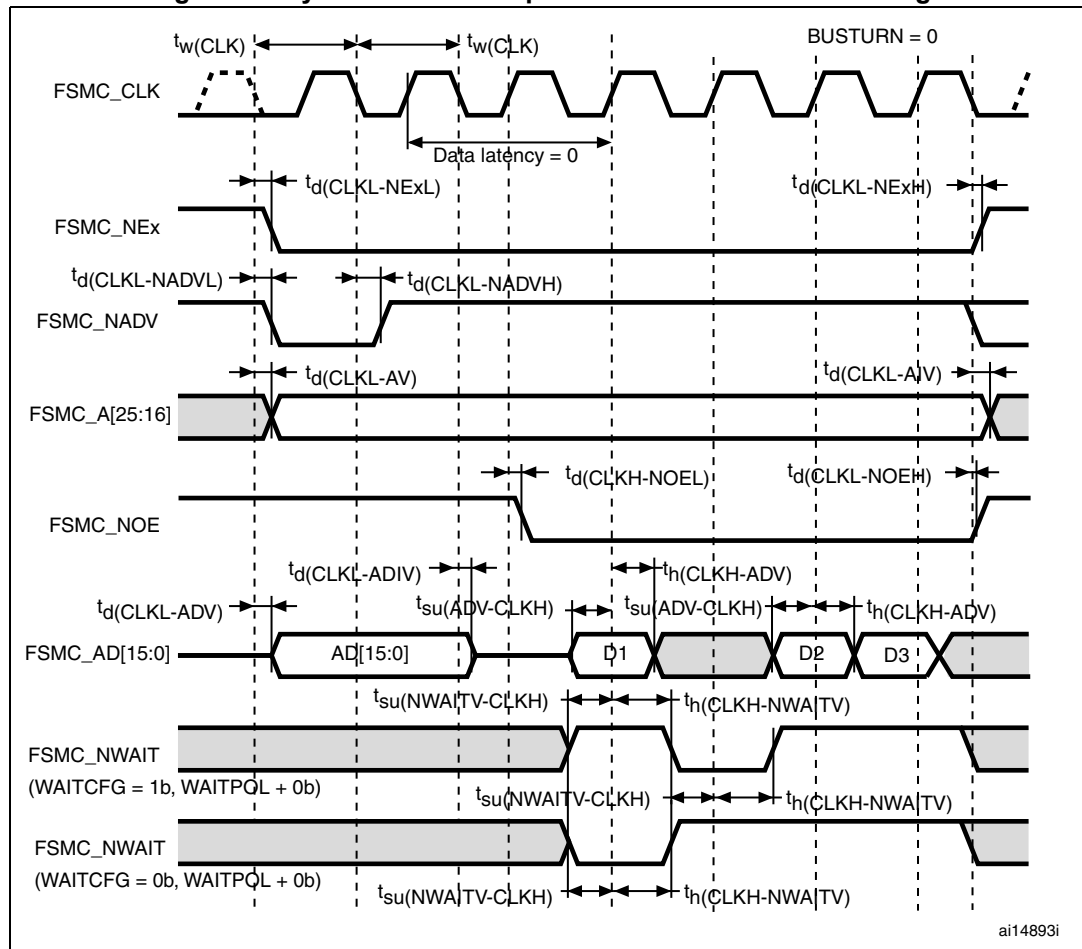


Figure 39. NAND controller waveforms for write access

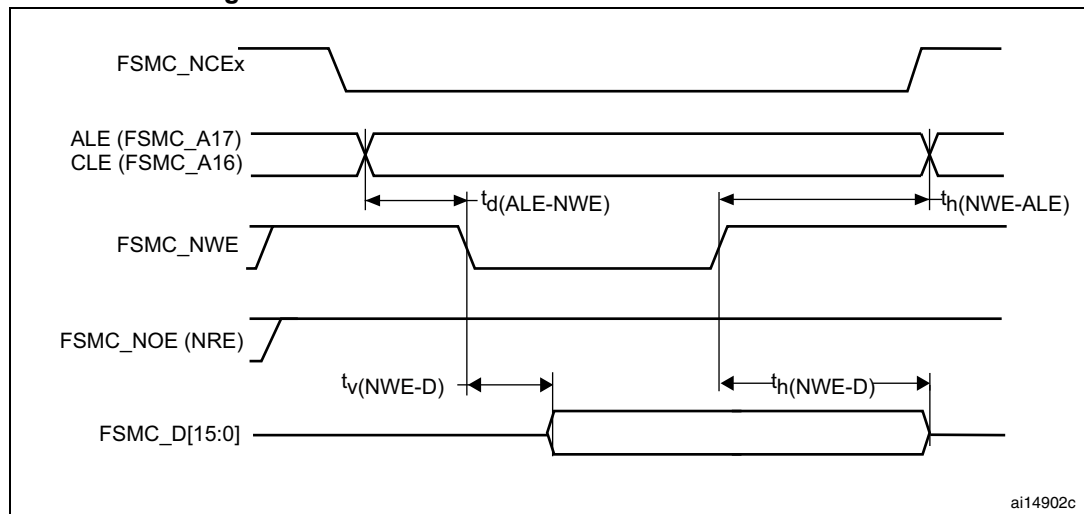
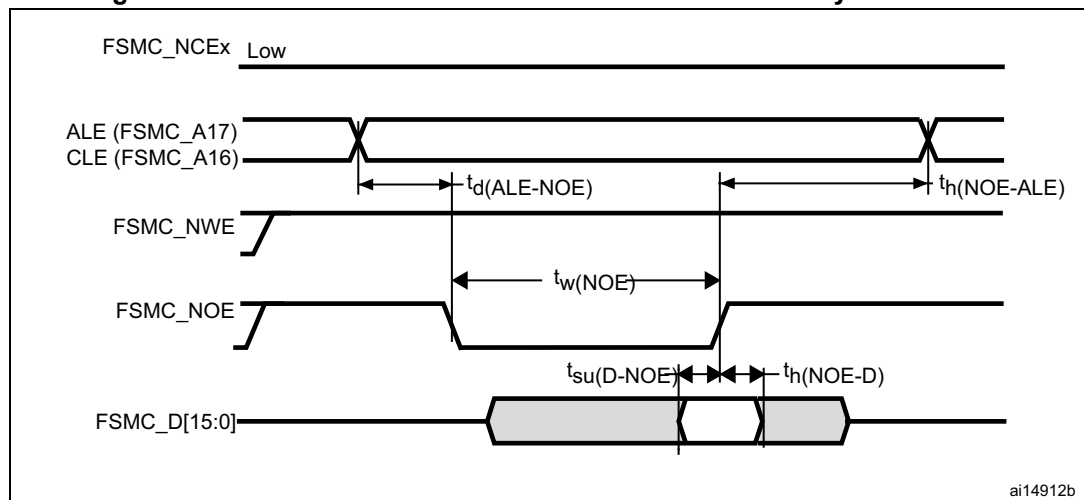


Figure 40. NAND controller waveforms for common memory read access



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 46](#) and [Table 48](#), respectively.

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 48. I/O AC characteristics⁽¹⁾

MODEx[1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	125 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	125 ⁽³⁾	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	10	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	25 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	25 ⁽³⁾	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	50	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	30	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	20	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5 ⁽³⁾	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	12 ⁽³⁾	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	12 ⁽³⁾	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 46](#).
3. Guaranteed by design.

Table 54. I²S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
f_{CK} $1/t_{c(CK)}$	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)		1.522	1.525	MHz
		Slave mode		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I ² S clock rise and fall time	Capacitive load C _L = 50 pF		-	8	ns
$t_{v(WS)}^{(1)}$	WS valid time	Master mode		3	-	
$t_{h(WS)}^{(1)}$	WS hold time	Master mode	I2S2	2	-	
			I2S3	0	-	
$t_{su(WS)}^{(1)}$	WS setup time	Slave mode		4	-	
$t_{h(WS)}^{(1)}$	WS hold time	Slave mode		0	-	
$t_{w(CKH)}^{(1)}$	CK high and low time	Master f _{PCLK} = 16 MHz, audio frequency = 48 kHz		312.5	-	
$t_{w(CKL)}^{(1)}$				345	-	
$t_{su(SD_MR)}^{(1)}$	Data input setup time	Master receiver	I2S2	2	-	
			I2S3	6.5	-	
$t_{su(SD_SR)}^{(1)}$	Data input setup time	Slave receiver		1.5	-	
$t_{h(SD_MR)}^{(1)(2)}$	Data input hold time	Master receiver		0	-	
$t_{h(SD_SR)}^{(1)(2)}$		Slave receiver		0.5	-	
$t_{v(SD_ST)}^{(1)(2)}$	Data output valid time	Slave transmitter (after enable edge)		-	18	
$t_{h(SD_ST)}^{(1)}$	Data output hold time	Slave transmitter (after enable edge)		11	-	
$t_{v(SD_MT)}^{(1)(2)}$	Data output valid time	Master transmitter (after enable edge)		-	3	
$t_{h(SD_MT)}^{(1)}$	Data output hold time	Master transmitter (after enable edge)		0	-	

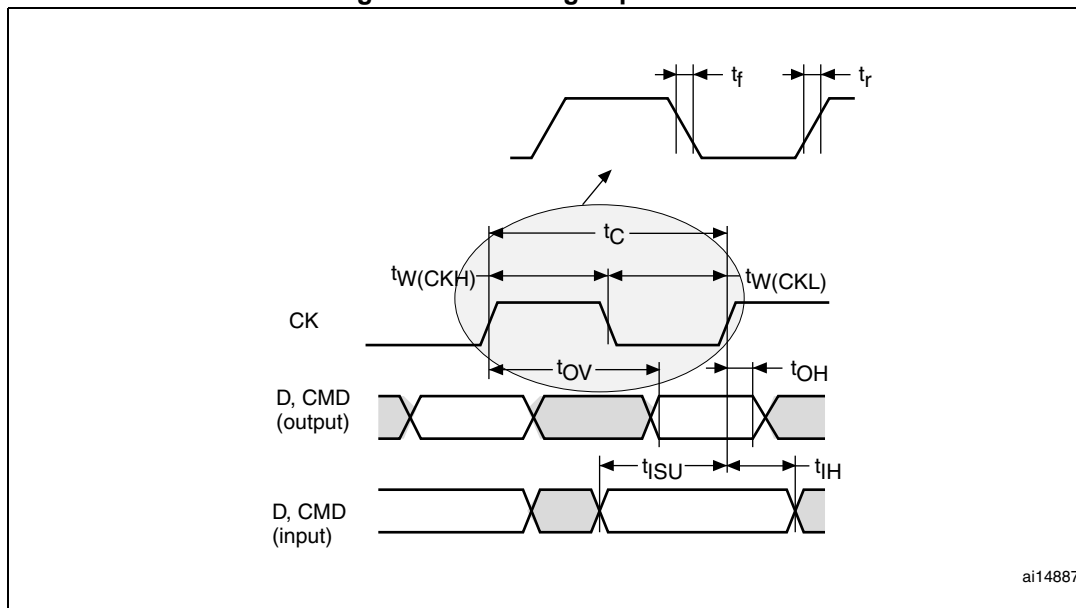
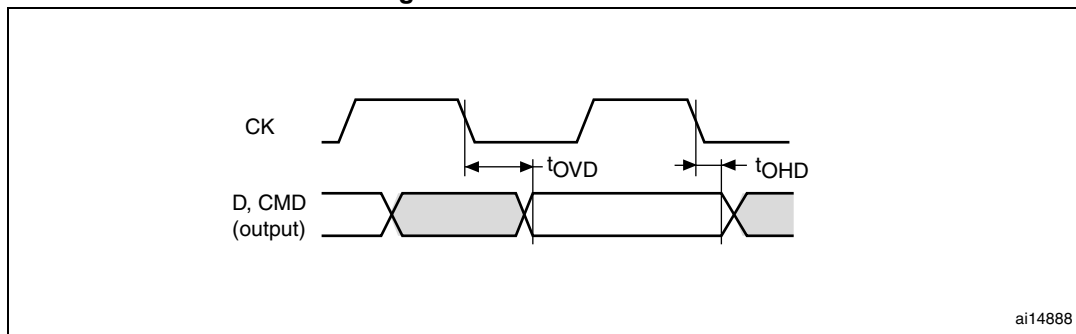
1. Guaranteed by design and/or characterization results.

2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 10](#).

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 54. SDIO high-speed mode**Figure 55. SD default mode****Table 55. SD / MMC characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
$tW(CKL)$	Clock low time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	32	-	ns
$tW(CKH)$	Clock high time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	30	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	4	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	

Table 55. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t _{ISU}	Input setup time	C _L ≤ 30 pF	2	-	ns
t _{IH}	Input hold time	C _L ≤ 30 pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t _{OV}	Output valid time	C _L ≤ 30 pF	-	6	ns
t _{OH}	Output hold time	C _L ≤ 30 pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode ⁽¹⁾					
t _{OVD}	Output valid default time	C _L ≤ 30 pF	-	7	ns
t _{OHD}	Output hold default time	C _L ≤ 30 pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

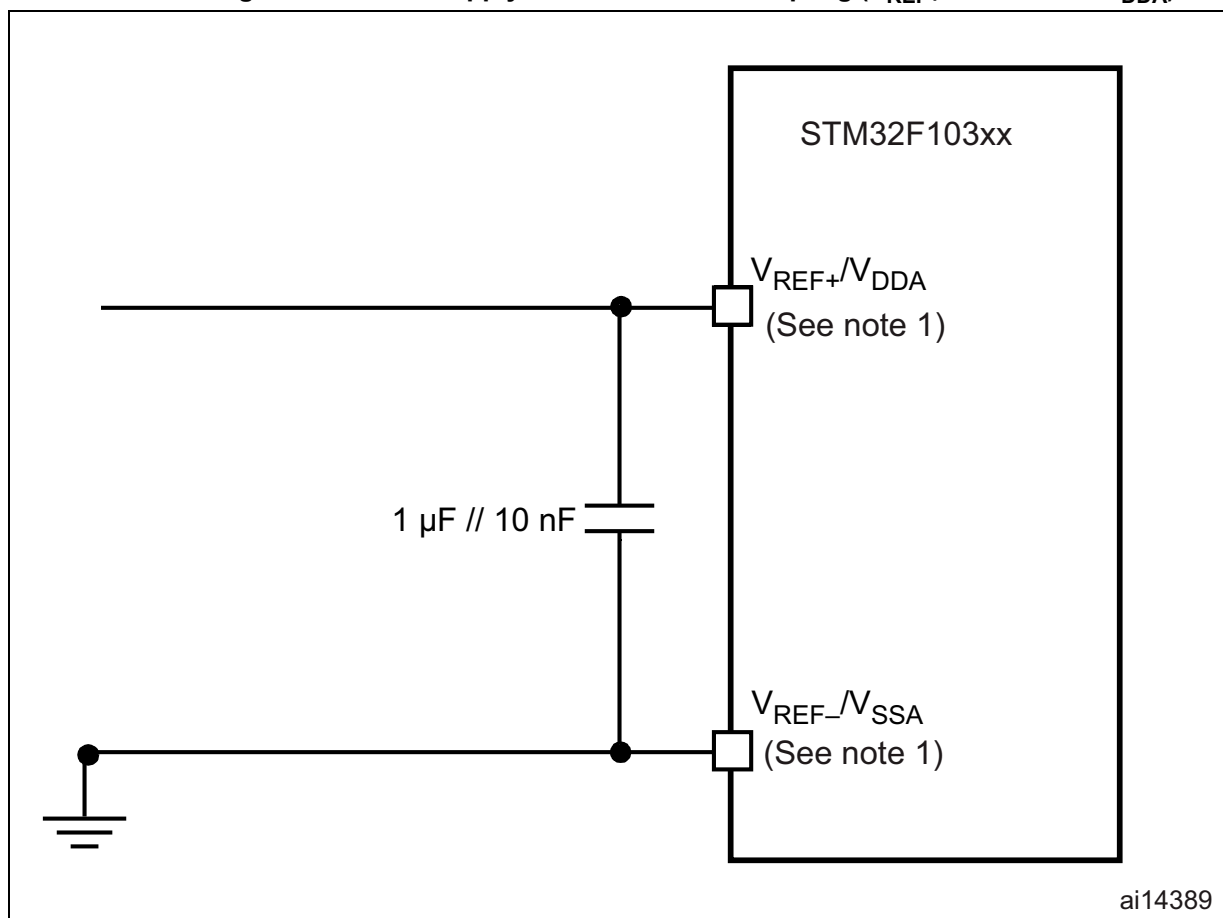
USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 56. USB startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB transceiver startup time	1	μs

1. Guaranteed by design.

Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

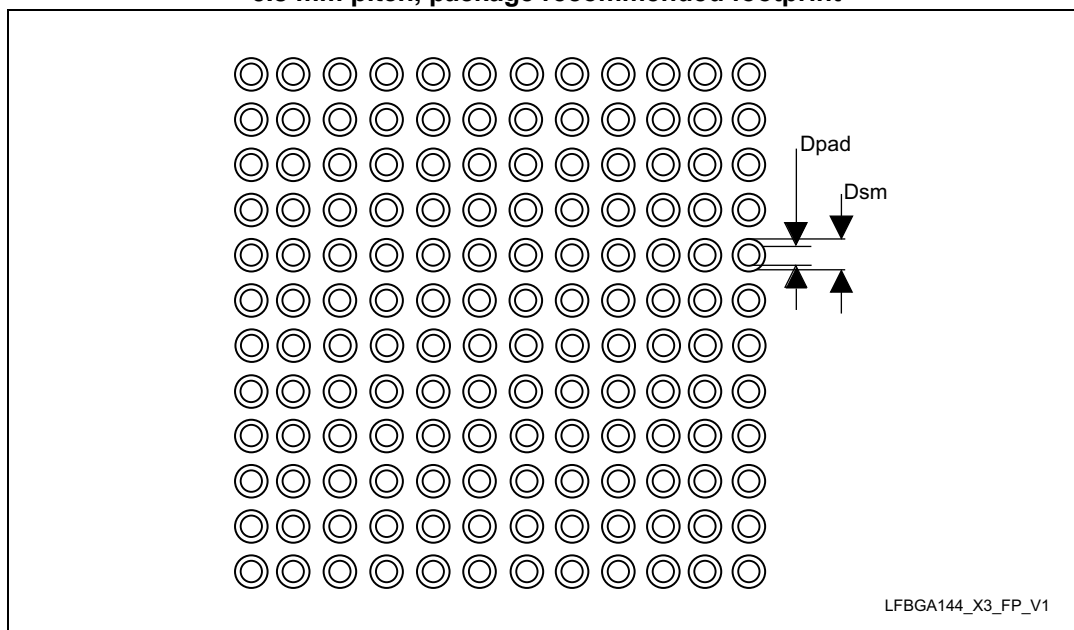
1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Typ	Min	Max
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.900	10.000	10.100	0.3898	0.3937	0.3976
D1	-	8.800	-	-	0.3465	-
E	9.900	10.000	10.100	0.3898	0.3937	0.3976
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

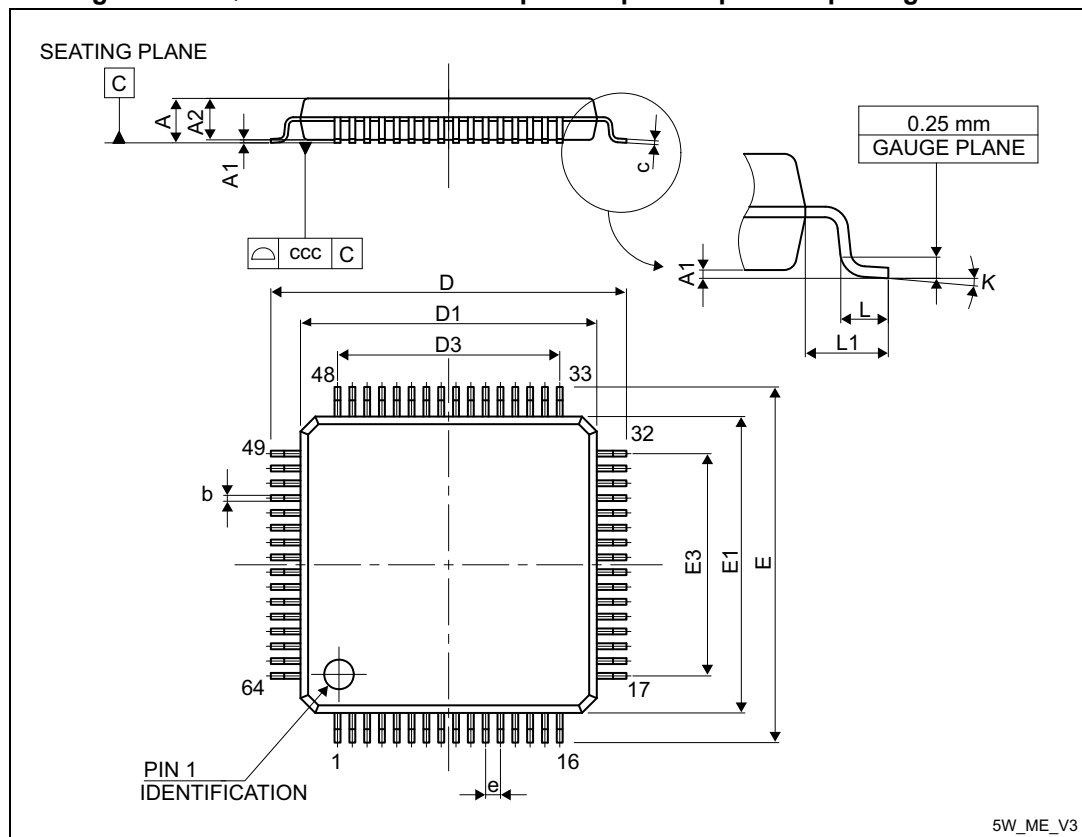
2. STATsChipPAC package dimensions.

Figure 63. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint**Table 66. LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.8 mm
D_{pad}	0.400 mm
UBM	0.350 mm

6.6 LQFP64 package information

Figure 76. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



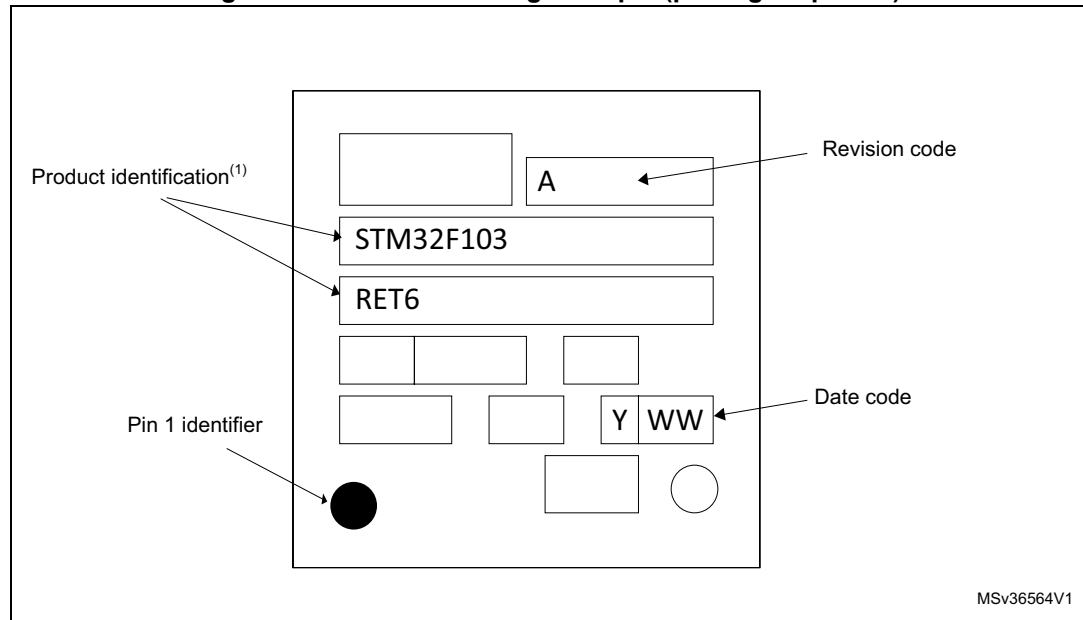
1. Drawing is not in scale.

Table 73. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking for LQFP64 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 78. LQFP64 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 76. Document revision history

Date	Revision	Changes
21-Jul-2008	3	Document status promoted from Preliminary Data to full datasheet. <i>FSMC (flexible static memory controller) on page 22</i> modified. Number of complementary channels corrected in <i>Figure 1: STM32F103xF, STM32F103xD and STM32F103xG STM32F103xF and STM32F103xG performance line block diagram</i>. <i>Power supply supervisor on page 23</i> modified and V_{DDA} added to <i>Table 14: General operating conditions on page 59</i>. Table notes revised in <i>Section 5: Electrical characteristics</i>. Capacitance modified in <i>Figure 12: Power supply scheme on page 57</i>. <i>Table 60: SCL frequency ($f_{PCLK1} = 36 \text{ MHz}$, $V_{DD} = 3.3 \text{ V}$)</i> updated. <i>Table 61: SPI characteristics</i> modified, $t_{h(NSS)}$ modified in <i>Figure 49: SPI timing diagram - slave mode and CPHA = 0 on page 123</i>. Minimum SDA and SCL fall time value for Fast mode removed from <i>Table 59: I²C characteristics on page 120</i>, note 1 modified. I_{DD_VBAT} values and some I_{DD} values with regulator in run mode added to <i>Table 21: Typical and maximum current consumptions in Stop and Standby modes on page 68</i>. <i>Table 34: Flash memory endurance and data retention on page 87</i> updated. $t_{su(NSS)}$ modified in <i>Table 61: SPI characteristics on page 122</i>. EO corrected in <i>Table 70: ADC accuracy on page 132</i>. <i>Figure 58: Typical connection diagram using the ADC on page 133</i> and note below corrected. Typical T_{S_temp} value removed from <i>Table 72: TS characteristics on page 137</i>. <i>Section 6.1: Package mechanical data on page 138</i> updated. Small text changes.