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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (4.47×4.4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rey6tr

List of figures

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xC, STM32F103xD and STM32F103xE performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from

Figure 8. STM32F103xC/D/E performance line WLCSP64 ballout, ball side

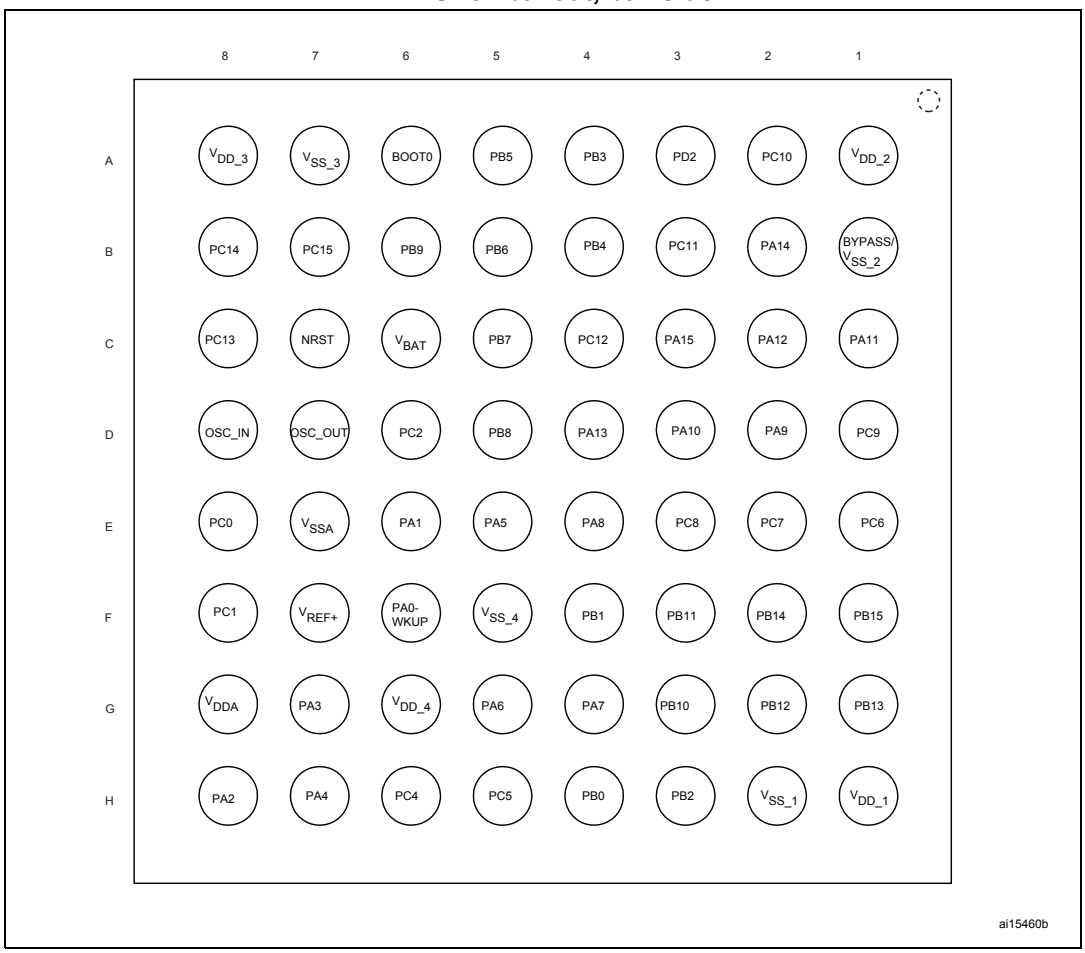


Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
G12	F10	E1	37	63	96	PC6	I/O	FT	PC6	I2S2_MCK/ TIM8_CH1/SDIO_D6	TIM3_CH1
F12	E10	E2	38	64	97	PC7	I/O	FT	PC7	I2S3_MCK/ TIM8_CH2/SDIO_D7	TIM3_CH2
F11	F9	E3	39	65	98	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
E11	E9	D1	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
E12	D9	E4	41	67	100	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(9)/MCO	-
D12	C9	D2	42	68	101	PA9	I/O	FT	PA9	USART1_TX(9)/ TIM1_CH2(9)	-
D11	D10	D3	43	69	102	PA10	I/O	FT	PA10	USART1_RX(9)/ TIM1_CH3(9)	-
C12	C10	C1	44	70	103	PA11	I/O	FT	PA11	USART1_CTS/USBDM CAN_RX(9)/TIM1_CH4(9)	-
B12	B10	C2	45	71	104	PA12	I/O	FT	PA12	USART1_RTS/USBDP/ CAN_TX(9)/TIM1_ETR(9)	-
A12	A10	D4	46	72	105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
C11	F8	-	-	73	106	Not connected					-
G9	E6	B1	47	74	107	V_{SS_2}	S	-	V_{SS_2}	-	-
F9	F6	A1	48	75	108	V_{DD_2}	S	-	V_{DD_2}	-	-
A11	A9	B2	49	76	109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
A10	A8	C3	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS/ I2S3_WS	TIM2_CH1_ETR PA15 / SPI1_NSS
B11	B9	A2	51	78	111	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
B10	B8	B3	52	79	112	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
C10	C8	C4	53	80	113	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
E10	D8	D8	5	81	114	PD0	I/O	FT	OSC_IN(10)	FSMC_D2(11)	CAN_RX
D10	E8	D7	6	82	115	PD1	I/O	FT	OSC_OUT(10)	FSMC_D3(11)	CAN_TX
E9	B7	A3	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	-
D9	C7	-	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	-
E5	E5	A7	63	99	143	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	F5	A8	64	100	144	V_{DD_3}	S	-	V_{DD_3}	-	-

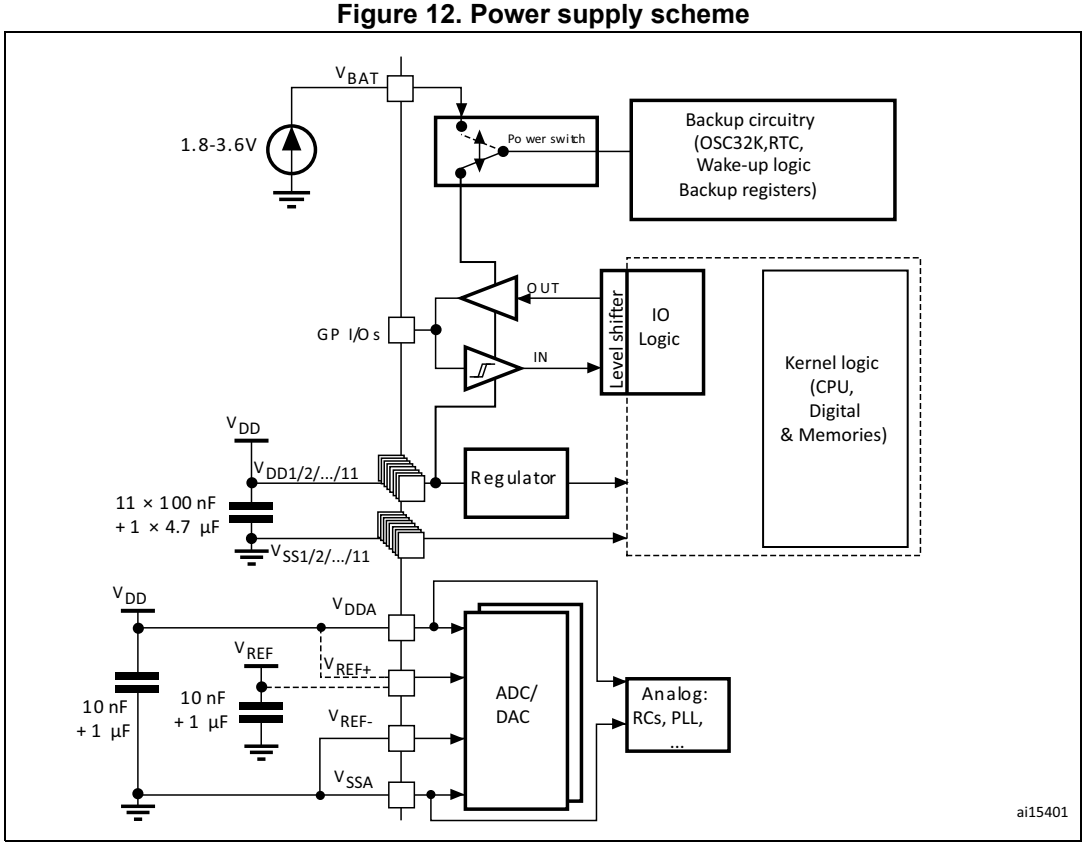
1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. In the WCLSP64 package, the PC3 I/O pin is not bonded and it must be configured by software to output mode (Push-pull) and writing 0 to the data register in order to avoid an extra consumption during low-power modes.
8. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
10. For the WCLSP64/LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
11. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 6. FSMC pin definition

Pins	FSMC					LQFP100 BGA100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

5.1.6 Power supply scheme

Figure 12. Power supply scheme



Caution: In *Figure 12*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme

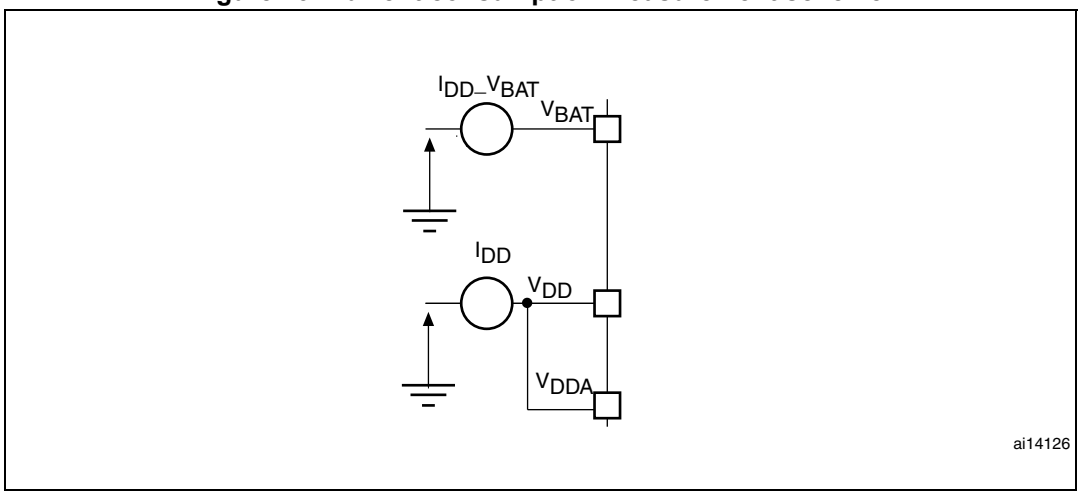


Table 20. Peripheral current consumption (continued)

Peripheral		Current consumption	Unit
APB2 (up to 72 MHz)	APB2-Bridge	4,17	µA/MHz
	GPIOA	8,47	
	GPIOB	8,47	
	GPIOC	6,53	
	GPIOD	8,47	
	GPIOE	6,53	
	GPIOF	6,53	
	GPIOG	6,11	
	SPI1	4,72	
	USART1	12,50	
	TIM1	22,92	
	TIM8	22,92	
	ADC1(4)	17,32	
	ADC2(4)	15,18	
	ADC3(4)	14,82	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1 or DMA2).
2. When the I2S is enabled, a current consumption equal to 0.02 mA must be added.
3. When DAC_OU1 or DAC_OUT2 is enabled, a current consumption equal to 0.36 mA must be added.
4. Specific conditions for measuring ADC current consumption: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADCx_CR2 register is set to 1, a current consumption of analog part equal to 0.54 mA must be added for each ADC.

Table 33. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms

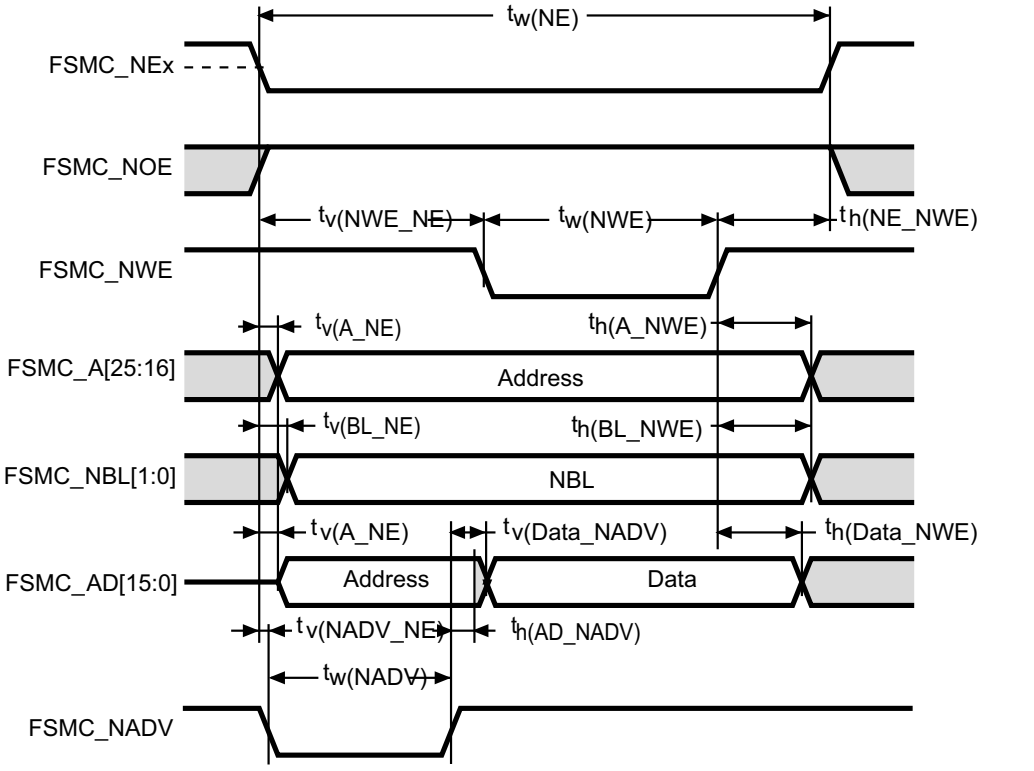
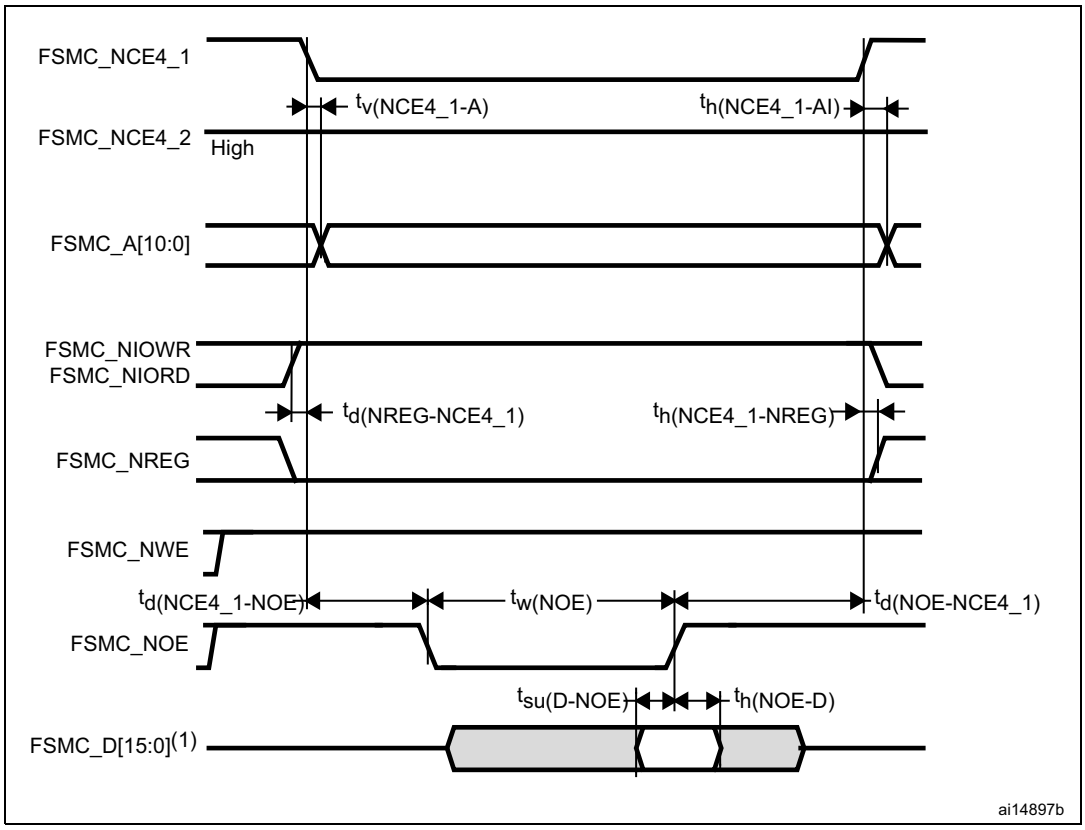


Table 34. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1$	$5t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$2t_{HCLK}$	$2t_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2t_{HCLK} - 1$	$2t_{HCLK} + 2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$t_{HCLK} - 1$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	ns

Figure 34. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 42. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP144 package compliant with IEC 61967-2	0.1 to 30 MHz	8	12	dBµV
			30 to 130 MHz	31	21	
			130 MHz to 1GHz	28	33	
			SAE EMI Level	4	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	III	500	

1. Guaranteed by characterization results.

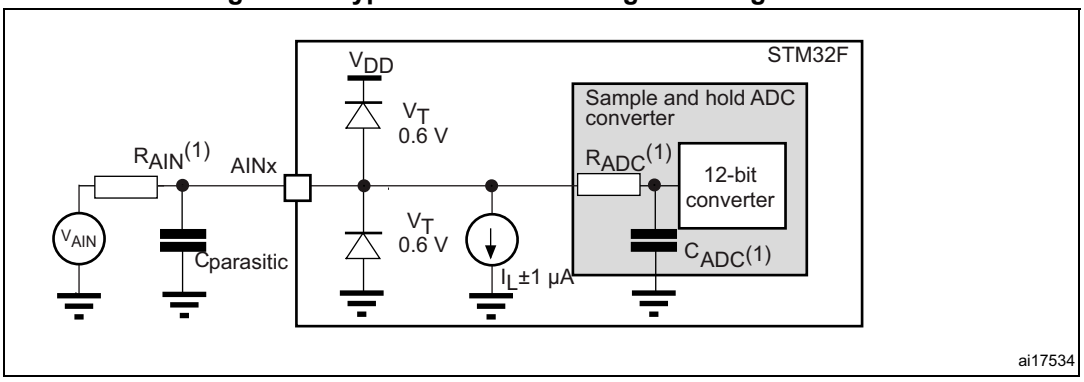
Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Figure 58. Typical connection diagram using the ADC

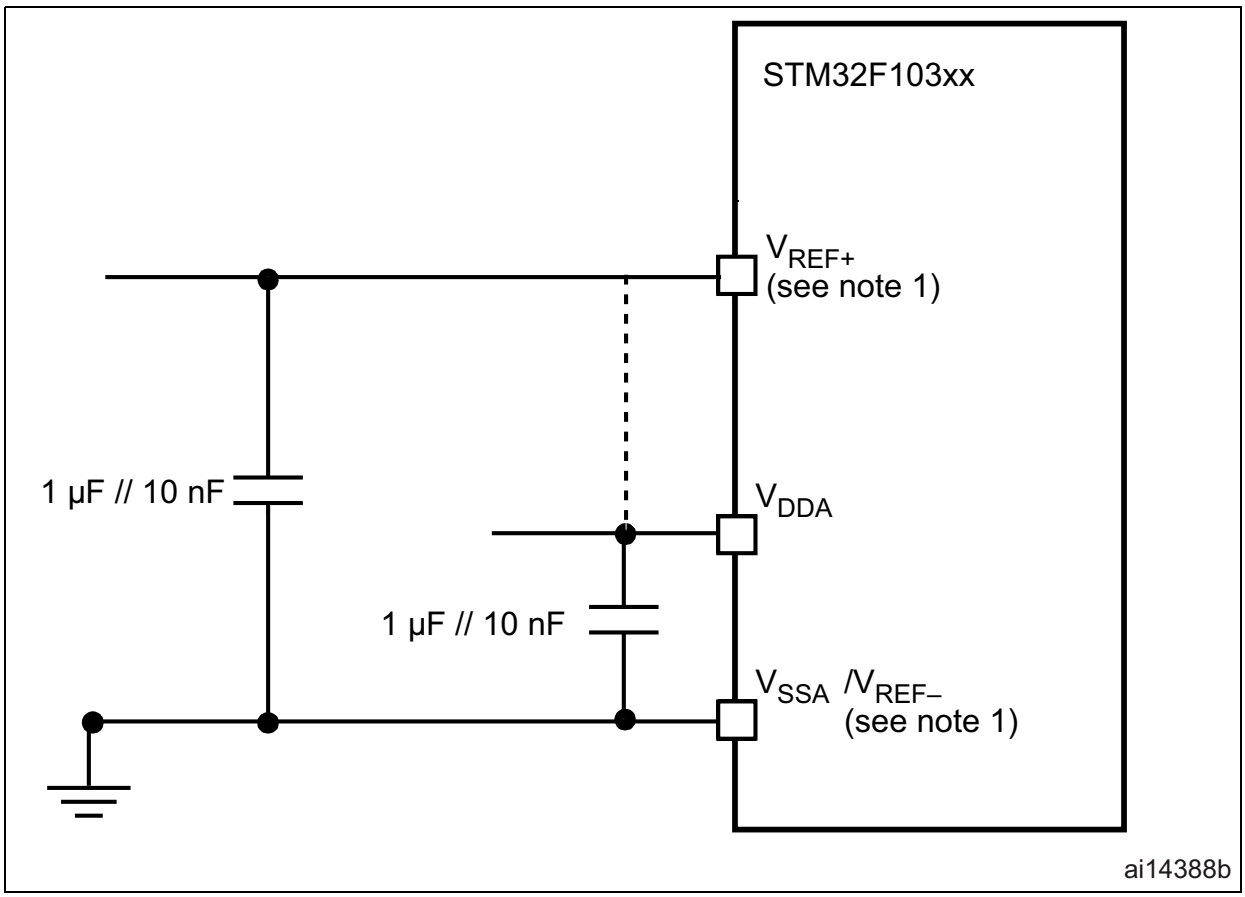


1. Refer to *Table 59* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

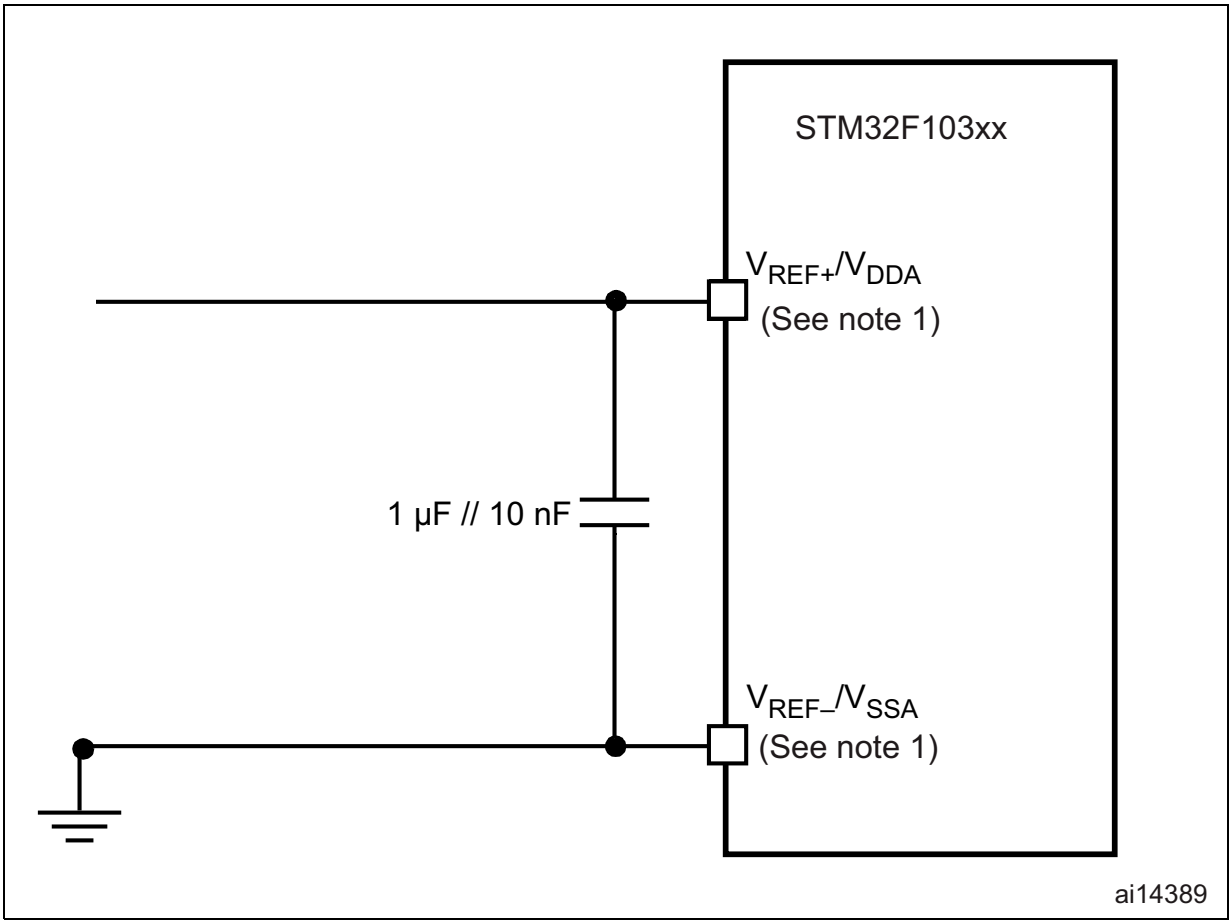
Power supply decoupling should be performed as shown in *Figure 59* or *Figure 60*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 59. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

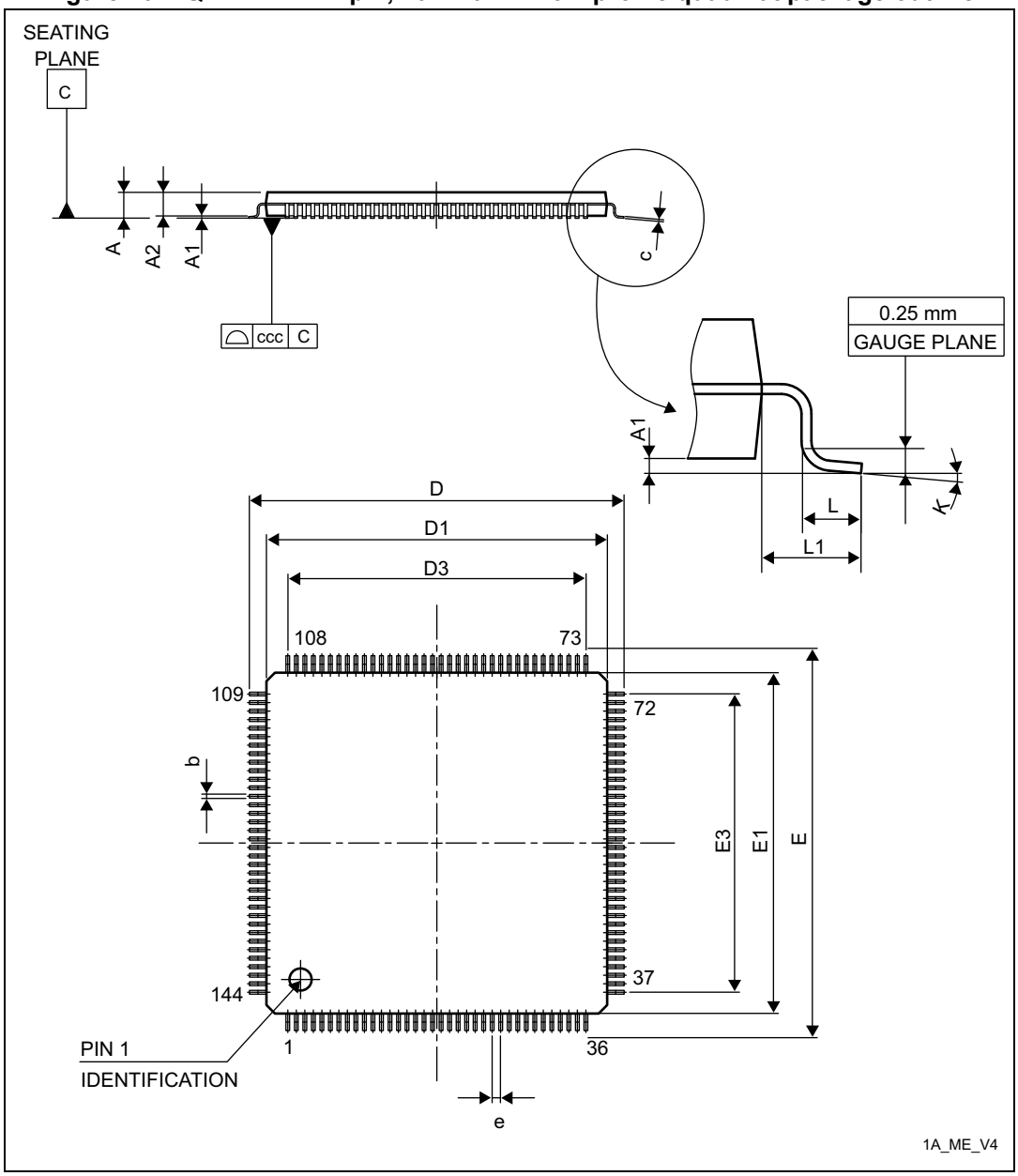
Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

6.4 LQFP144 package information

Figure 70. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Using the values obtained in *Table 74* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 75: Ordering information scheme*).

Figure 79. LQFP100 P_D max vs. T_A

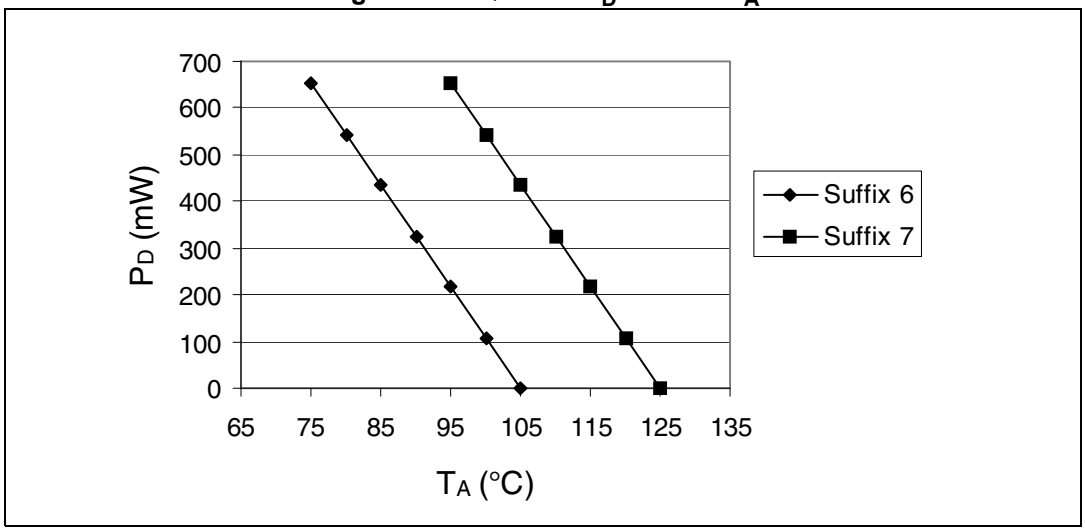


Table 76.Document revision history

Date	Revision	Changes
21-Jul-2008	3	Document status promoted from Preliminary Data to full datasheet. *FSMC (flexible static memory controller) on page 22* modified. Number of complementary channels corrected in *Figure 1: STM32F103xF, STM32F103xD and STM32F103xGSTM32F103xF and STM32F103xG performance line block diagram*. *Power supply supervisor on page 23* modified and V_{DDA} added to *Table 14: General operating conditions on page 59*. Table notes revised in *Section 5: Electrical characteristics*. Capacitance modified in *Figure 12: Power supply scheme on page 57*. *Table 60: SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)* updated. *Table 61: SPI characteristics* modified, $t_{h(NSS)}$ modified in *Figure 49: SPI timing diagram - slave mode and CPHA = 0 on page 123*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 59: I^2C characteristics on page 120*, note 1 modified. I_{DD_VBAT} values and some I_{DD} values with regulator in run mode added to *Table 21: Typical and maximum current consumptions in Stop and Standby modes on page 68*. *Table 34: Flash memory endurance and data retention on page 87* updated. $t_{su(NSS)}$ modified in *Table 61: SPI characteristics on page 122*. EO corrected in *Table 70: ADC accuracy on page 132*. *Figure 58: Typical connection diagram using the ADC on page 133* and note below corrected. Typical T_{S_temp} value removed from *Table 72: TS characteristics on page 137*. *Section 6.1: Package mechanical data on page 138* updated. Small text changes.

Table 76.Document revision history

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified *on page 1*. *Figure 4: STM32F103xC and STM32F103xE performance line BGA100 ballout* corrected. I/O information clarified *on page 1*. In *Table 5: High-density STM32F103xx pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column PG14 pin description modified in *Table 6: FSMC pin definition*. *Figure 9: Memory map on page 54* modified. Note modified in *Table 18: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 20: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 17*, *Figure 18* and *Figure 19* show typical curves (titles changed). *Table 25: High-speed external user clock characteristics* and *Table 26: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 29: HSI oscillator characteristics*. FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 24: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 25: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 35: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 39: Asynchronous multiplexed PSRAM/NOR write timings*. $t_{h(Data\_NWE)}$ modified in *Table 36: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings* In *Table 41: Synchronous multiplexed PSRAM write timings* and *Table 43: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 28: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 29: Synchronous multiplexed PSRAM write timings* and *Figure 31: Synchronous non-multiplexed PSRAM write timings* modified. *Figure 52: I2S slave timing diagram (Philips protocol)(1)* and *Figure 53: I2S master timing diagram (Philips protocol)(1)* modified. WLCSP64 package added (see *Figure 8: STM32F103xC and STM32F103xE performance line WLCSP64 ballout, ball side*, *Table 8: High-density STM32F103xx pin definitions*, *Figure 65: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline* and *Table 76: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data*). Small text changes.