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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Det	ails
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Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vct6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.3 Overview

2.3.1 ARM[®] Cortex[®]-M3 core with embedded Flash and SRAM

The ARM Cortex[®]-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex[®]-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xC, STM32F103xD and STM32F103xE performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz



2.3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.30 Embedded Trace Macrocell™

The ARM[®] Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.



	1	2	3	4	5	6	7	8	9	10
А	PC14- OSC32_IN	PC13- TAMPER- RTC	PE2	PB9	РВ7	PB4	PB3	PA15	PA14	PA13
В	PC15- pSC32_OUT	V _{BAT}	PE3	PB8	PB6	PD5	PD2	PC11	PC10	PA12
с	OSC_IN	V _{SS_5}	PE4	PE1	PB5	PD6	PD3	PC12	PA9	PA11
D	OSC_OUT	V _{DD_5}	PES	PEO	BOOTO	PD7	PD4	PDO	PA8	PA10
E	NRST	PC2	PE6	V _{SS_4}	V _{SS_3}	V _{SS_2}	V _{SS_1}	PD1	PC9	PC7
F	PCO	PC1	PC3	V _{DD_4}	V _{DD_3}	V _{DD_2}	V _{DD_1}	NC	PC8	PC6
G	V _{SSA}	PA0-WKUP	PA4	PC4	PB2	PE10	PE14	PB15	PD11	PD15
н	V _{REF-}	PA1	PA5	PC5	PE7	PE11	PE15	PB14	PD10	PD14
J	V _{REF+}	PA2	PA6	PB0	PE8	PE12	PB10	PB13	PD9	PD13
к	V _{DDA}	РАЗ	PA7	PB1	PE9	PE13	PB11	PB12	PD8	PD12
										Al14601c

Figure 4. STM32F103xC/D/E performance line BGA100 ballout

1. The above figure shows the package top view.



		Pir	าร			<u> </u>				Alternate funct	tions ⁽⁴⁾
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144	Pin name	Type ⁽¹⁾	I / O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Default	Remap
M11	K8	G2	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK ⁽⁹⁾ / TIM1_BKIN ⁽⁹⁾	-
M12	J8	G1	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS ⁽⁹⁾ / TIM1_CH1N	-
L11	H8	F2	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS ⁽⁹⁾ /	-
L12	G8	F1	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N ⁽⁹⁾ /	-
L9	K9	-	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	J9	-	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	H9	-	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	G9	-	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	K10	-	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	J10	-	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	-	-	83	V _{SS_8}	S	-	V _{SS_8}	-	-
F8	-	I	-	I	84	V_{DD_8}	S	-	V_{DD_8}	-	-
K11	H10	I	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	G10	-	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	-	-	87	PG2	I/O	FT	PG2	FSMC_A12	-
J11	-	-	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	-
J10	-	-	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	-
H12	-	-	-	-	90	PG5	I/O	FT	PG5	FSMC_A15	-
H11	-	-	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	-
H10	-	-	-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	-
G11	-	-	-	-	93	PG8	I/O	FT	PG8	-	-
G10	-	-	-	-	94	V _{SS_9}	S	-	V _{SS_9}	-	-
F10	-	-	-	-	95	V _{DD_9}	S	-	V _{DD_9}	-	-



	FSMC					
Pins	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	LQFP100 BGA100 ⁽¹⁾
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 6. FSMC pin definition



4 Memory mapping

The memory map is shown in Figure 9.



Figure 9. Memory map







Figure 20. High-speed external clock source AC timing diagram







High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R _F	Feedback resistor	-	-	200	-	kΩ
С	Recommended load capacitance versus equivalent serial resistance of the crystal $(R_S)^{(3)}$	R _S = 30 Ω	-	30	-	pF
i ₂	HSE driving current	V _{DD} = 3.3 V, V _{IN} = V _{SS} with 30 pF load	-	-	1	mA
9 _m	Oscillator transconductance	Startup	25	-	-	mA/V
t _{SU(HSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized	-	2	-	ms

Fable 23. HSE 4-16 MHz oscillator characteristics ⁽¹⁾⁽²	2)
--	----

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by characterization results.

3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.

4. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 22*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website *www.st.com*.





1. R_{EXT} value depends on the crystal characteristics.

DocID14611 Rev 12



5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Symbol	Doromotor		Unit		
Symbol	Falameter	Min	Тур	Max ⁽¹⁾	Unit
f	PLL input clock ⁽²⁾	1	8.0	25	MHz
'PLL_IN	PLL input clock duty cycle	40	-	60	%
f _{PLL_OUT}	PLL multiplier output clock	16	-	72	MHz
t _{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

|--|

1. Guaranteed by characterization results.

2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{\text{PLL}_{OUT}}$.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
t _{prog}	16-bit programming time	$T_A = -40$ to +105 °C	40	52.5	70	μs
t _{ERASE}	Page (2 KB) erase time	T _A = -40 to +105 °C	20	-	40	ms
t _{ME}	Mass erase time	T _A = -40 to +105 °C	20	-	40	ms
		Read mode f _{HCLK} = 72 MHz with 2 wait states, V _{DD} = 3.3 V	-	-	28	mA
I _{DD}	Supply current	Write mode f _{HCLK} = 72 MHz, V _{DD} = 3.3 V	-	-	7	mA
		Erase mode f _{HCLK} = 72 MHz, V _{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V _{DD} = 3.0 to 3.6 V	-	-	50	μA
V _{prog}	Programming voltage	-	2	-	3.6	V

Table 29. Flash memory characteristics

1. Guaranteed by design.





Figure 29. Synchronous multiplexed PSRAM write timings





Figure 30. Synchronous non-multiplexed NOR/PSRAM read timings

Table 37. Synchronous	non-multiplexed NOR/PSRAM	l read timings ⁽¹⁾⁽²⁾
,		

Symbol	Parameter	Min	Max	Unit
t _{w(CLK)}	FSMC_CLK period	27.7	-	ns
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x = 02)	-	1.5	ns
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x = 02)	2	-	ns
t _{d(CLKL-NADVL)}	FSMC_CLK low to FSMC_NADV low	-	4	ns
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	5	-	ns
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x = 025)	-	0	ns
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x = 025)	4	-	ns
t _{d(CLKL-NOEL)}	FSMC_CLK low to FSMC_NOE low	-	1.5	ns
t _{d(CLKL-NOEH)}	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
t _{su(DV-CLKH)}	su(DV-CLKH) FSMC_D[15:0] valid data before FSMC_CLK high		-	ns
t _{h(CLKH-DV)}	FSMC_D[15:0] valid data after FSMC_CLK high	7	-	ns
t _{su(NWAITV-CLKH)}	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
t _{h(CLKH-NWAITV)}	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.

2. Guaranteed by characterization results.





Figure 31. Synchronous non-multiplexed PSRAM write timings

Table 38. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
t _{w(CLK)}	FSMC_CLK period	27.7	-	ns
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x = 02)	-	2	ns
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x = 02)	2	-	ns
t _{d(CLKL-NADVL)}	FSMC_CLK low to FSMC_NADV low	-	4	ns
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	5	-	ns
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x = 1625)	-	0	ns
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x = 1625)	2	-	ns
t _{d(CLKL-NWEL)}	FSMC_CLK low to FSMC_NWE low	-	1	ns
t _{d(CLKL-NWEH)}	FSMC_CLK low to FSMC_NWE high	1	-	ns
t _{d(CLKL-Data)}	FSMC_D[15:0] valid data after FSMC_CLK low	-	6	ns
t _{d(CLKL-NBLH)}	FSMC_CLK low to FSMC_NBL high	1	-	ns
t _{su(NWAITV-CLKH)}	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
t _{h(CLKH-NWAITV)}	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.

2. Guaranteed by characterization results.



NAND controller waveforms and timings

Figure 38 through *Figure 41* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 38. NAND controller waveforms for read access





5.3.21 Temperature sensor characteristics

Symbol	Parameter	Min	Тур	Max	Unit
TL	V _{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope	Average slope	4.0	4.3	4.6	mV/°C
V ₂₅	Voltage at 25 °C	1.34	1.43	1.52	V
t _{START} ⁽¹⁾	Startup time	4	-	10	μs
T _{S_temp} ⁽²⁾⁽¹⁾	ADC sampling time when reading the temperature	-	-	17.1	μs

Table 64. TS characteristics

1. Guaranteed by design.

2. Shortest sampling time can be determined in the application by multiple iterations.



		millimatora	J	inchos ⁽¹⁾		
Symbol	millimeters			Incnes		
	Min	Тур	Мах	Тур	Min	Мах
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.900	10.000	10.100	0.3898	0.3937	0.3976
D1	-	8.800	-	-	0.3465	-
E	9.900	10.000	10.100	0.3898	0.3937	0.3976
E1	-	8.800	-	-	0.3465	-
е	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm,0.8 mm pitch, package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. STATSChipPAC package dimensions.





Table 66. LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values	
Pitch	0.8 mm	
Dpad	0.400 mm	
UBM	0.350 mm	

DocID14611 Rev 12



meenamear data (continued)						
Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Мах
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

Table 72. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 74. LQFP100 recommended footprint

1. Dimensions are in millimeters.



Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



Device marking for LQFP64 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.



Figure 78. LQFP64 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



Using the values obtained in *Table 74* T_{Jmax} is calculated as follows:

- For LQFP100, 46 °C/W
- T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 75: Ordering information scheme*).







Date	Revision	Changes
Date 21-Jul-2009	Revision	ChangesFigure 1: STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram updated.Note 5 updated and Note 4 added in Table 5: High-densitySTM32F103xC/D/E pin definitions.VRERINT and T _{Coeff} added to Table 13: Embedded internal reference voltage.Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM modified.f _{HSE-ext} min modified in Table 21: High-speed external user clock
		<i>buffered DAC</i> added. <i>Figure 63: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline</i> and <i>Table 75: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data</i> updated.
24-Sep-2009	7	Number of DACs corrected in <i>Table 3: STM32F103xx family</i> . I _{DD_VBAT} updated in <i>Table 17: Typical and maximum current</i> <i>consumptions in Stop and Standby modes</i> . <i>Figure 16: Typical current consumption on VBAT with RTC on vs.</i> <i>temperature at different VBAT values</i> added. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to
		IEC 61967-2 in Section 5.3.11: EMC characteristics on page 87. Table 63: DAC characteristics modified. Small text changes.

Table 76.Document revision history

