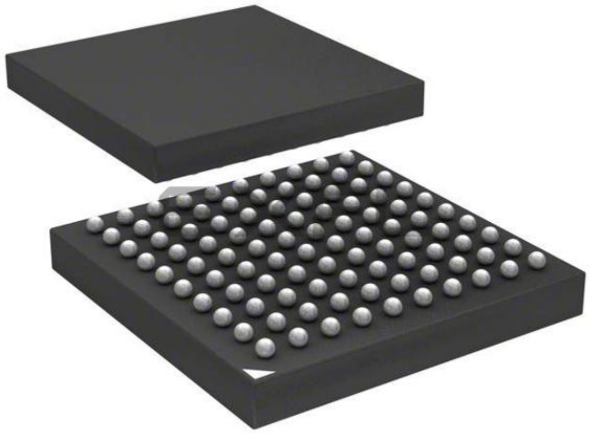

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What is "Embedded - Microcontrollers"?

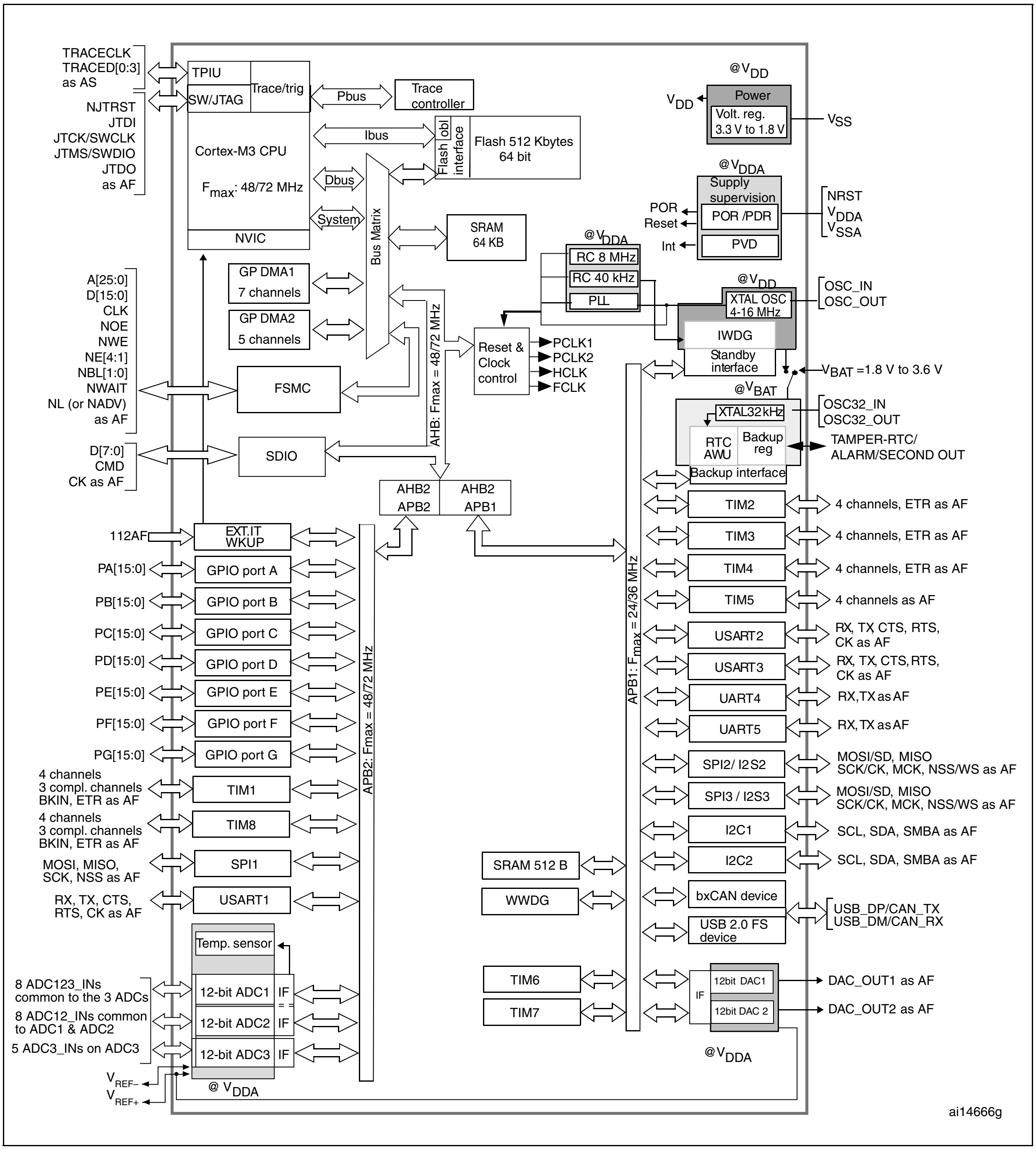
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vdh6

List of figures

Figure 1. STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 75*) or –40 °C to +105 °C (suffix 7, see *Table 75*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.9

2.3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.30 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
M11	K8	G2	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK[9]/ TIM1_BKIN[9]	-
M12	J8	G1	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS[9]/ TIM1_CH1N	-
L11	H8	F2	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS[9]/	-
L12	G8	F1	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N[9]/	-
L9	K9	-	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	J9	-	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	H9	-	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	G9	-	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	K10	-	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	J10	-	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	-	-	83	V_{SS_8}	S	-	V_{SS_8}	-	-
F8	-	-	-	-	84	V_{DD_8}	S	-	V_{DD_8}	-	-
K11	H10	-	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	G10	-	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	-	-	87	PG2	I/O	FT	PG2	FSMC_A12	-
J11	-	-	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	-
J10	-	-	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	-
H12	-	-	-	-	90	PG5	I/O	FT	PG5	FSMC_A15	-
H11	-	-	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	-
H10	-	-	-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	-
G11	-	-	-	-	93	PG8	I/O	FT	PG8	-	-
G10	-	-	-	-	94	V_{SS_9}	S	-	V_{SS_9}	-	-
F10	-	-	-	-	95	V_{DD_9}	S	-	V_{DD_9}	-	-

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 11* are derived from tests performed under the ambient temperature condition summarized in *Table 10*.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 24. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, $V_{IN} = V_{SS}$		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer, PCB layout and humidity.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 23). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3t_{HCLK} - 1$	$3t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7.5	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	$t_{HCLK} + 7$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$t_{HCLK} + 1.5$	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms

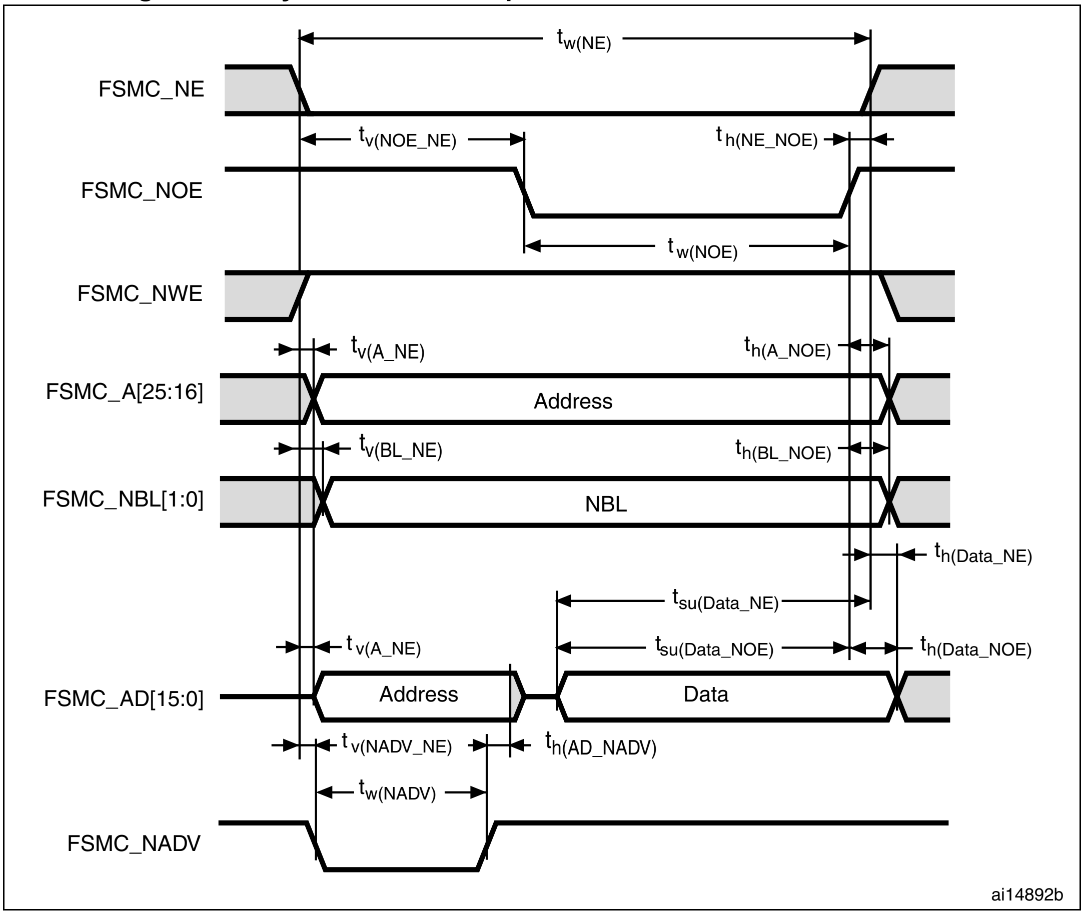


Table 33. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

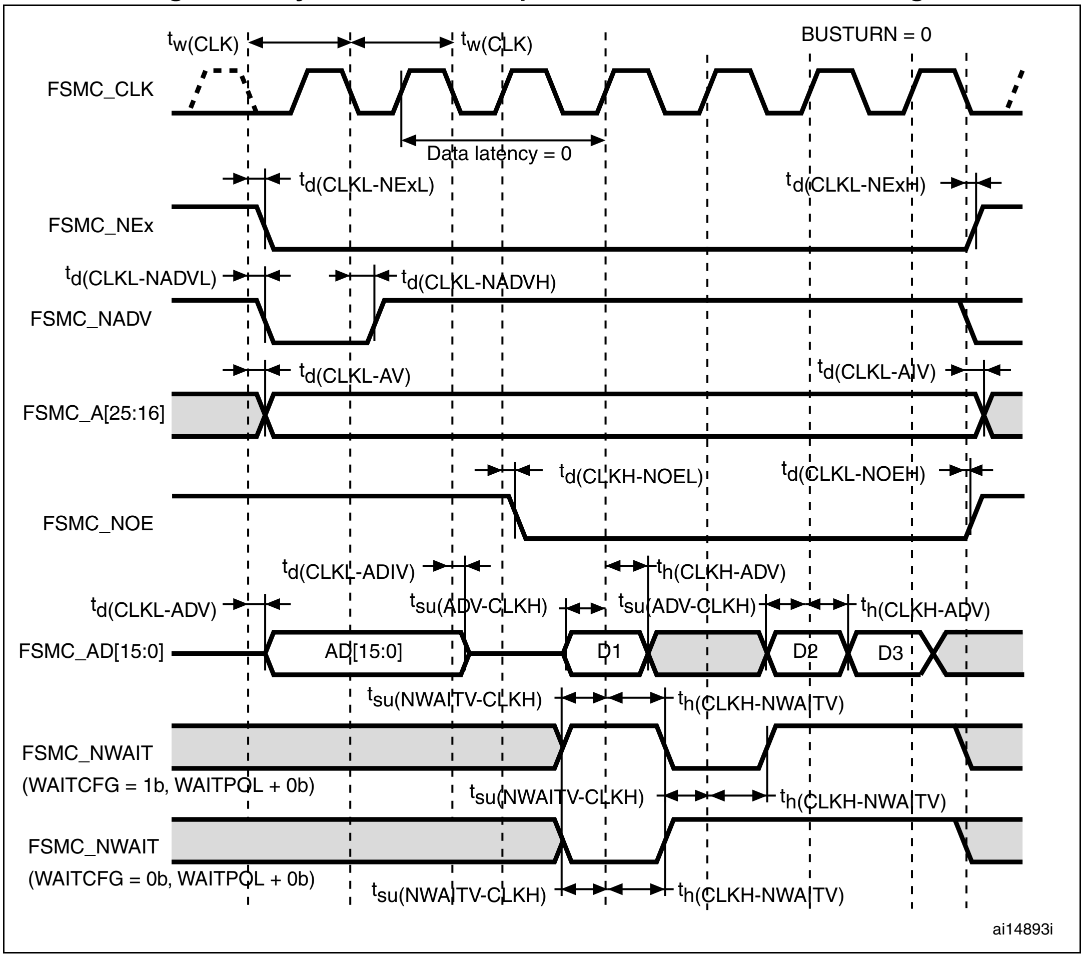
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK} - 2$	$7t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} -1.5$	$t_{HCLK} + 1.5$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} -2	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 24$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2t_{HCLK} + 25$	-	ns

Synchronous waveforms and timings

Figure 28 through *Figure 31* represent synchronous waveforms and *Table 36* through *Table 38* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 28. Synchronous multiplexed NOR/PSRAM read timings



5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

Figure 42. Standard I/O input characteristics - CMOS port

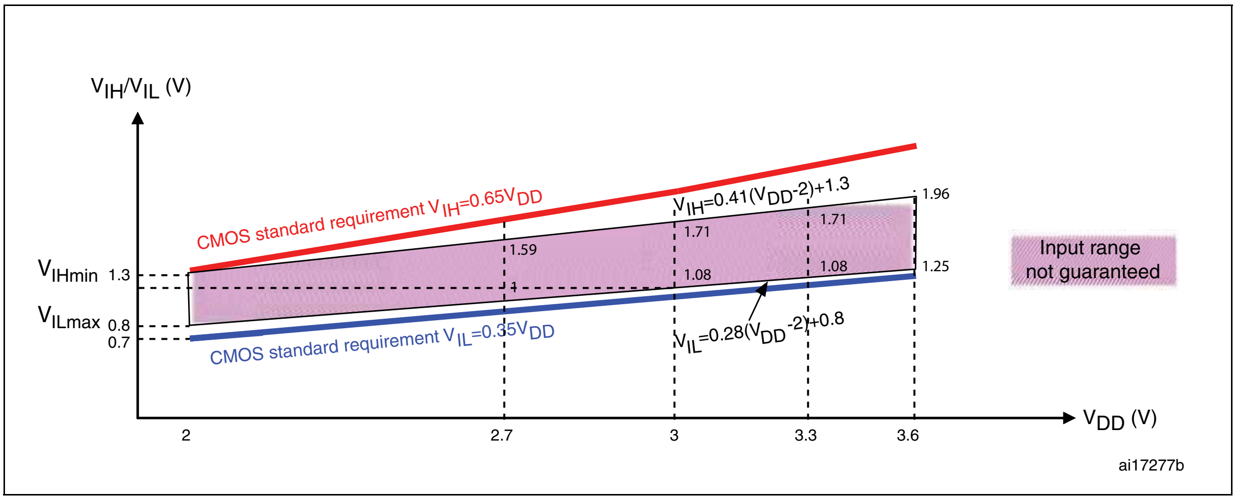


Figure 43. Standard I/O input characteristics - TTL port

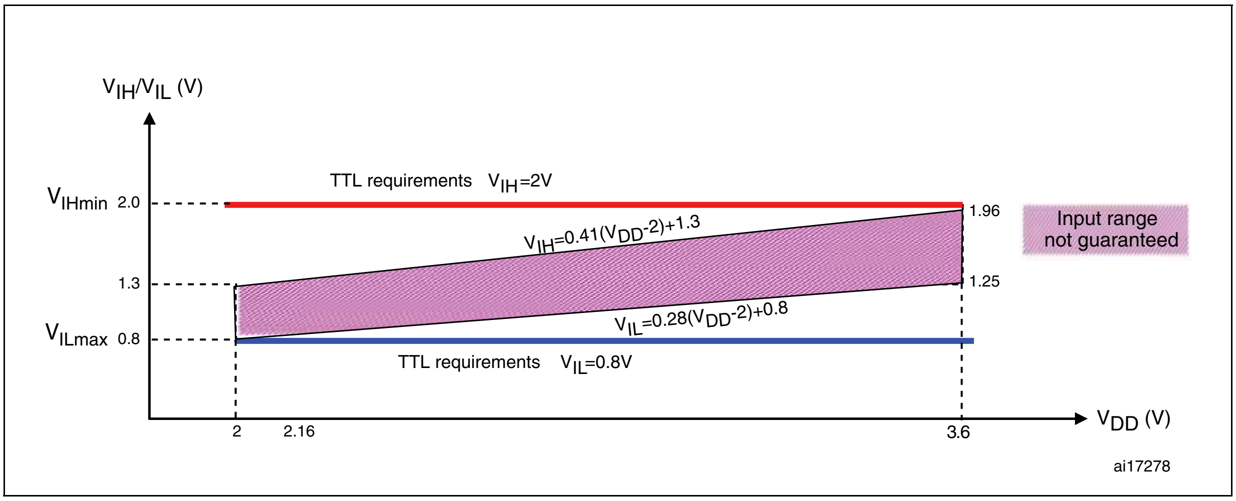


Figure 44. 5 V tolerant I/O input characteristics - CMOS port

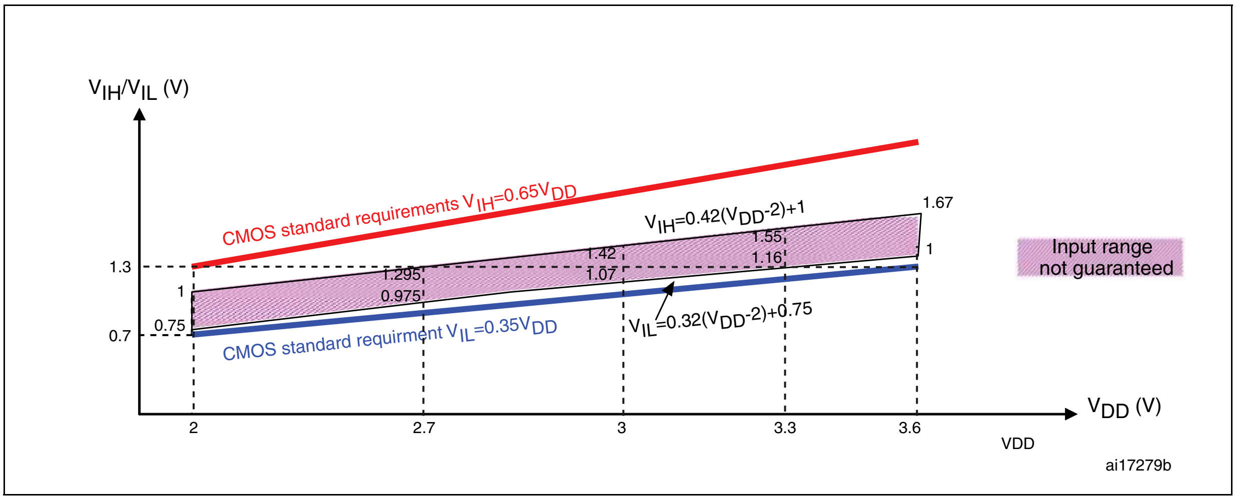
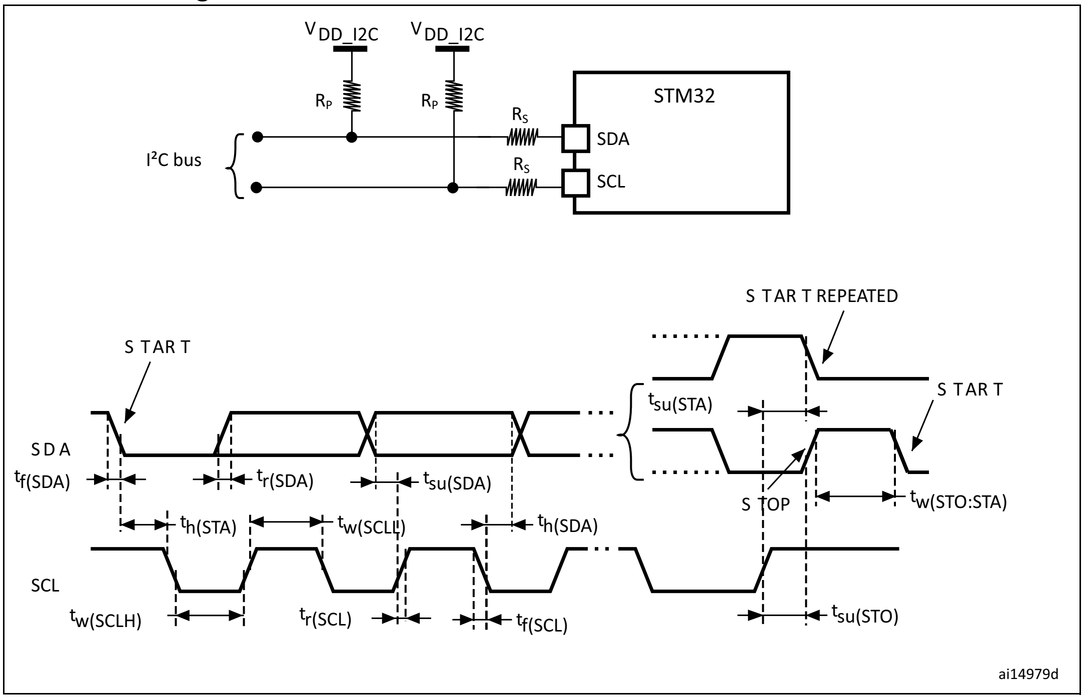


Figure 48. I^2C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs: Series protection resistors.
3. Rp: Pull-up resistors.
4. VDD_I2C : I2C bus supply

Table 52. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Table 54. I^2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)		1.522	1.525	MHz
		Slave mode		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode		4	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
$t_{w(CKH)}$ (1)	CK high and low time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz		312.5	-	
$t_{w(CKL)}$ (1)				345	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	2	-	
			I2S3	6.5	-	
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver		1.5	-	
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver		0	-	
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver		0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)		-	18	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)		11	-	
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)		-	3	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)		0	-	

1. Guaranteed by design and/or characterization results.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.

Table 55. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 56. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 67. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 66. LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprintoutline

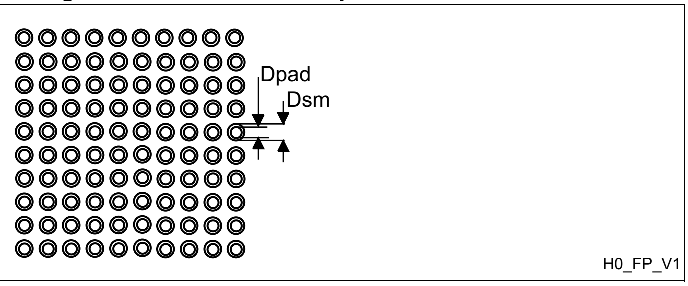


Table 68. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

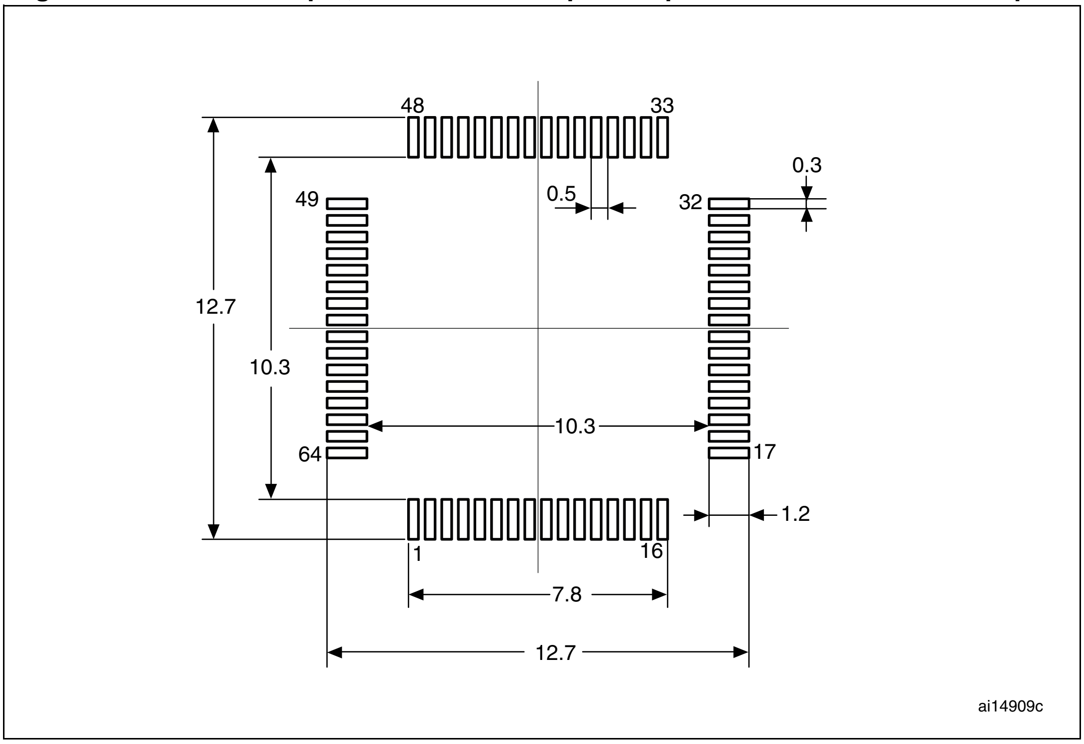
Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Table 73. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

7 Part numbering

Table 75. Ordering information scheme

Example: STM32 F 103 R C T 6 xxx

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = general-purpose

Device subfamily
103 = performance line

Pin count
R = 64 pins
V = 100 pins
Z = 144 pins

Flash memory size
C = 256 Kbytes of Flash memory
D = 384 Kbytes of Flash memory
E = 512 Kbytes of Flash memory

Package
H = BGA
T = LQFP
Y = WLCSP64

Temperature range
6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options
xxx = programmed parts
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 76.Document revision history

Date	Revision	Changes
12-Dec-2008	4	Timers specified on page 1 (motor control capability mentioned). Section 2.2: Full compatibility throughout the family updated. Table 6: High-density timer feature comparison added. General-purpose timers (TIMx) and Advanced-control timers (TIM1 and TIM8) on page 27 updated. Figure 1: STM32F103xF, STM32F103xD and STM32F103xGSTM32F103xF and STM32F103xG performance line block diagram modified. Note 10 added, main function after reset and Note 5 on page 44 updated in Table 8: High-density STM32F103xx pin definitions. Note 2 modified below Table 11: Voltage characteristics on page 58, $\|DV_{DDx}\|$ min and $\|DV_{DDx}\|$ min removed. Note 2 and P_D values for LQFP144 and LFBGA144 packages added to Table 14: General operating conditions on page 59. Measurement conditions specified in Section 5.3.5: Supply current characteristics on page 62. Max values at T_A = 85 °C and T_A = 105 °C updated in Table 21: Typical and maximum current consumptions in Stop and Standby modes on page 68. Section 5.3.10: FSMC characteristics on page 87 updated. Data added to Table 50: EMI characteristics on page 111. I_{VREF} added to Table 67: ADC characteristics on page 130. Table 81: Package thermal characteristics on page 146 updated. Small text changes.

Table 76.Document revision history

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified *on page 1*. *Figure 4: STM32F103xC and STM32F103xE performance line BGA100 ballout* corrected. I/O information clarified *on page 1*. In *Table 5: High-density STM32F103xx pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column PG14 pin description modified in *Table 6: FSMC pin definition*. *Figure 9: Memory map on page 54* modified. Note modified in *Table 18: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 20: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 17*, *Figure 18* and *Figure 19* show typical curves (titles changed). *Table 25: High-speed external user clock characteristics* and *Table 26: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 29: HSI oscillator characteristics*. FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 24: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 25: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 35: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 39: Asynchronous multiplexed PSRAM/NOR write timings*. $t_{h(Data\_NWE)}$ modified in *Table 36: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings* In *Table 41: Synchronous multiplexed PSRAM write timings* and *Table 43: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 28: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 29: Synchronous multiplexed PSRAM write timings* and *Figure 31: Synchronous non-multiplexed PSRAM write timings* modified. *Figure 52: I2S slave timing diagram (Philips protocol)(1)* and *Figure 53: I2S master timing diagram (Philips protocol)(1)* modified. WLCSP64 package added (see *Figure 8: STM32F103xC and STM32F103xE performance line WLCSP64 ballout, ball side*, *Table 8: High-density STM32F103xx pin definitions*, *Figure 65: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline* and *Table 76: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data*). Small text changes.