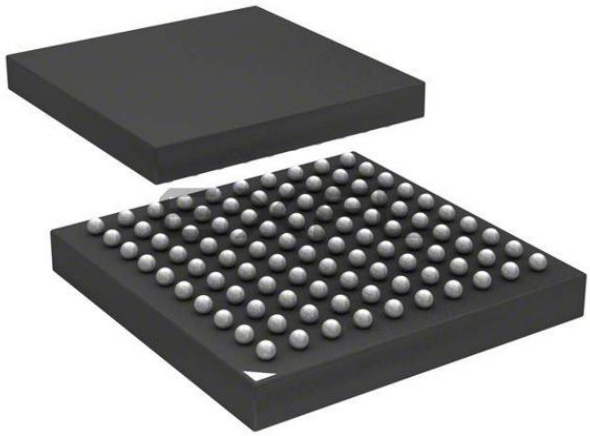

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vdh6tr

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP144	-	666	mW
		LQFP100	-	434	
		LQFP64	-	444	
		LFBGA100	-	500	
		LFBGA144	-	500	
		WLCSP64	-	400	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 59: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.7: Thermal characteristics on page 133*).
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.7: Thermal characteristics on page 133*).

Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

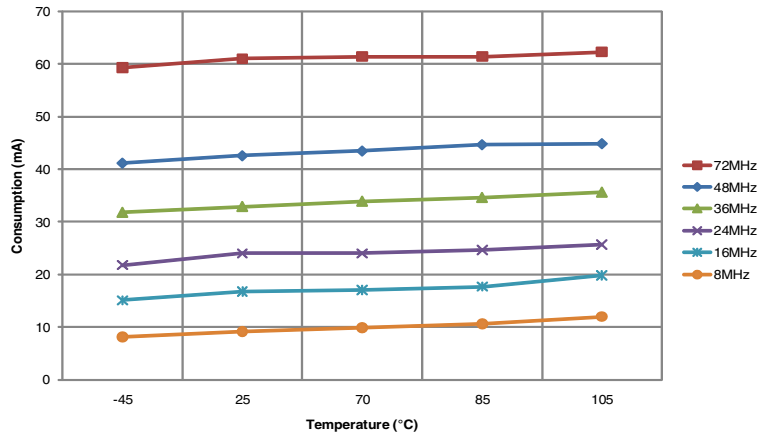


Figure 15. Typical current consumption in Run mode versus frequency (at 3.6 V)- code with data processing running from RAM, peripherals disabled

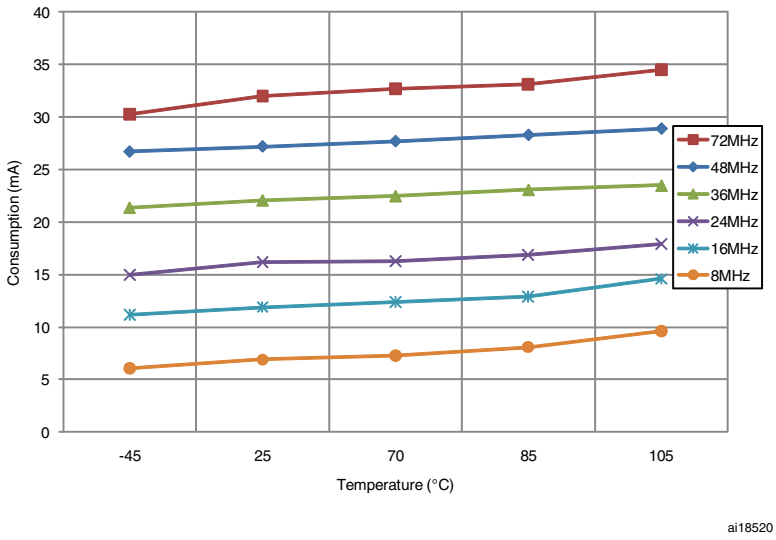
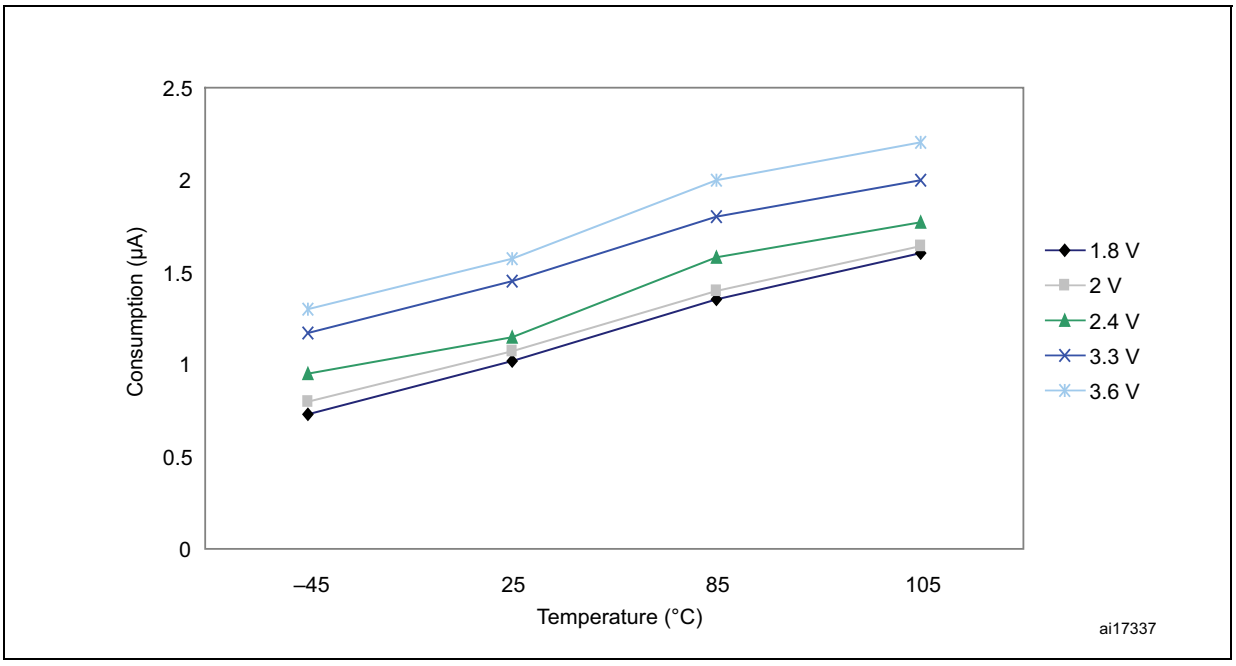


Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	1130	µA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	1110	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5(2)	6.5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2(2)	2.3(2)	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results.

Figure 16. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values



5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 21. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

The characteristics given in *Table 22* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 22. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 20. High-speed external clock source AC timing diagram

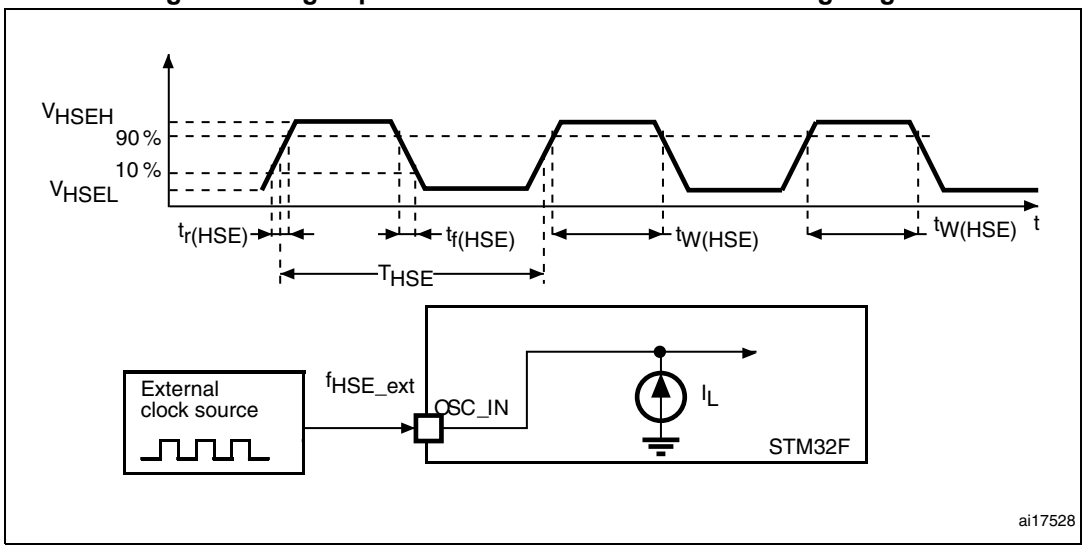
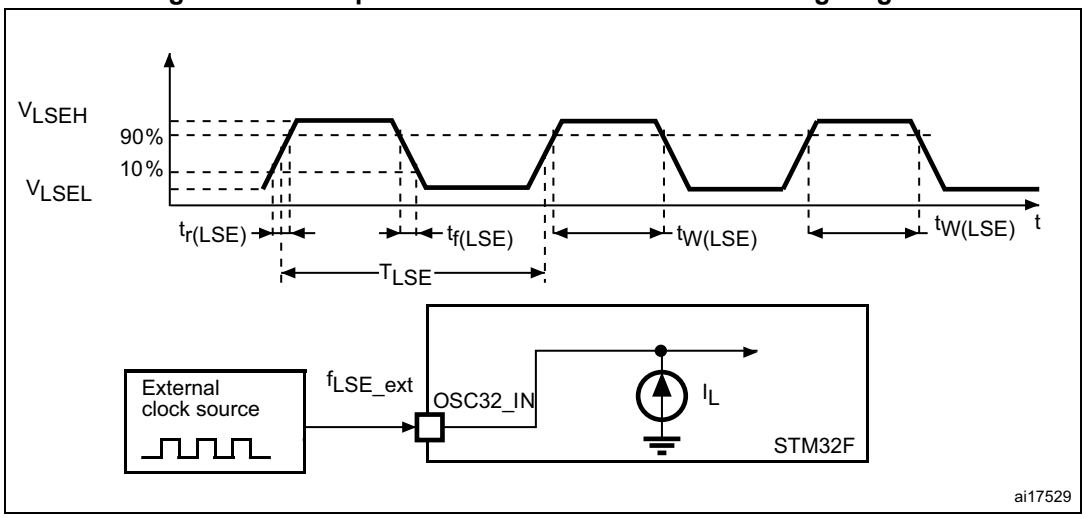


Figure 21. Low-speed external clock source AC timing diagram



5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms

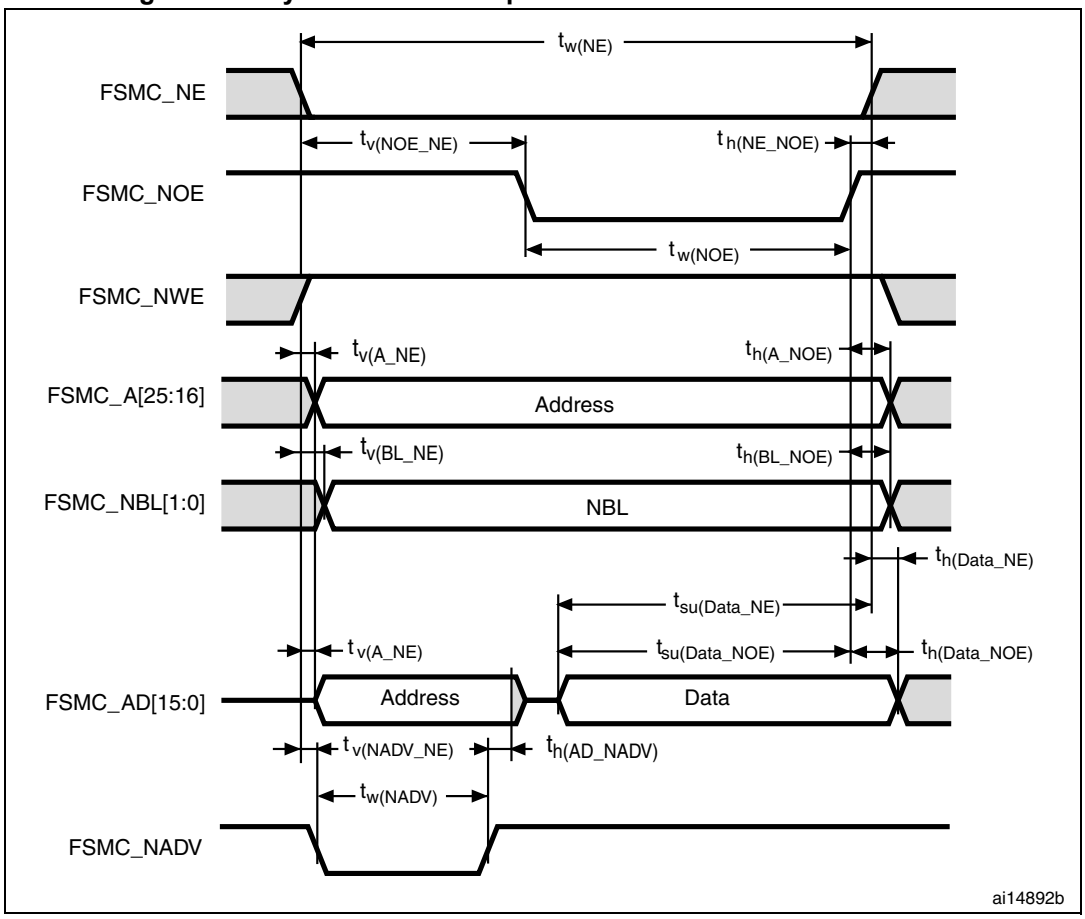


Table 33. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

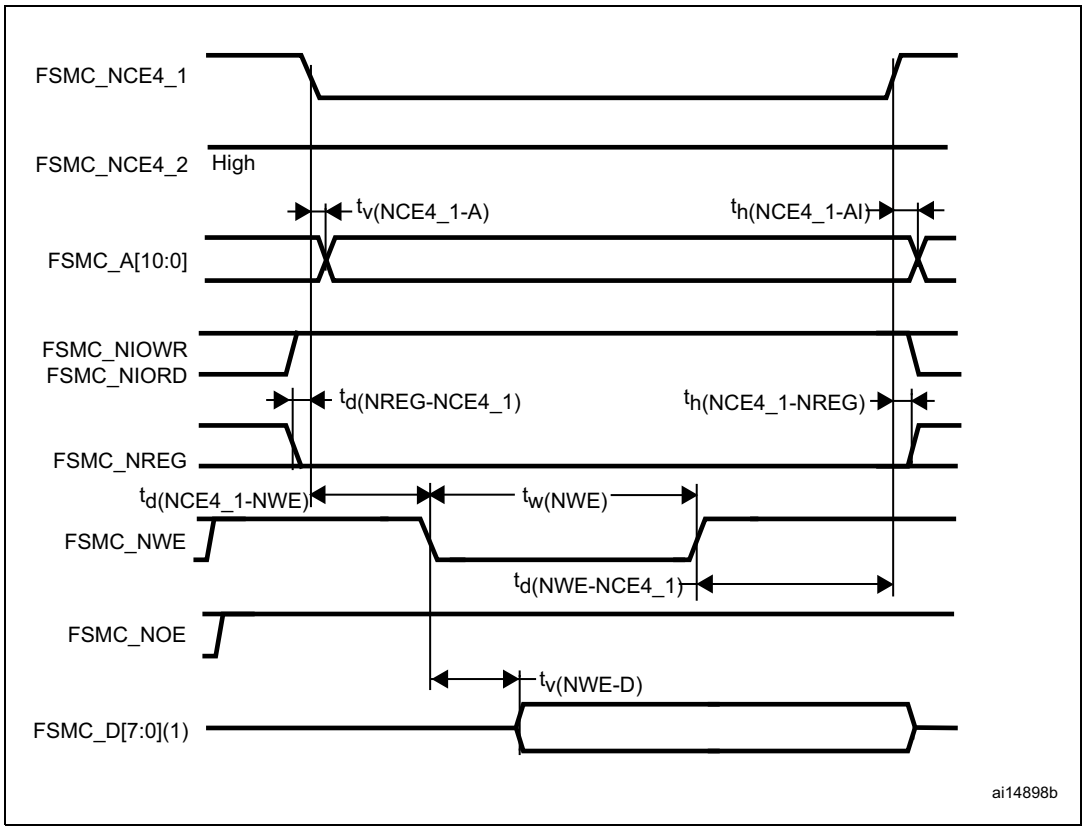
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK} – 2$	$7t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} – 0.5$	$3t_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK} – 1$	$4t_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} –1.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} -2	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 24$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2t_{HCLK} + 25$	-	ns

Table 34. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$t_{HCLK} - 3$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4t_{HCLK}$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.6	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 1.5$	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$t_{HCLK} + 1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$t_{HCLK} - 5$	-	ns

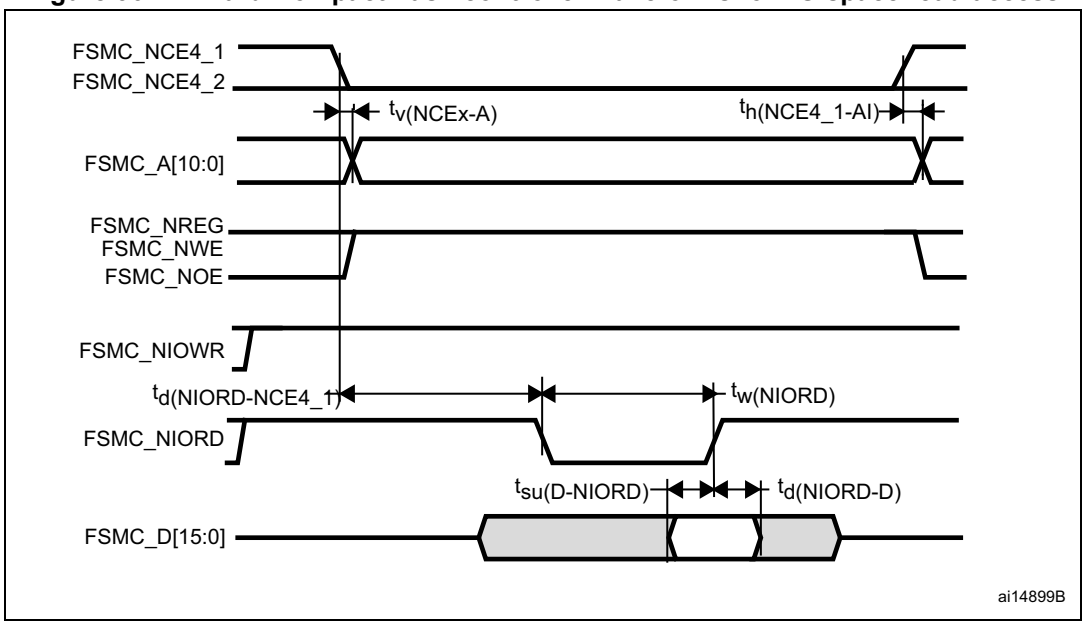
1. C_L = 15 pF.
2. BGuaranteed by characterization results.

Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access



NAND controller waveforms and timings

Figure 38 through *Figure 41* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 38. NAND controller waveforms for read access

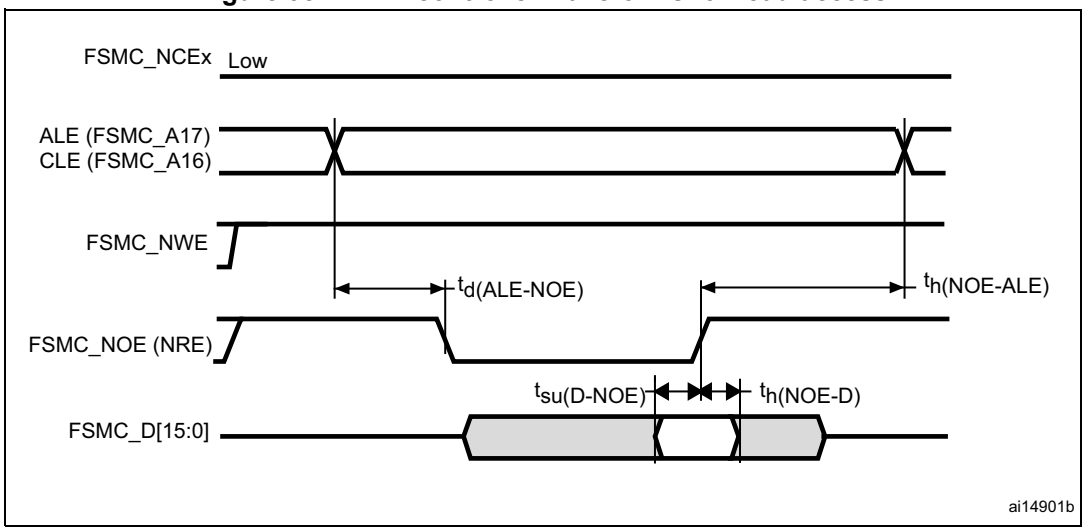


Figure 42. Standard I/O input characteristics - CMOS port

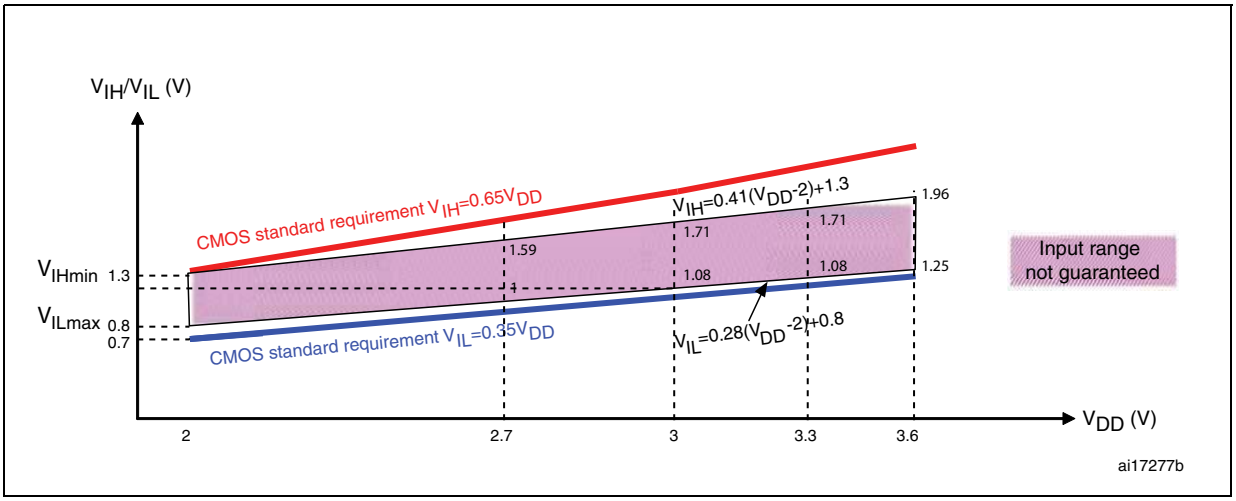


Figure 43. Standard I/O input characteristics - TTL port

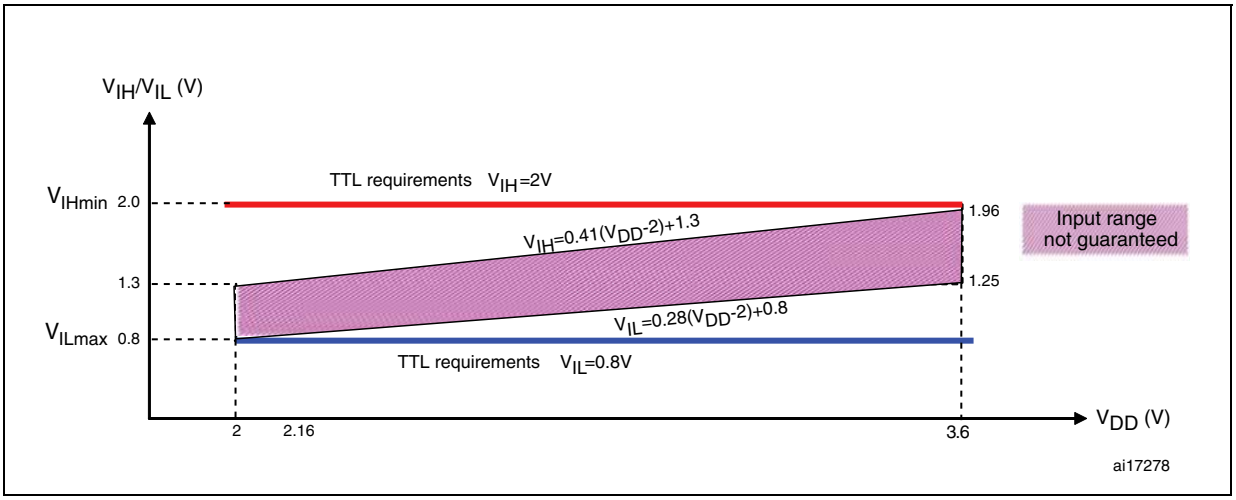


Figure 44. 5 V tolerant I/O input characteristics - CMOS port

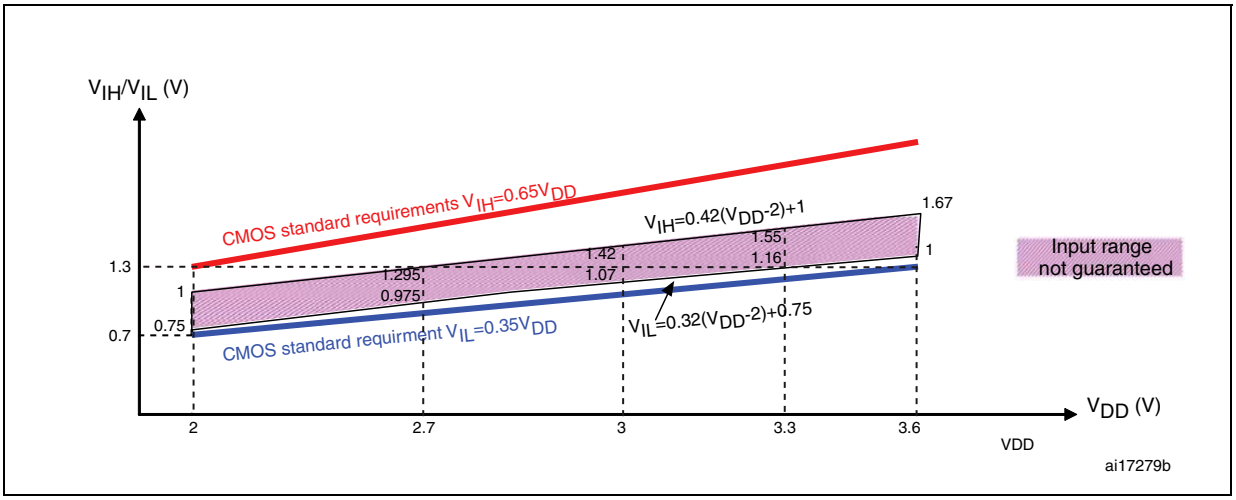
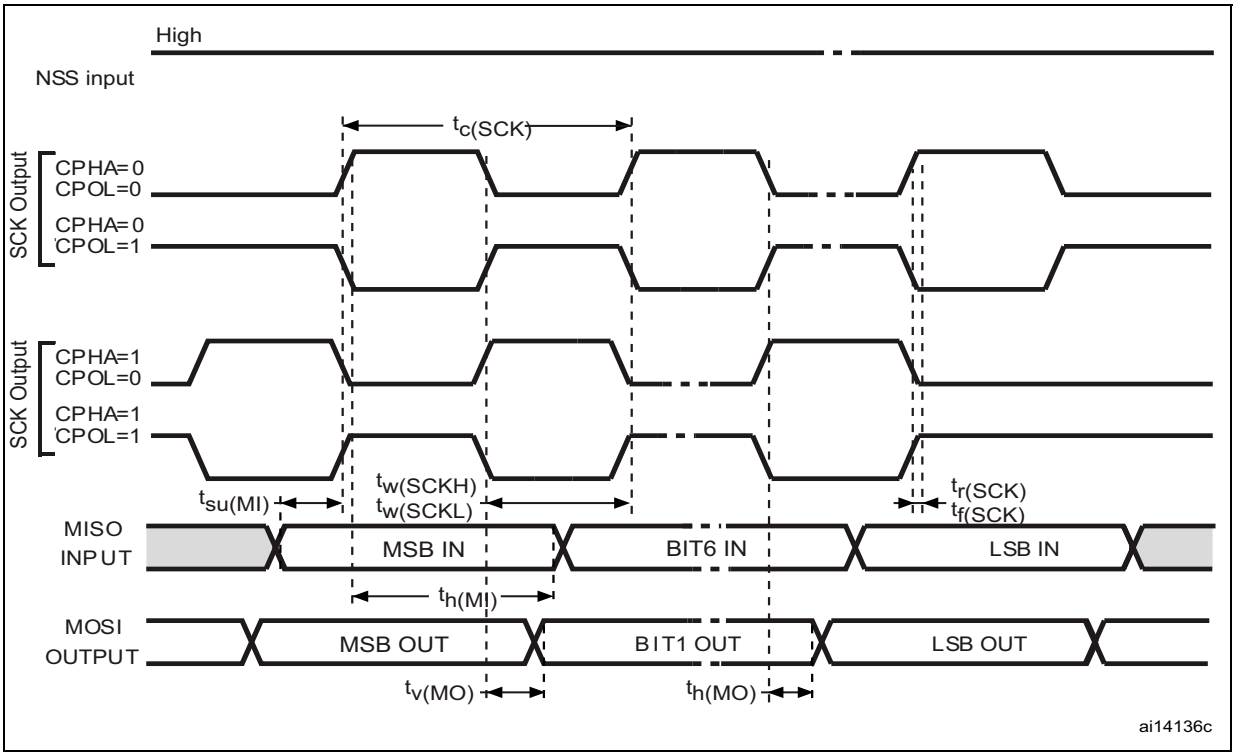


Figure 51. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 54. I^2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)		1.522	1.525	MHz
		Slave mode		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode		4	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
$t_{w(CKH)}$ (1)	CK high and low time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz		312.5	-	
$t_{w(CKL)}$ (1)				345	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	2	-	
			I2S3	6.5	-	
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver		1.5	-	
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver		0	-	
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver		0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)		-	18	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)		11	-	
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)		-	3	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)		0	-	

1. Guaranteed by design and/or characterization results.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.

Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.900	10.000	10.100	0.3898	0.3937	0.3976
D1	-	8.800	-	-	0.3465	-
E	9.900	10.000	10.100	0.3898	0.3937	0.3976
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

Figure 63. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint

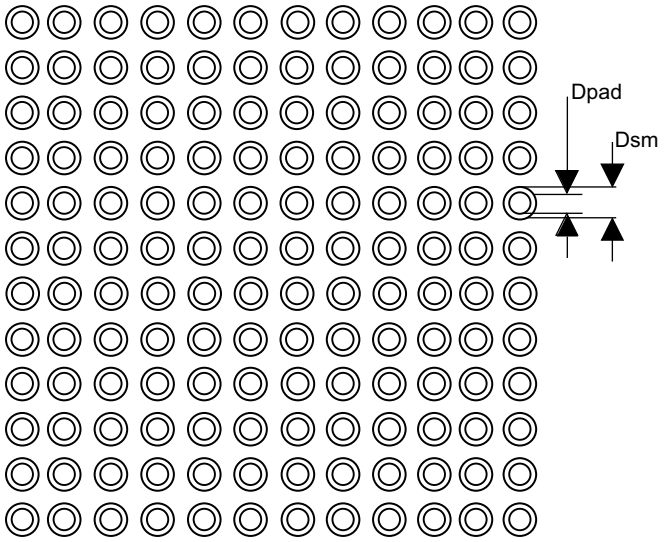


Table 66. LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
UBM	0.350 mm

Table 71. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Using the values obtained in *Table 74* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 75: Ordering information scheme*).

Figure 79. LQFP100 P_D max vs. T_A

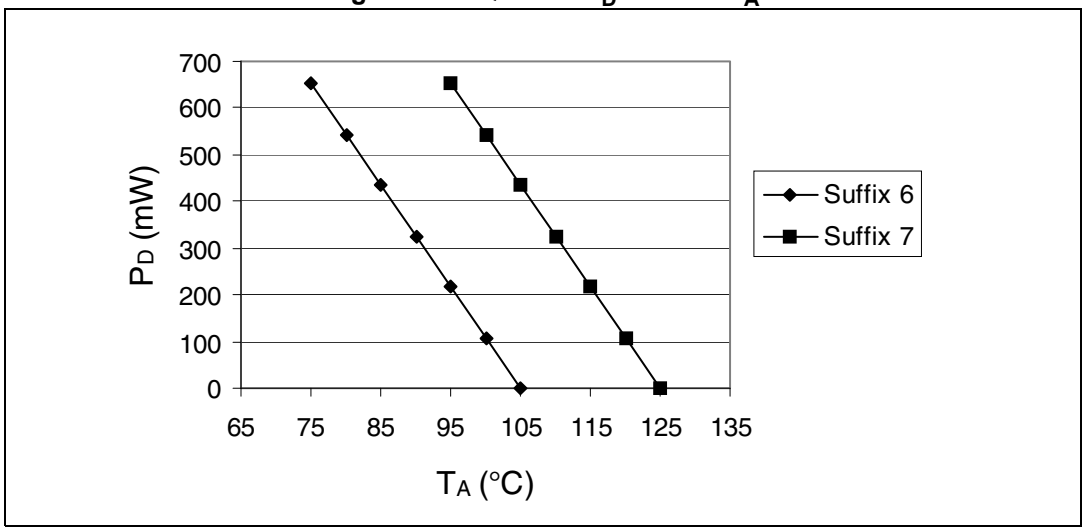


Table 76.Document revision history

Date	Revision	Changes
12-Dec-2008	4	Timers specified *on page 1* (motor control capability mentioned). *Section 2.2: Full compatibility throughout the family* updated. *Table 6: High-density timer feature comparison* added. *General-purpose timers (TIMx)* and *Advanced-control timers (TIM1 and TIM8) on page 27* updated. *Figure 1: STM32F103xF, STM32F103xD and STM32F103xGSTM32F103xF and STM32F103xG performance line block diagram* modified. *Note 10* added, main function after reset and *Note 5 on page 44* updated in *Table 8: High-density STM32F103xx pin definitions*. *Note 2* modified below *Table 11: Voltage characteristics on page 58*, $\|DV_{DDx}\|$ min and $\|DV_{DDx}\|$ min removed. *Note 2* and P_D values for LQFP144 and LFBGA144 packages added to *Table 14: General operating conditions on page 59*. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 62*. Max values at T_A = 85 °C and T_A = 105 °C updated in *Table 21: Typical and maximum current consumptions in Stop and Standby modes on page 68*. *Section 5.3.10: FSMC characteristics on page 87* updated. Data added to *Table 50: EMI characteristics on page 111*. I_{VREF} added to *Table 67: ADC characteristics on page 130*. *Table 81: Package thermal characteristics on page 146* updated. Small text changes.

Table 76.Document revision history

Date	Revision	Changes
19-Apr-2011	8	Updated package choice for 103Rx in *Table 2* Updated footnotes below *Table 7: Voltage characteristics on page 43* and *Table 8: Current characteristics on page 43* Updated tw min in *Table 21: High-speed external user clock characteristics on page 58* Updated startup time in *Table 24: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 61* Updated note 2 in *Table 51: I2C characteristics on page 97* Updated *Figure 48: I2C bus AC waveforms and measurement circuit* Updated *Figure 47: Recommended NRST pin protection* Updated *Section 5.3.14: I/O port characteristics* Updated *Table 35: Synchronous multiplexed NOR/PSRAM read timings on page 73* Updated FSMC *Figure 26* thru *Figure 31* Updated *Figure 41.: NAND controller waveforms for common memory write access* and *Figure 48.: I2C bus AC waveforms and measurement circuit* Added *Section 5.3.13: I/O current injection characteristics* Updated *Figure 67* and added *Table 69: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data on page 121* LQFP64 package mechanical data updated: see *Figure 73.: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 73: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data on page 130*.
30-Sept-2014	9	Added *Note 7* in *Table 5: High-density STM32F103xC/D/E pin definitions on page 31*. Updated *Note 10* in *Table 5: High-density STM32F103xC/D/E pin definitions on page 31*. Modified *Note 2* in *Table 62: ADC accuracy on page 109* Modified *Note 3* in *Table 62: ADC accuracy on page 109* Modified notes in *Table 51: I2C characteristics on page 97* Updated *Figure 51: SPI timing diagram - master mode(1) on page 101*
23-Feb-2015	10	Updated *Figure 66.: BGA pad footprint*, *Figure 70: LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline*, *Figure 73.: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 74.: LQFP100 recommended footprint*, *Figure 76.: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 77.: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* Added *Figure 72.: LQFP144 marking example (package top view)*, *Figure 75.: LQFP100 marking example (package top view)*, *Figure 78.: LQFP64 marking example (package top view)* Updated *Table 72: LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*