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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

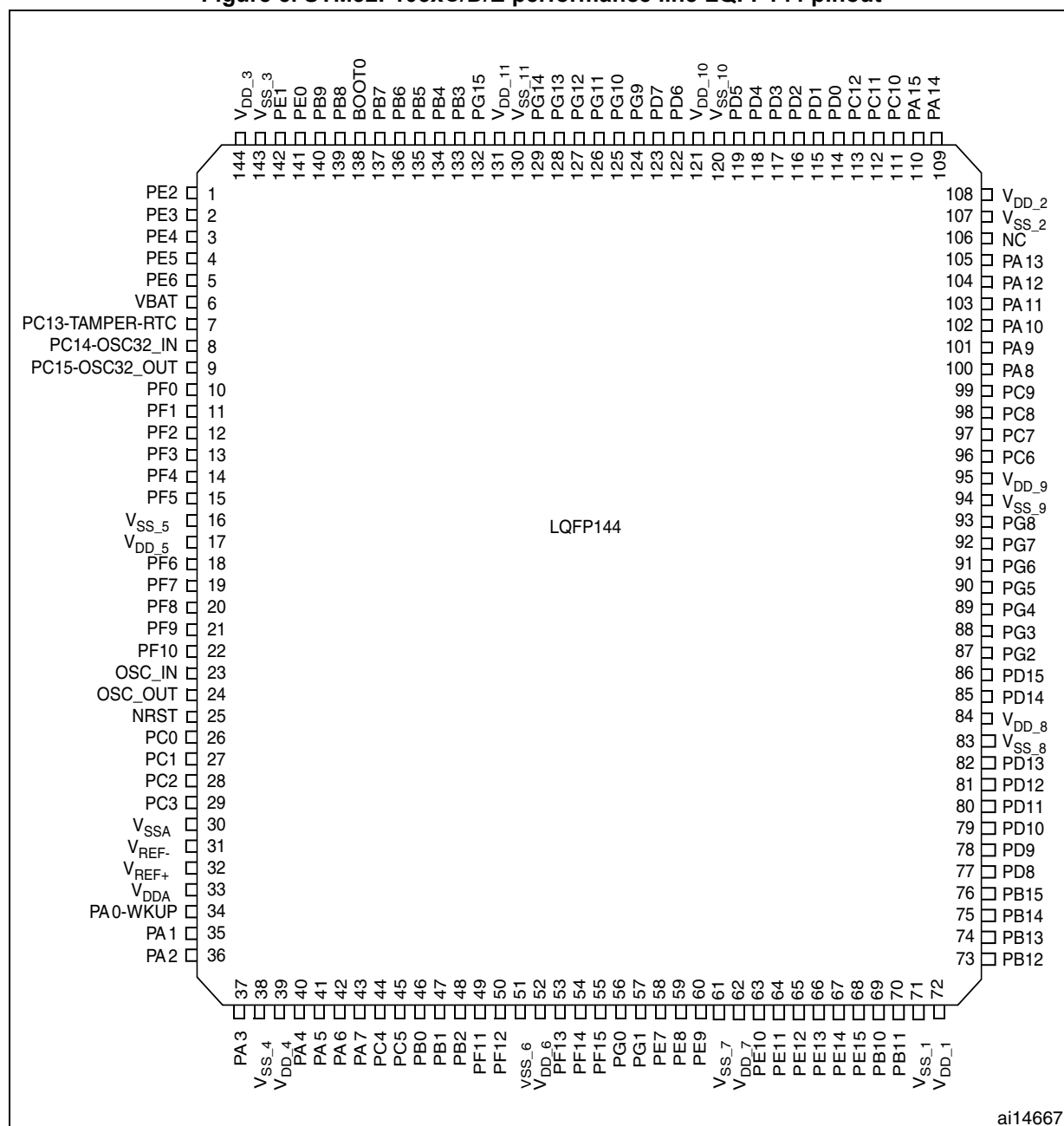
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vdt6

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Figure 5. STM32F103xC/D/E performance line LQFP144 pinout



1. The above figure shows the package top view.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type ⁽¹⁾	I / O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	-
E5	E5	A7	63	99	143	V _{SS_3}	S	-	V _{SS_3}	-	-
F5	F5	A8	64	100	144	V _{DD_3}	S	-	V _{DD_3}	-	-

1. I = input, O = output, S = supply.

2. FT = 5 V tolerant.

3. Function availability depends on the chosen device.

4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).

5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

7. In the WCLSP64 package, the PC3 I/O pin is not bonded and it must be configured by software to output mode (Push-pull) and writing 0 to the data register in order to avoid an extra consumption during low-power modes.

8. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V_{REF+} functionality is provided instead.

9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

10. For the WCLSP64/LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

11. For devices delivered in LQFP64 packages, the FSMC function is not available.

5.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 11](#) are derived from tests performed under the ambient temperature condition summarized in [Table 10](#).

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	$\mu s/V$
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 12](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 ⁽¹⁾	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}^{(2)}$	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)

When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ ⁽¹⁾		Unit
				All peripherals enabled ⁽²⁾	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock ⁽³⁾	72 MHz	51	30.5	mA
			48 MHz	34.6	20.7	
			36 MHz	26.6	16.2	
			24 MHz	18.5	11.4	
			16 MHz	12.8	8.2	
			8 MHz	7.2	5	
			4 MHz	4.2	3.1	
			2 MHz	2.7	2.1	
			1 MHz	2	1.7	
			500 kHz	1.6	1.4	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45	27	mA
			48 MHz	34	20.1	
			36 MHz	26	15.6	
			24 MHz	17.9	10.8	
			16 MHz	12.2	7.6	
			8 MHz	6.6	4.4	
			4 MHz	3.6	2.5	
			2 MHz	2.1	1.5	
			1 MHz	1.4	1.1	
			500 kHz	1	0.8	
			125 kHz	0.7	0.6	

1. Typical values are measures at $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$.

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8\text{ MHz}$.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N _{END}	Endurance	T _A = -40 to +85 °C (6 suffix versions) T _A = -40 to +105 °C (7 suffix versions)	10	kcycles
t _{RET}	Data retention	1 kcycle ⁽²⁾ at T _A = 85 °C	30	Years
		1 kcycle ⁽²⁾ at T _A = 105 °C	10	
		10 kcycles ⁽²⁾ at T _A = 55 °C	20	

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

Figure 29. Synchronous multiplexed PSRAM write timings

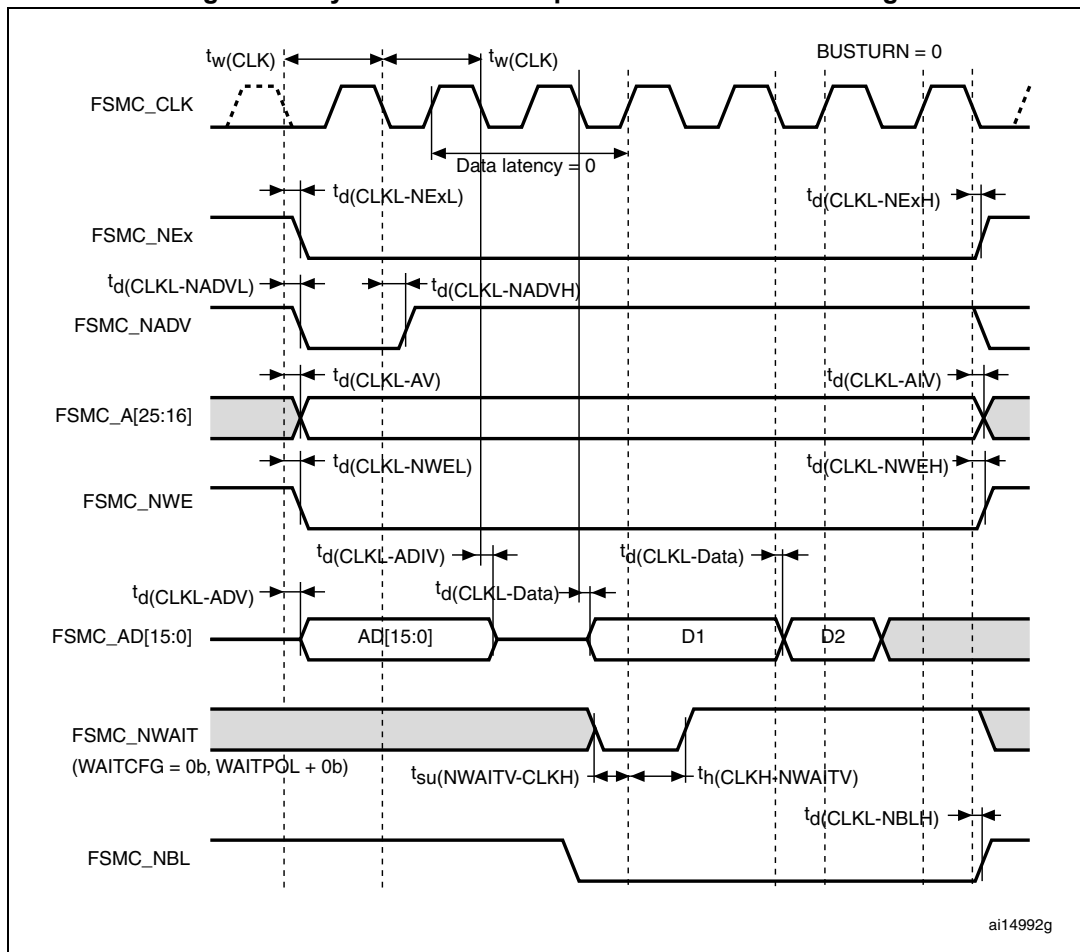


Table 36. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADV_L)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADV_H)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_h(CLKH-NWAITV)$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. $C_L = 15$ pF.

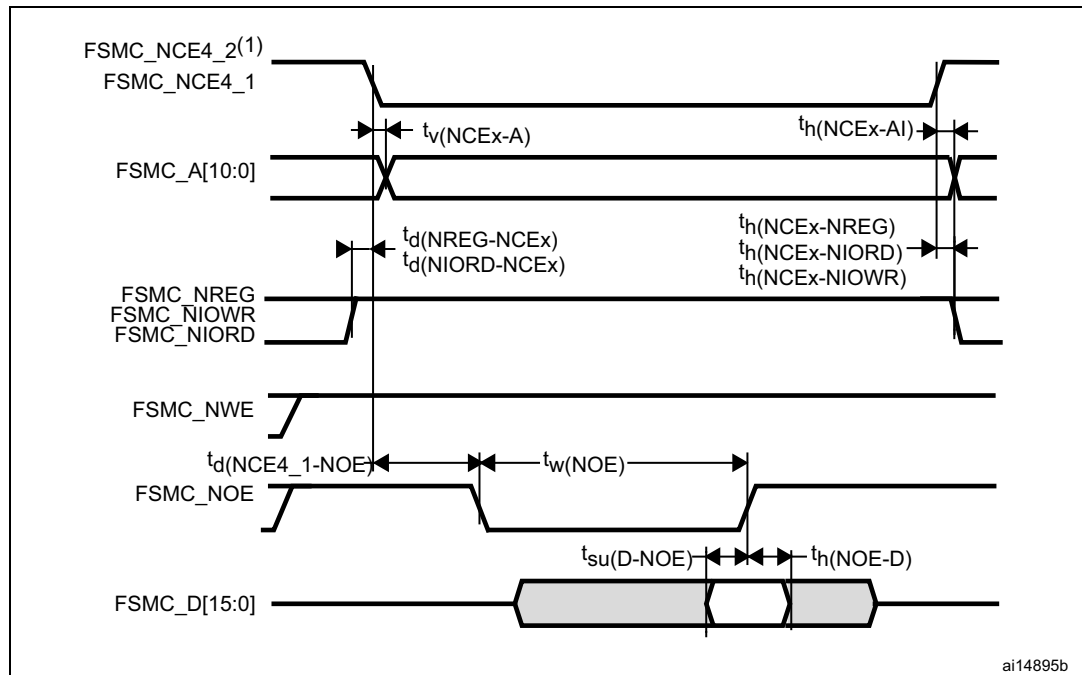
2. Guaranteed by characterization results.

PC Card/CompactFlash controller waveforms and timings

Figure 32 through Figure 37 represent synchronous waveforms and Table 39 provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 32. PC Card/CompactFlash controller waveforms for common memory read access



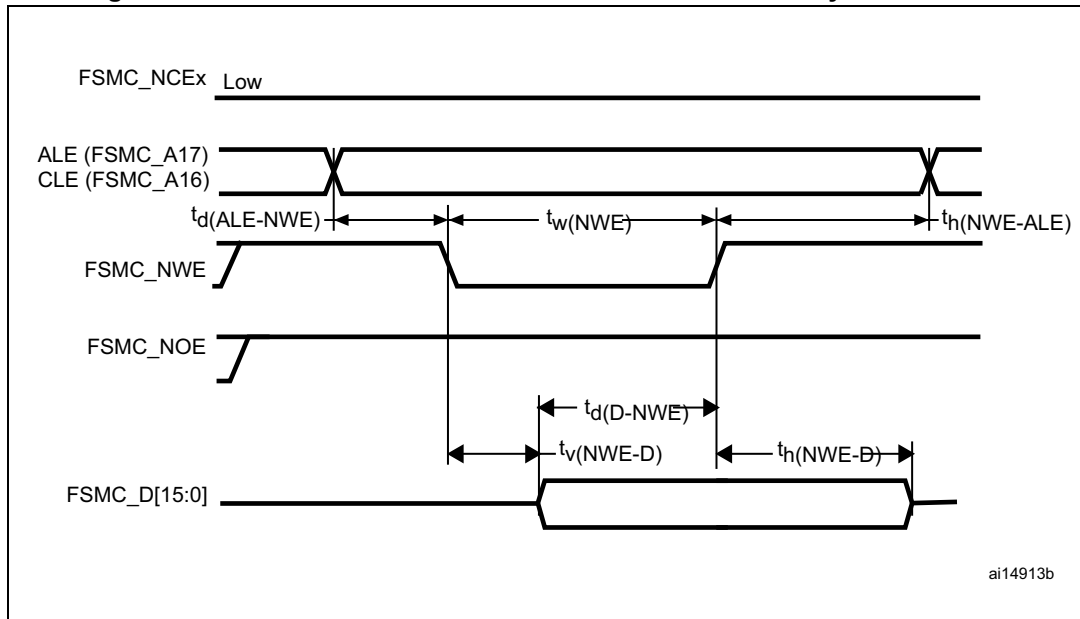
1. FSMC_NCE4_2 remains high (inactive during 8-bit access).

Table 39. Switching characteristics for PC Card/CF read and write cycles⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8t_{HCLK} + 3$	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5t_{HCLK} + 1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5t_{HCLK} + 3ns$	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5t_{HCLK} - 5$	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	$5t_{HCLK} + 2.5$	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5t_{HCLK} - 5$	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8t_{HCLK} + 2$	-	ns

1. $C_L = 15$ pF.

2. Guaranteed by characterization results.

Figure 41. NAND controller waveforms for common memory write access**Table 40. Switching characteristics for NAND Flash read and write cycles⁽¹⁾**

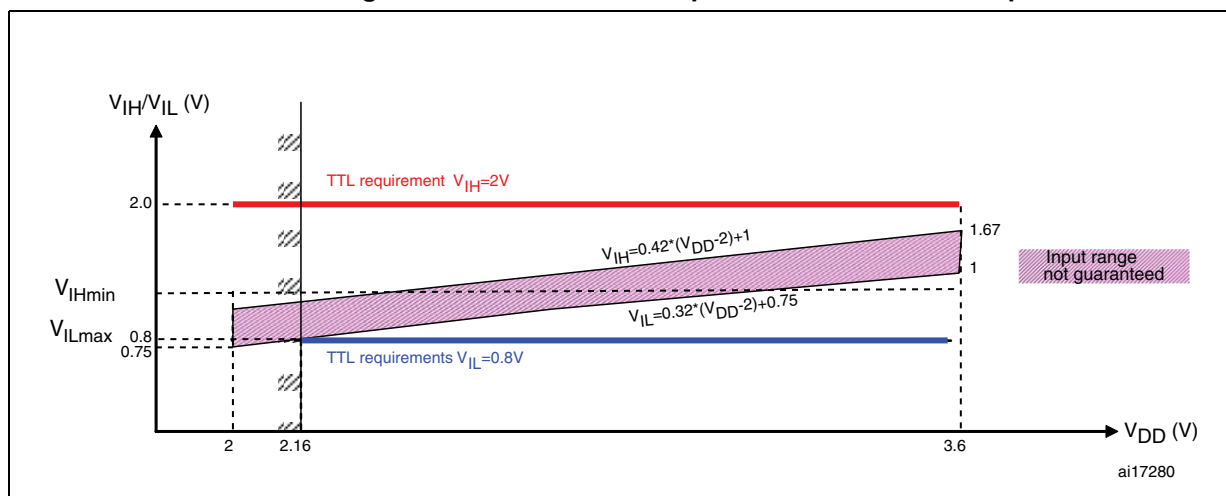
Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}^{(2)}$	FSMC_D[15:0] valid before FSMC_NWE high	$5t_{HCLK} + 12$	-	ns
$t_{w(NOE)}^{(2)}$	FSMC_NWE low width	$4t_{HCLK}-1.5$	$4t_{HCLK}+1.5$	ns
$t_{su(D-NOE)}^{(2)}$	FSMC_D[15:0] valid data before FSMC_NOE high	25	-	ns
$t_{h(NOE-D)}^{(2)}$	FSMC_D[15:0] valid data after FSMC_NOE high	7	-	-
$t_{w(NWE)}^{(2)}$	FSMC_NWE low width	$4t_{HCLK}-1$	$4t_{HCLK}+1$	ns
$t_{v(NWE-D)}^{(2)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}^{(2)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK} + 4$	-	ns
$t_{d(ALE-NWE)}^{(3)}$	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}^{(3)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 4.5$	-	ns
$t_{d(ALE-NOE)}^{(3)}$	FSMC_ALE valid before FSMC_NOE low	-	$3t_{HCLK} + 2$	ns
$t_{h(NOE-ALE)}^{(3)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 4.5$	-	ns

1. $C_L = 15$ pF.

2. Guaranteed by characterization results.

3. Guaranteed by design.

Figure 45. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 8](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 8](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 47](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#). All I/Os are CMOS and TTL compliant.

Table 47. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port ⁽³⁾ $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port ⁽³⁾ $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	

Input/output AC characteristics

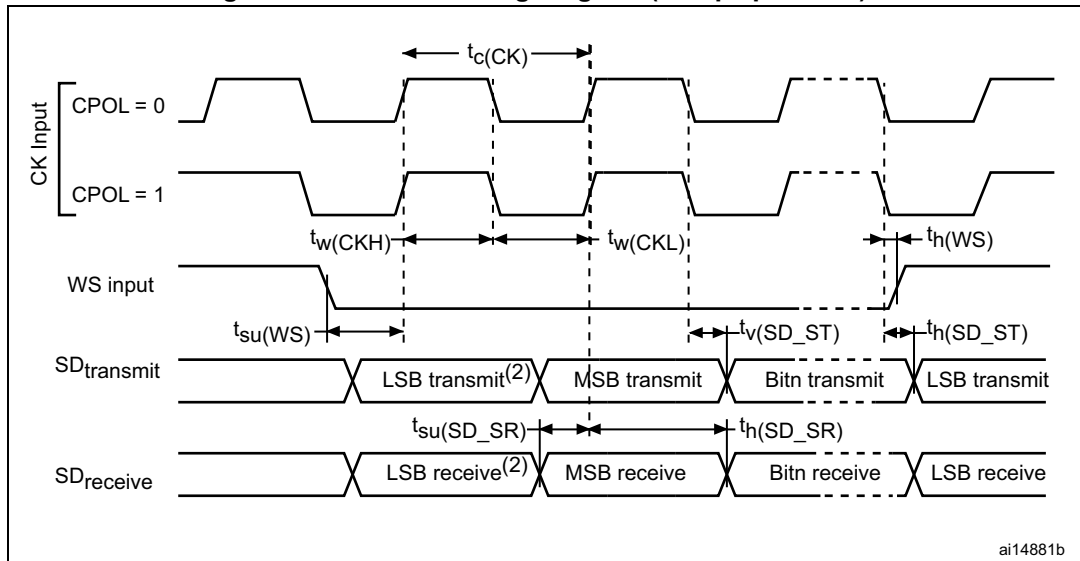
The definition and values of input/output AC characteristics are given in [Figure 46](#) and [Table 48](#), respectively.

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

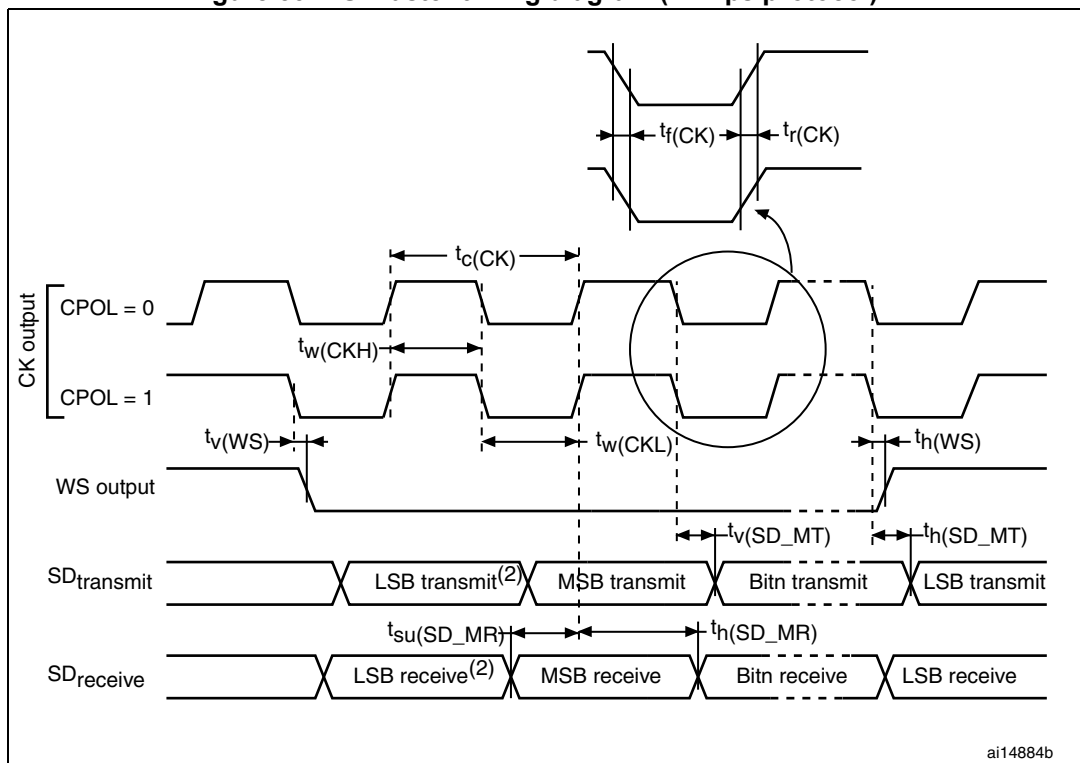
Table 48. I/O AC characteristics⁽¹⁾

MODEx[1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	125 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	125 ⁽³⁾	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	10	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	25 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	25 ⁽³⁾	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	50	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	30	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	20	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5 ⁽³⁾	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	12 ⁽³⁾	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	12 ⁽³⁾	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 46](#).
3. Guaranteed by design.

Figure 52. I²S slave timing diagram (Philips protocol)⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 53. I²S master timing diagram (Philips protocol)⁽¹⁾

1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 55. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t _{ISU}	Input setup time	C _L ≤ 30 pF	2	-	ns
t _{IH}	Input hold time	C _L ≤ 30 pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t _{OV}	Output valid time	C _L ≤ 30 pF	-	6	ns
t _{OH}	Output hold time	C _L ≤ 30 pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode ⁽¹⁾					
t _{OVD}	Output valid default time	C _L ≤ 30 pF	-	7	ns
t _{OHD}	Output hold default time	C _L ≤ 30 pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 56. USB startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB transceiver startup time	1	μs

1. Guaranteed by design.

5.3.18 CAN (controller area network) interface

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 10](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Current on the V_{REF} input pin	-	-	160 ⁽¹⁾	220	μ A
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_S^{(2)}$	Sampling rate	-	0.05	-	1	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 14$ MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range ⁽³⁾	-	0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
$R_{AIN}^{(2)}$	External input impedance	See Equation 1 and Table 60 for details	-	-	50	$\kappa\Omega$
$R_{ADC}^{(2)}$	Sampling switch resistance	-	-	-	1	$\kappa\Omega$
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{CAL}^{(2)}$	Calibration time	$f_{ADC} = 14$ MHz	5.9			μ s
		-	83			$1/f_{ADC}$
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.214	μ s
		-	-	-	3 ⁽⁴⁾	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.143	μ s
		-	-	-	2 ⁽⁴⁾	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 14$ MHz	0.107	-	17.1	μ s
		-	1.5	-	239.5	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time	-	0	0	1	μ s
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 14$ MHz	1	-	18	μ s
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

5.3.20 DAC electrical specifications

Table 63. DAC characteristics

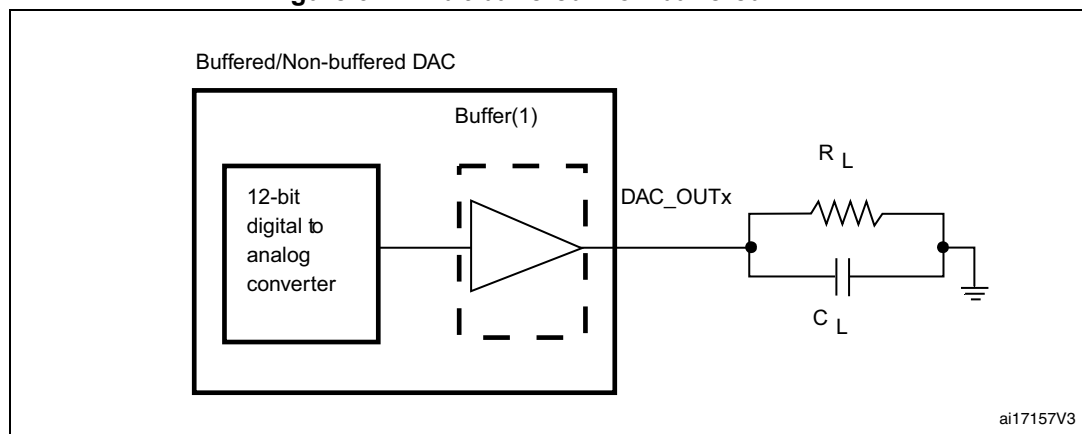
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
$R_{LOAD}^{(1)}$	Resistive load with buffer ON	5	-	-	k Ω	-
$R_O^{(2)}$	Impedance output with buffer OFF	-	-	15	k Ω	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
$C_{LOAD}^{(1)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
$DAC_OUT_{min}^{(1)}$	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x155) and (0xEAB) at $V_{REF+} = 2.4$ V
$DAC_OUT_{max}^{(1)}$	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	
$DAC_OUT_{min}^{(1)}$	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
$DAC_OUT_{max}^{(1)}$	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{REF+} - 1LSB$	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	μ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode ⁽³⁾	-	-	380	μ A	With no load, middle code (0x800) on the inputs
		-	-	480	μ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
$DNL^{(4)}$	Differential non linearity Difference between two consecutive code-1LSB)	-	-	± 0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	± 2	LSB	Given for the DAC in 12-bit configuration
$INL^{(3)}$	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	± 1	LSB	Given for the DAC in 10-bit configuration
		-	-	± 4	LSB	Given for the DAC in 12-bit configuration

Table 63. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset ⁽³⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	± 10	mV	-
		-	-	± 3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6$ V
		-	-	± 12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6$ V
Gain error ⁽³⁾	Gain error	-	-	± 0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}^{(3)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ± 1 LSB)	-	3	4	μ s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω
Update rate ⁽³⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω
$t_{WAKEUP}^{(3)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μ s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω input code between lowest and highest possible ones.
PSRR+ ⁽¹⁾	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-67	-40	dB	No R_{LOAD} , $C_{LOAD} = 50$ pF

1. Guaranteed by design.
2. Guaranteed by characterization.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

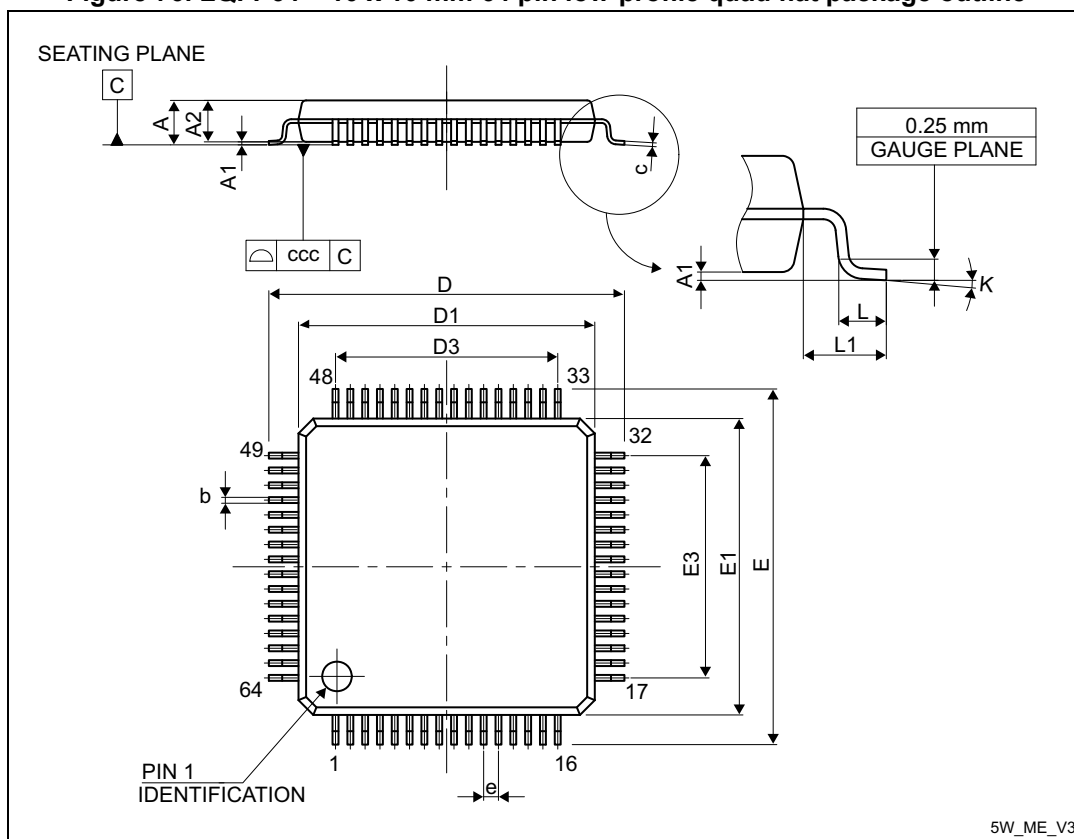
Figure 61. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.6 LQFP64 package information

Figure 76. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 73. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Using the values obtained in [Table 74](#) T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ($-40 < T_J < 125\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 75: Ordering information scheme](#)).

Figure 79. LQFP100 P_D max vs. T_A

