Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vet6

List of figures

1 Introduction

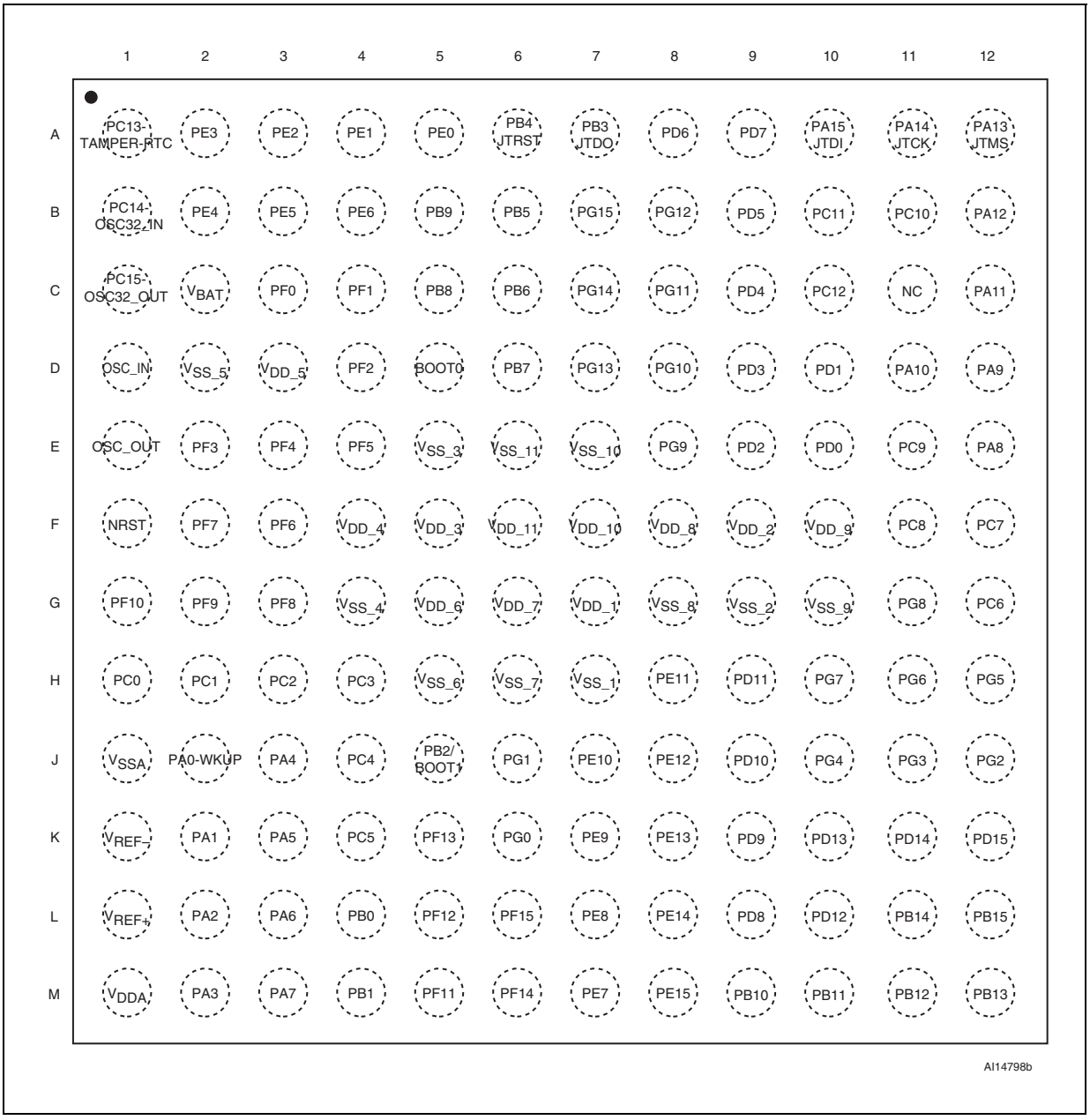
This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xC, STM32F103xD and STM32F103xE high-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xC/D/E family, please refer to *Section 2.2: Full compatibility throughout the family*.

The high-density STM32F103xC/D/E datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website at the following address: *http://infocenter.arm.com*.

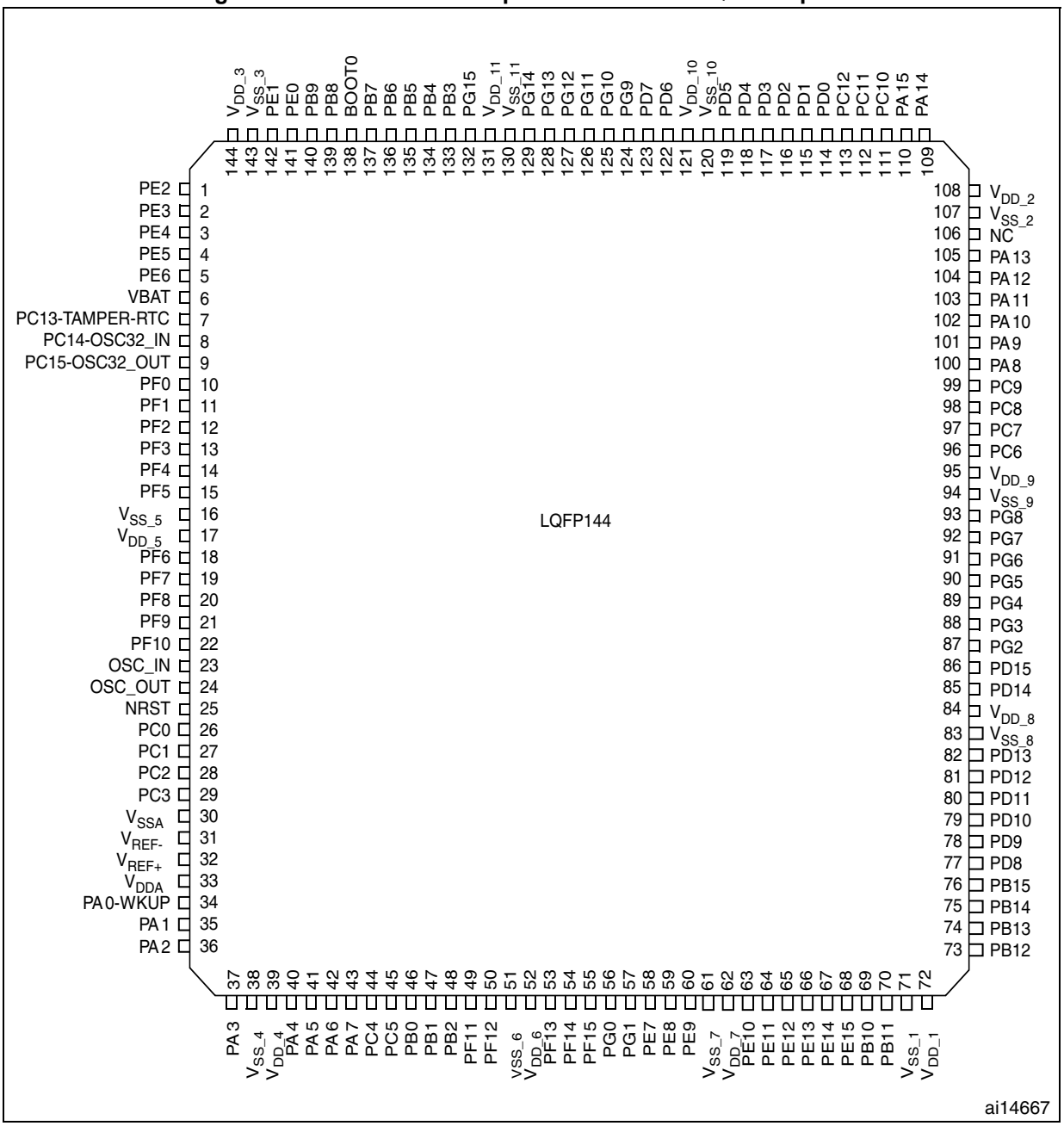
3 Pinouts and pin descriptions

Figure 3. STM32F103xC/D/E BGA144 ballout



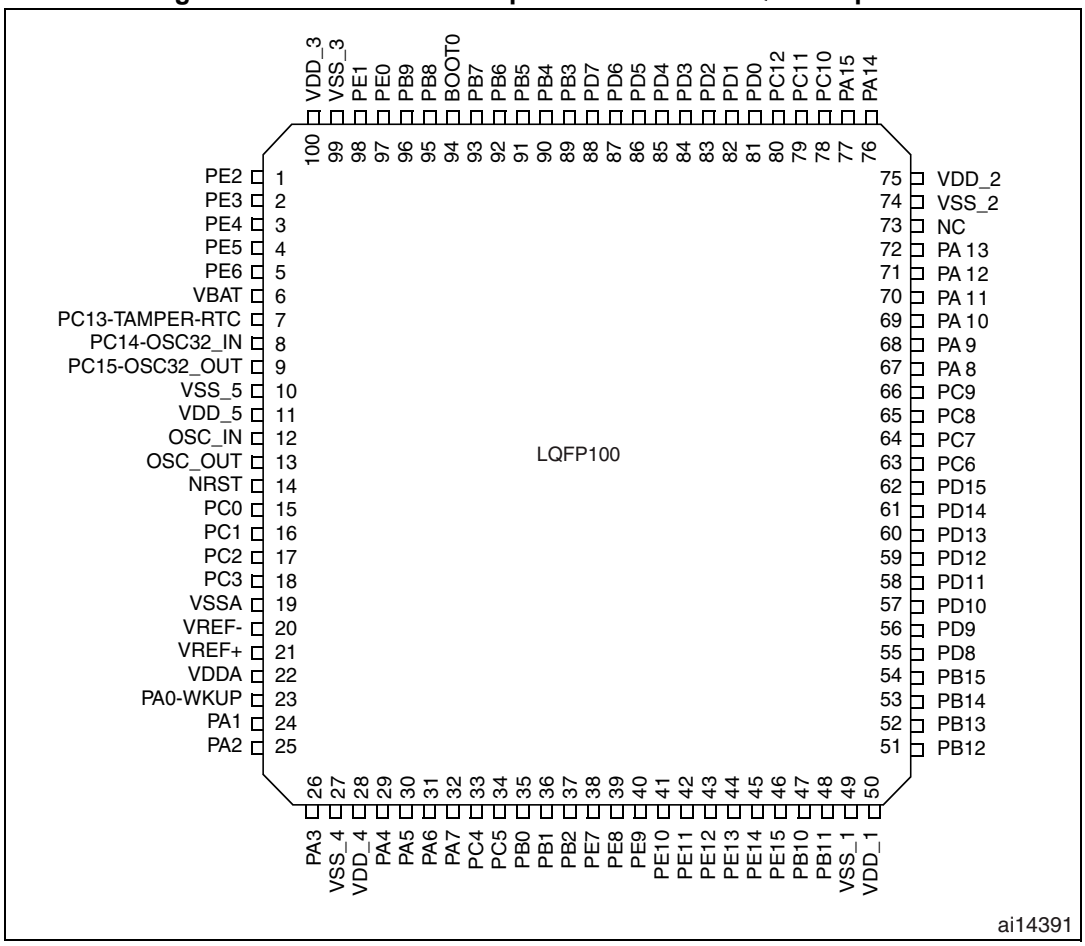
1. The above figure shows the package top view.

Figure 5. STM32F103xC/D/E performance line LQFP144 pinout



1. The above figure shows the package top view.

Figure 6. STM32F103xC/D/E performance line LQFP100 pinout



1. The above figure shows the package top view.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
H3	E2	D6	10	17	28	PC2	I/O	-	PC2	ADC123_IN12	-
H4	F3	-	11	18	29	PC3(7)	I/O	-	PC3	ADC123_IN13	-
J1	G1	E7	12	19	30	V_{SSA}	S	-	V_{SSA}	-	-
K1	H1	-	-	20	31	V_{REF-}	S	-	V_{REF-}	-	-
L1	J1	F7 (8)	-	21	32	V_{REF+}	S	-	V_{REF+}	-	-
M1	K1	G8	13	22	33	V_{DDA}	S	-	V_{DDA}	-	-
J2	G2	F6	14	23	34	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS(9) ADC123_IN0 TIM2_CH1_ETR TIM5_CH1/TIM8_ETR	-
K2	H2	E6	15	24	35	PA1	I/O	-	PA1	USART2_RTS(9) ADC123_IN1/ TIM5_CH2/TIM2_CH2(9)	-
L2	J2	H8	16	25	36	PA2	I/O	-	PA2	USART2_TX(9)/TIM5_CH3 ADC123_IN2/ TIM2_CH3 (9)	-
M2	K2	G7	17	26	37	PA3	I/O	-	PA3	USART2_RX(9)/TIM5_CH4 ADC123_IN3/TIM2_CH4(9)	-
G4	E4	F5	18	27	38	V_{SS_4}	S	-	V_{SS_4}	-	-
F4	F4	G6	19	28	39	V_{DD_4}	S	-	V_{DD_4}	-	-
J3	G3	H7	20	29	40	PA4	I/O	-	PA4	SPI1_NSS(9)/ USART2_CK(9) DAC_OUT1/ADC12_IN4	-
K3	H3	E5	21	30	41	PA5	I/O	-	PA5	SPI1_SCK(9) DAC_OUT2 ADC12_IN5	-
L3	J3	G5	22	31	42	PA6	I/O	-	PA6	SPI1_MISO(9) TIM8_BKIN/ADC12_IN6 TIM3_CH1(9)	TIM1_BKIN
M3	K3	G4	23	32	43	PA7	I/O	-	PA7	SPI1_MOSI(9)/ TIM8_CH1N/ADC12_IN7 TIM3_CH2(9)	TIM1_CH1N
J4	G4	H6	24	33	44	PC4	I/O	-	PC4	ADC12_IN14	-
K4	H4	H5	25	34	45	PC5	I/O	-	PC5	ADC12_IN15	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
L4	J4	H4	26	35	46	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	F4	27	36	47	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4(9) TIM8_CH3N	TIM1_CH3N
J5	G5	H3	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	-	-	51	V_{SS_6}	S	-	V_{SS_6}	-	-
G5	-	-	-	-	52	V_{DD_6}	S	-	V_{DD_6}	-	-
K5	-	-	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	H5	-	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	-	-	61	V_{SS_7}	S	-	V_{SS_7}	-	-
G6	-	-	-	-	62	V_{DD_7}	S	-	V_{DD_7}	-	-
J7	G6	-	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	G3	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX(9)	TIM2_CH3
M10	K7	F3	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX(9)	TIM2_CH4
H7	E7	H2	31	49	71	V_{SS_1}	S	-	V_{SS_1}	-	-
G7	F7	H1	32	50	72	V_{DD_1}	S	-	V_{DD_1}	-	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

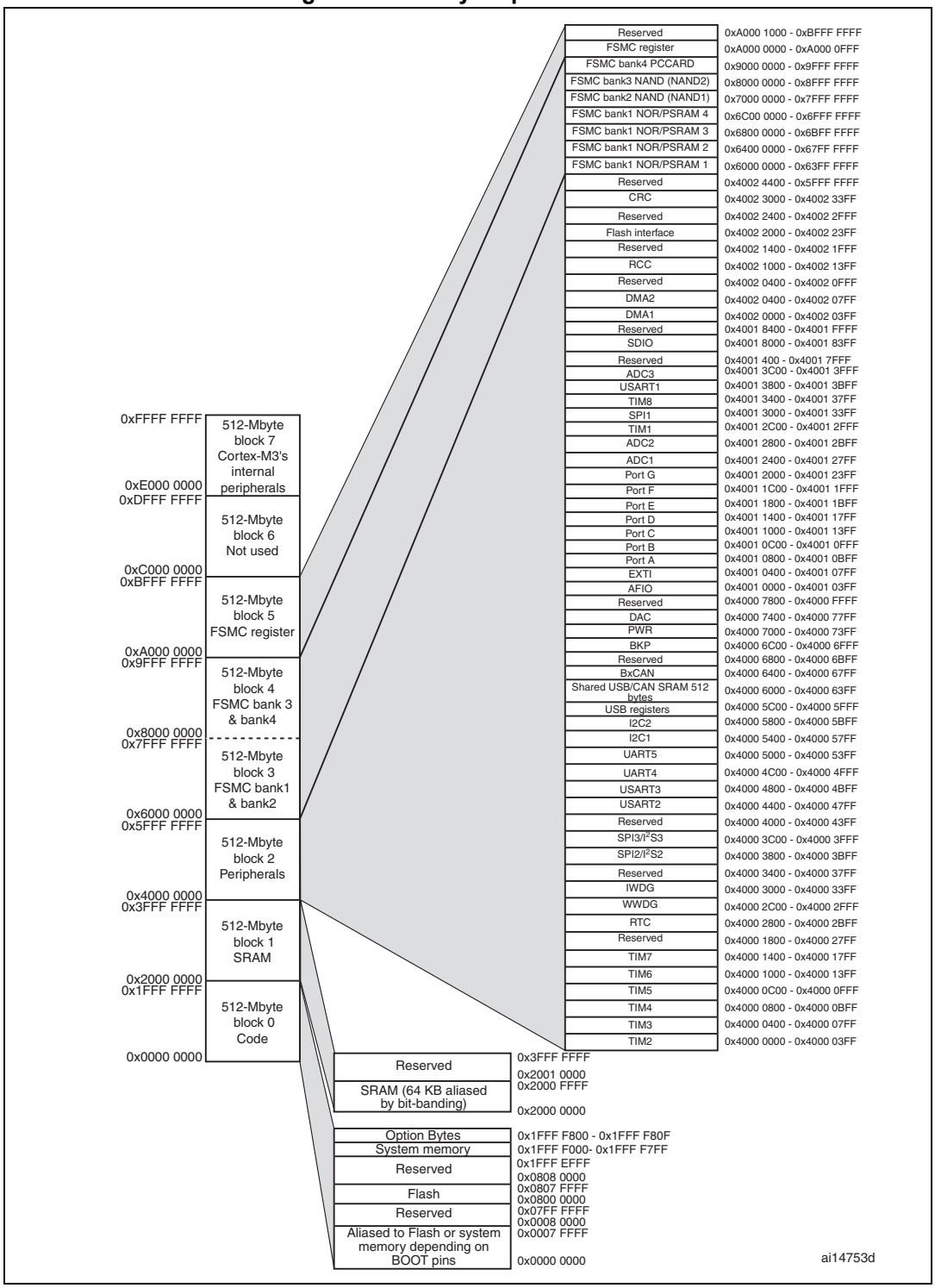
Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	-
E5	E5	A7	63	99	143	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	F5	A8	64	100	144	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. In the WCLSP64 package, the PC3 I/O pin is not bonded and it must be configured by software to output mode (Push-pull) and writing 0 to the data register in order to avoid an extra consumption during low-power modes.
8. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
10. For the WCLSP64/LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
11. For devices delivered in LQFP64 packages, the FSMC function is not available.

4 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



5.3.4 Embedded reference voltage

The parameters given in *Table 13* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 13. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/°C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 14*, *Table 15* and *Table 16* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Figure 20. High-speed external clock source AC timing diagram

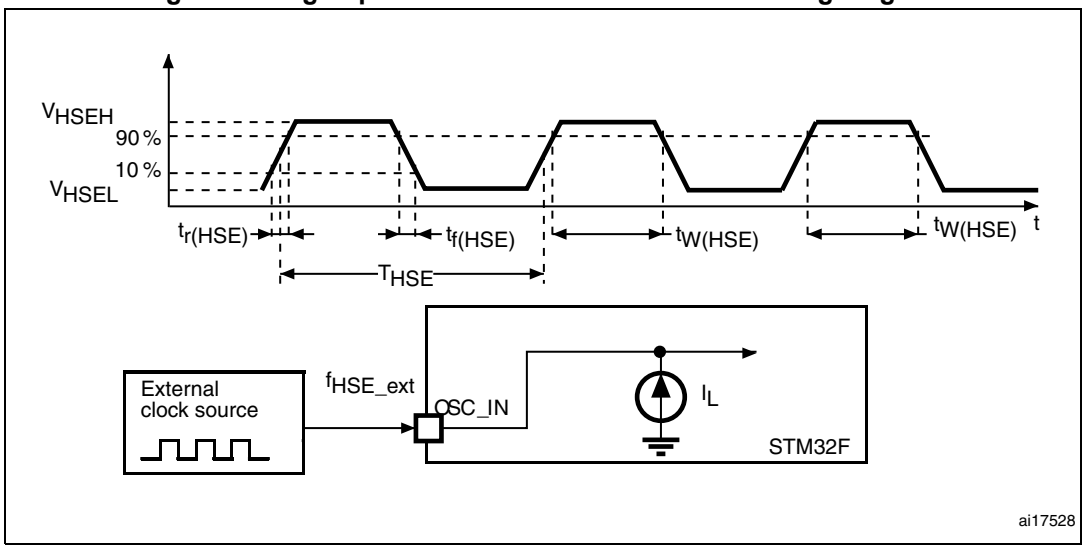


Figure 21. Low-speed external clock source AC timing diagram

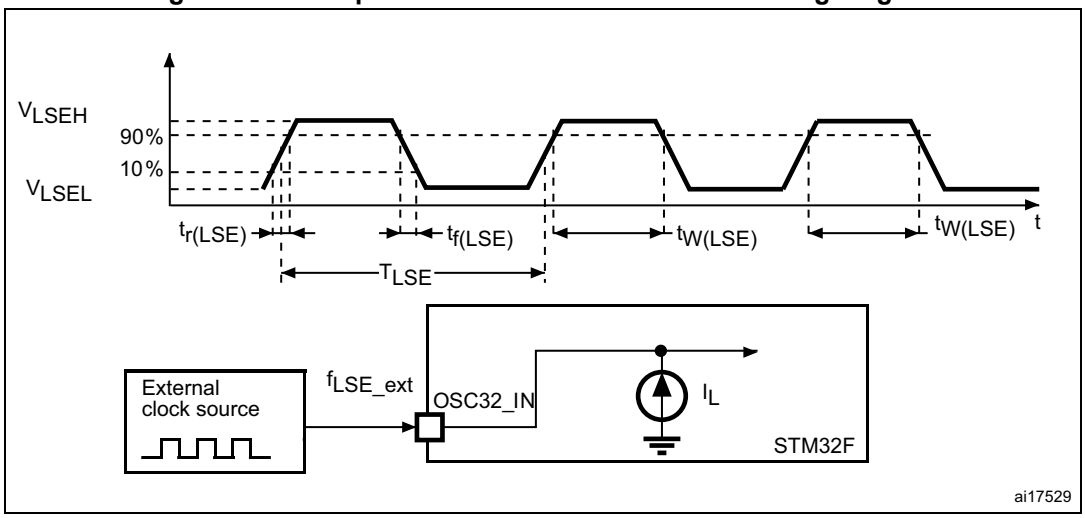
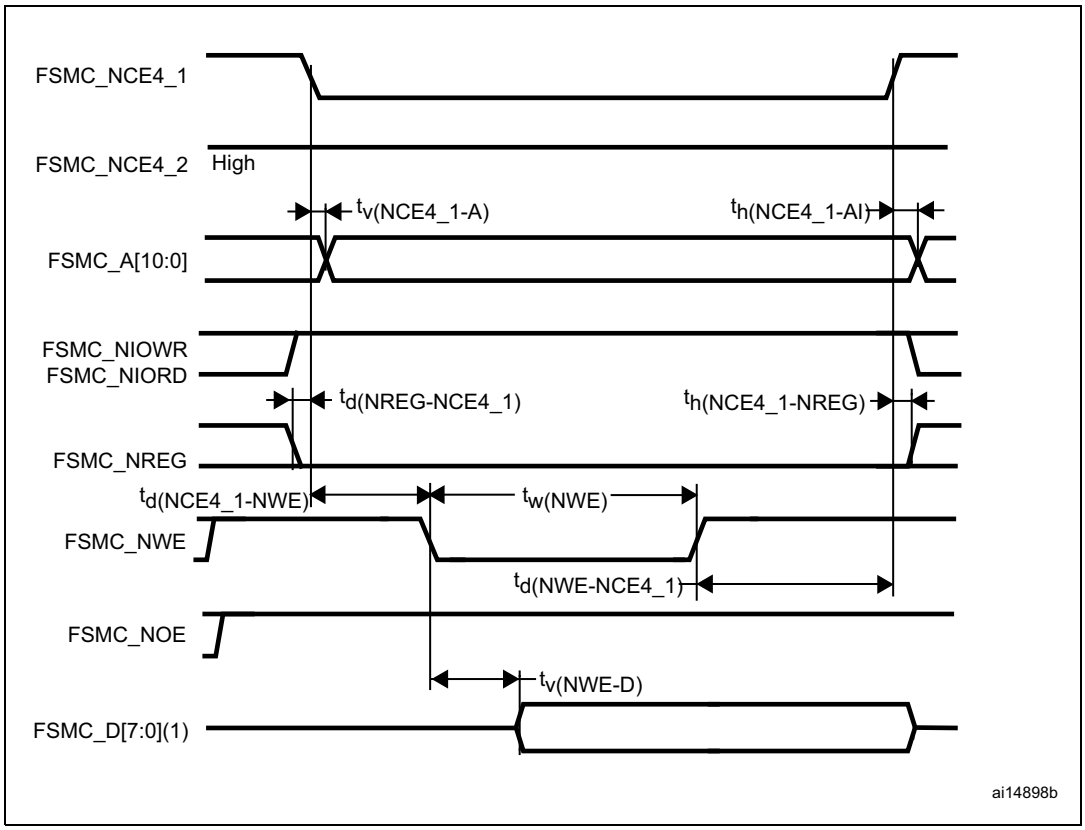
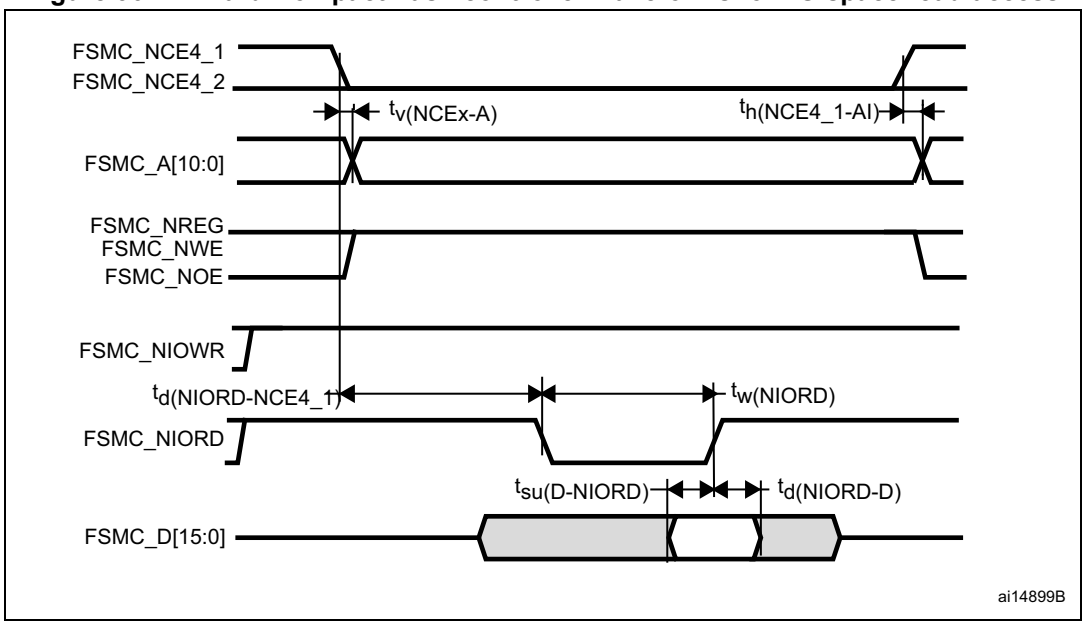


Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access



5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

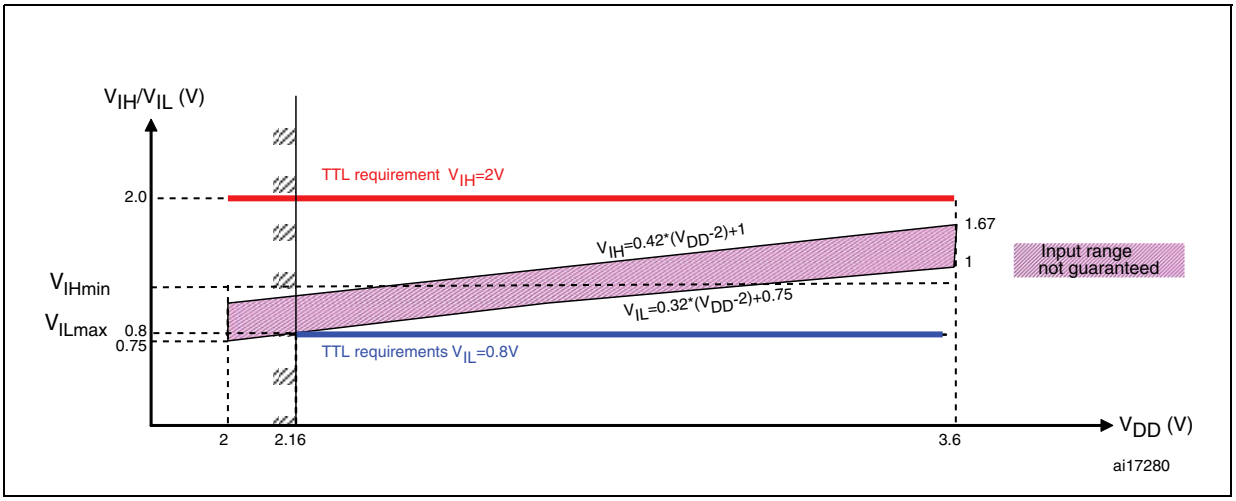
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

Figure 45. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 8*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 8*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 47. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(3) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 46* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 46*.
3. Guaranteed by design.

Figure 49. SPI timing diagram - slave mode and CPHA = 0

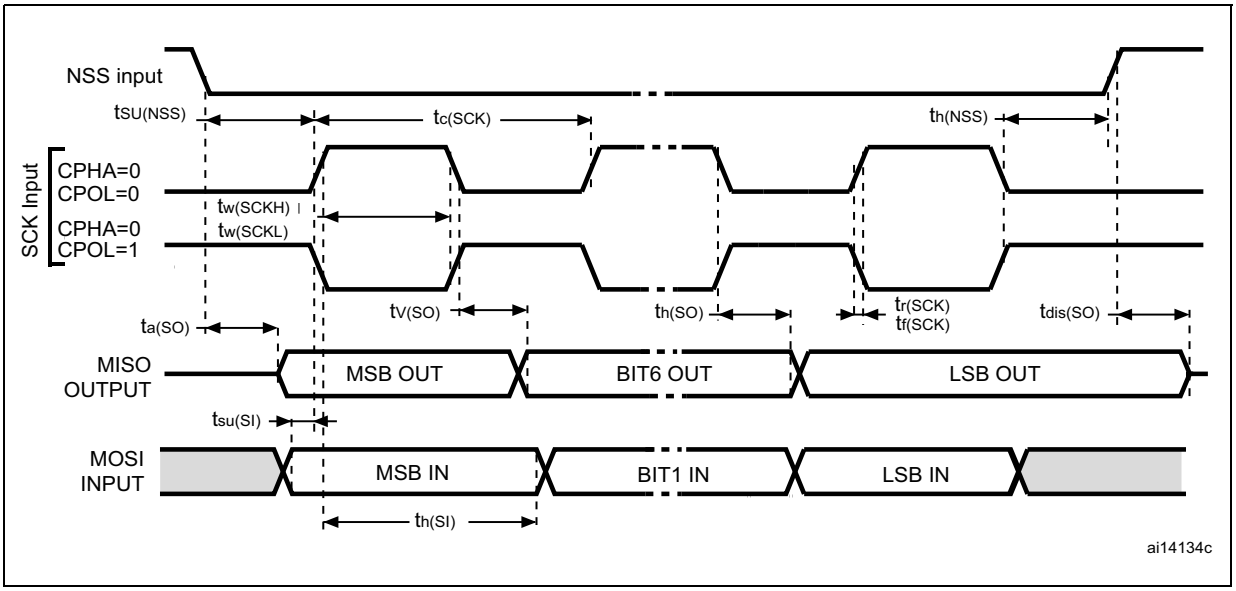
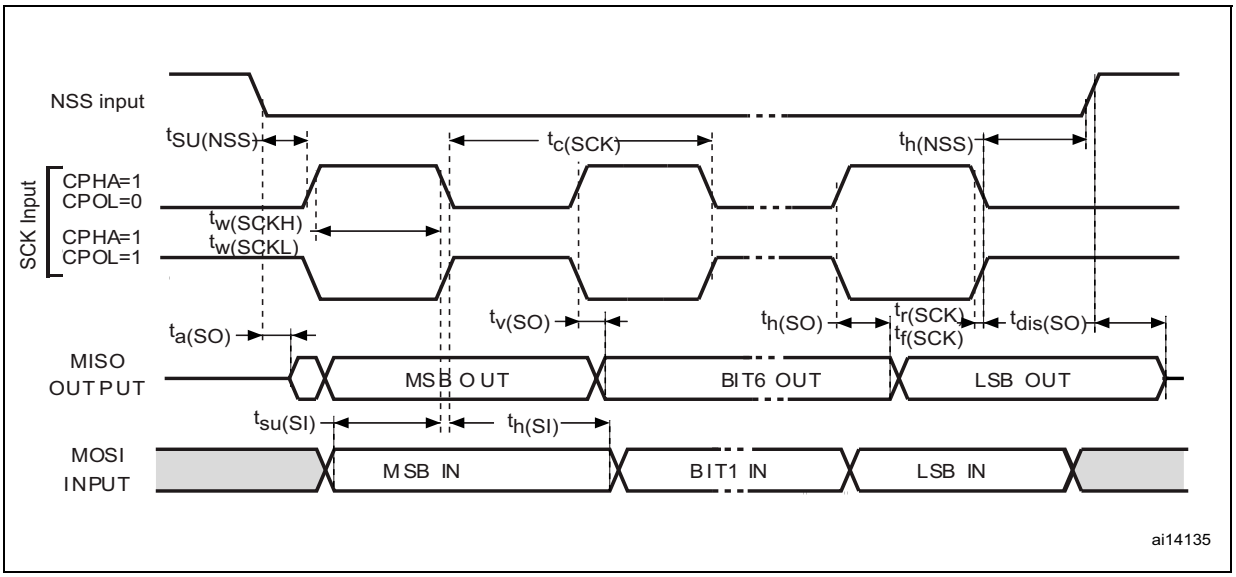
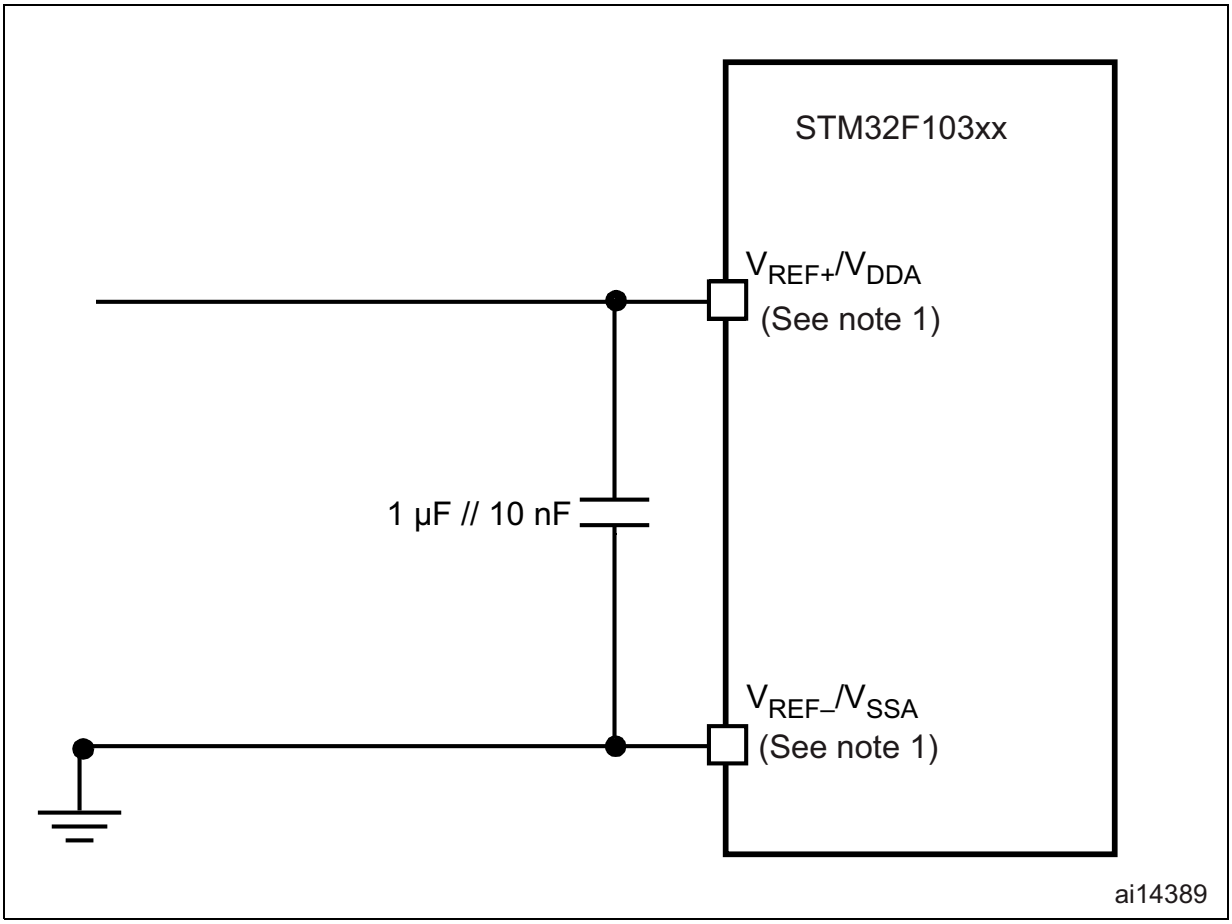


Figure 50. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	9.900	10.000	10.100	0.3898	0.3937	0.3976
D1	-	8.800	-	-	0.3465	-
E	9.900	10.000	10.100	0.3898	0.3937	0.3976
E1	-	8.800	-	-	0.3465	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

Figure 63. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint

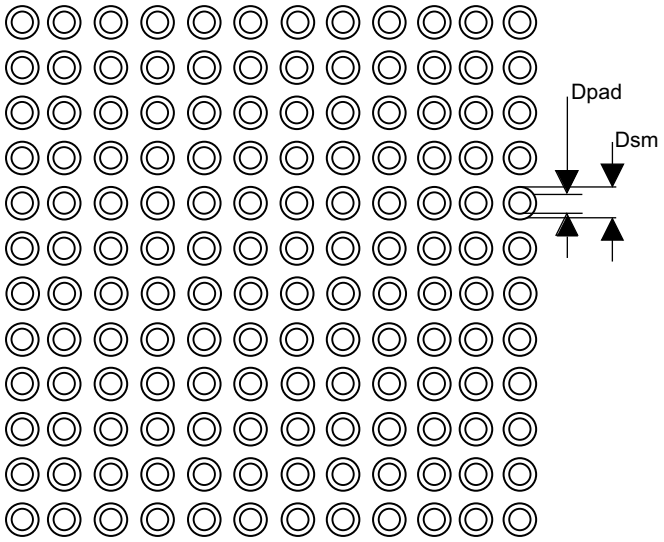
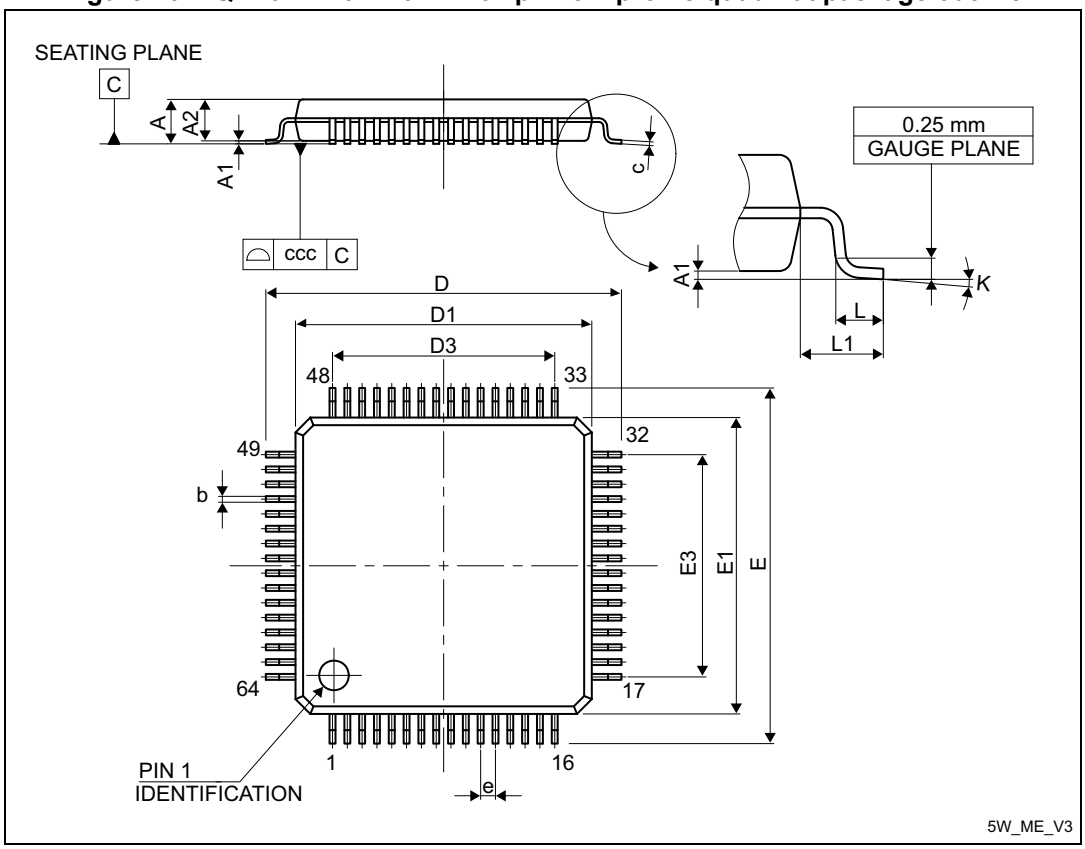


Table 66. LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.400 mm
UBM	0.350 mm

6.6 LQFP64 package information

Figure 76. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

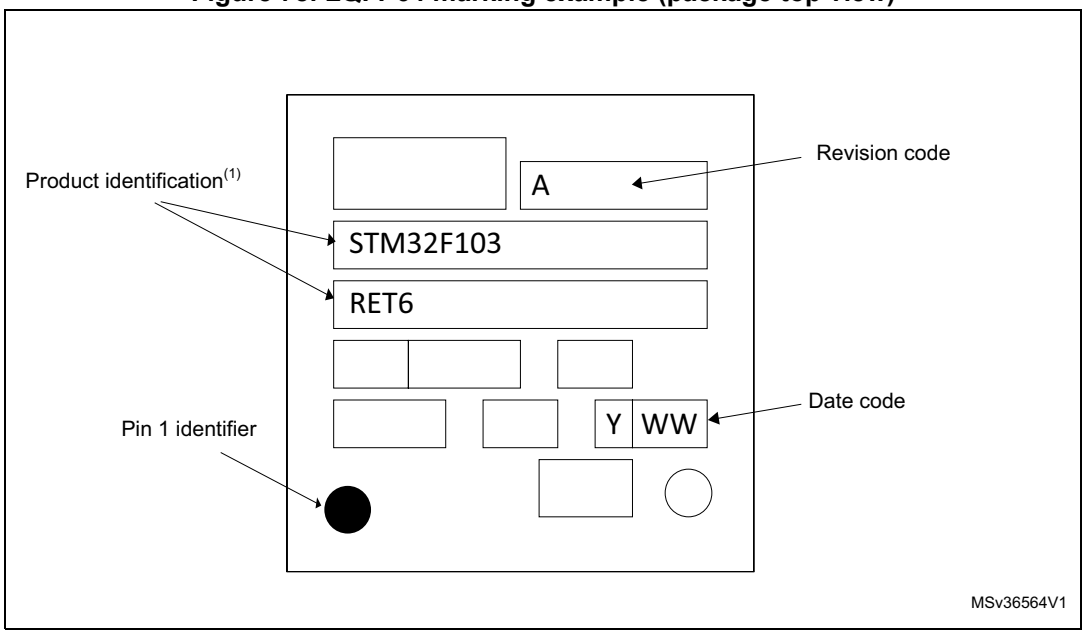
Table 73. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking for LQFP64 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 78. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.