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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vet7

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xC, STM32F103xD and STM32F103xE high-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xC/D/E family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The high-density STM32F103xC/D/E datasheet should be read in conjunction with the STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex[®]-M3 core please refer to the Cortex[®]-M3 Technical Reference Manual, available from the www.arm.com website at the following address:
<http://infocenter.arm.com>.



Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type ⁽¹⁾	I / O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
L4	J4	H4	26	35	46	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	F4	27	36	47	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4 ⁽⁹⁾ TIM8_CH3N	TIM1_CH3N
J5	G5	H3	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	-	-	51	V _{SS_6}	S	-	V _{SS_6}	-	-
G5	-	-	-	-	52	V _{DD_6}	S	-	V _{DD_6}	-	-
K5	-	-	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	H5	-	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	-	-	61	V _{SS_7}	S	-	V _{SS_7}	-	-
G6	-	-	-	-	62	V _{DD_7}	S	-	V _{DD_7}	-	-
J7	G6	-	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	G3	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX ⁽⁹⁾	TIM2_CH3
M10	K7	F3	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX ⁽⁹⁾	TIM2_CH4
H7	E7	H2	31	49	71	V _{SS_1}	S	-	V _{SS_1}	-	-
G7	F7	H1	32	50	72	V _{DD_1}	S	-	V _{DD_1}	-	-

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100 BGA100 ⁽¹⁾
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18	-	Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

The memory map is shown in [Figure 9](#).

Figure 9. Memory map

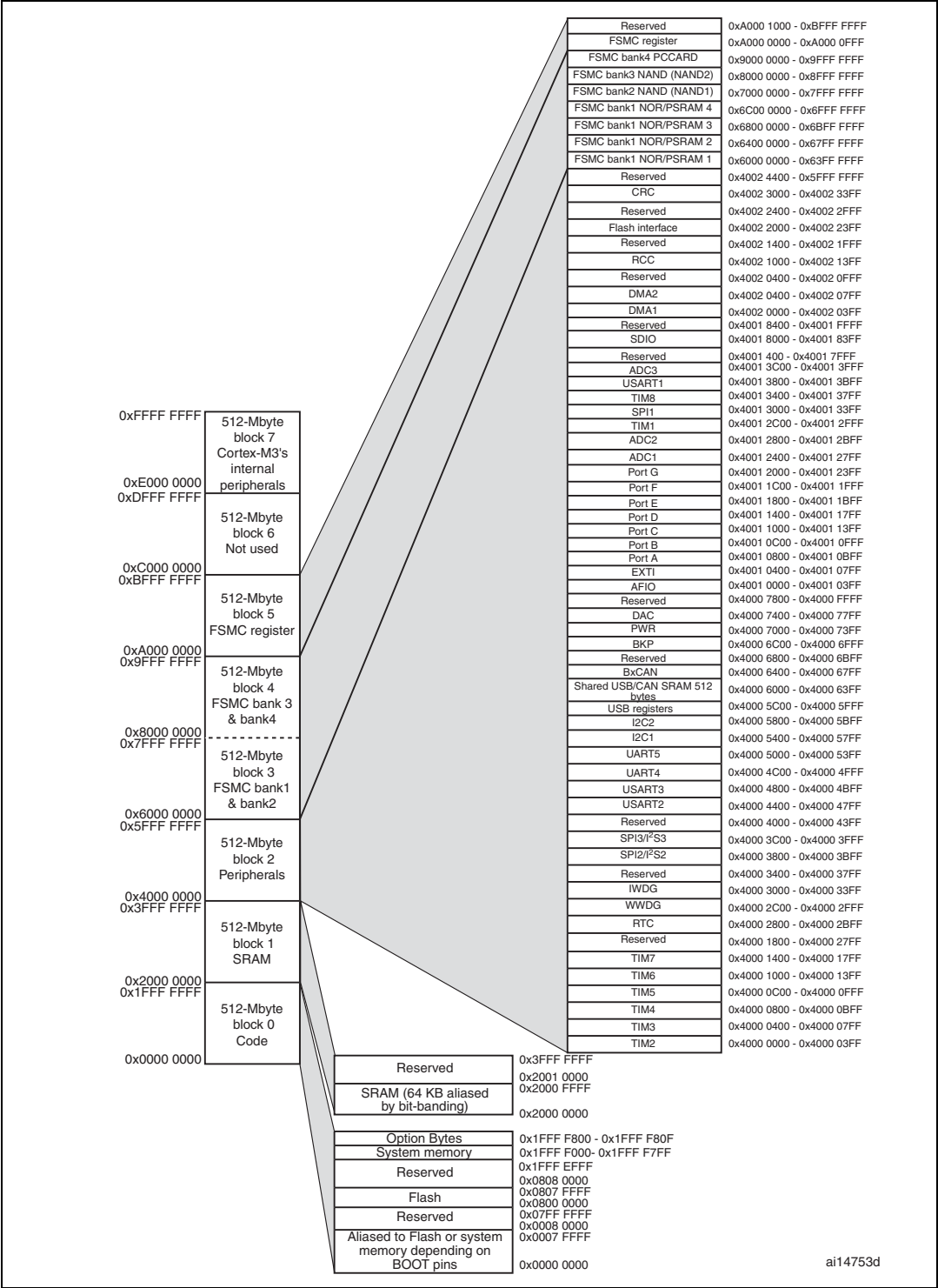


Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ ⁽¹⁾			Max		Unit
			$V_{DD}/V_{BAT} = 2.0\text{ V}$	$V_{DD}/V_{BAT} = 2.4\text{ V}$	$V_{DD}/V_{BAT} = 3.3\text{ V}$	$T_A = 85\text{ }^{\circ}\text{C}$	$T_A = 105\text{ }^{\circ}\text{C}$	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	1130	μA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	1110	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5 ⁽²⁾	6.5 ⁽²⁾	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2 ⁽²⁾	2.3 ⁽²⁾	

1. Typical values are measured at $T_A = 25\text{ }^{\circ}\text{C}$.

2. Guaranteed by characterization results.

Figure 16. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

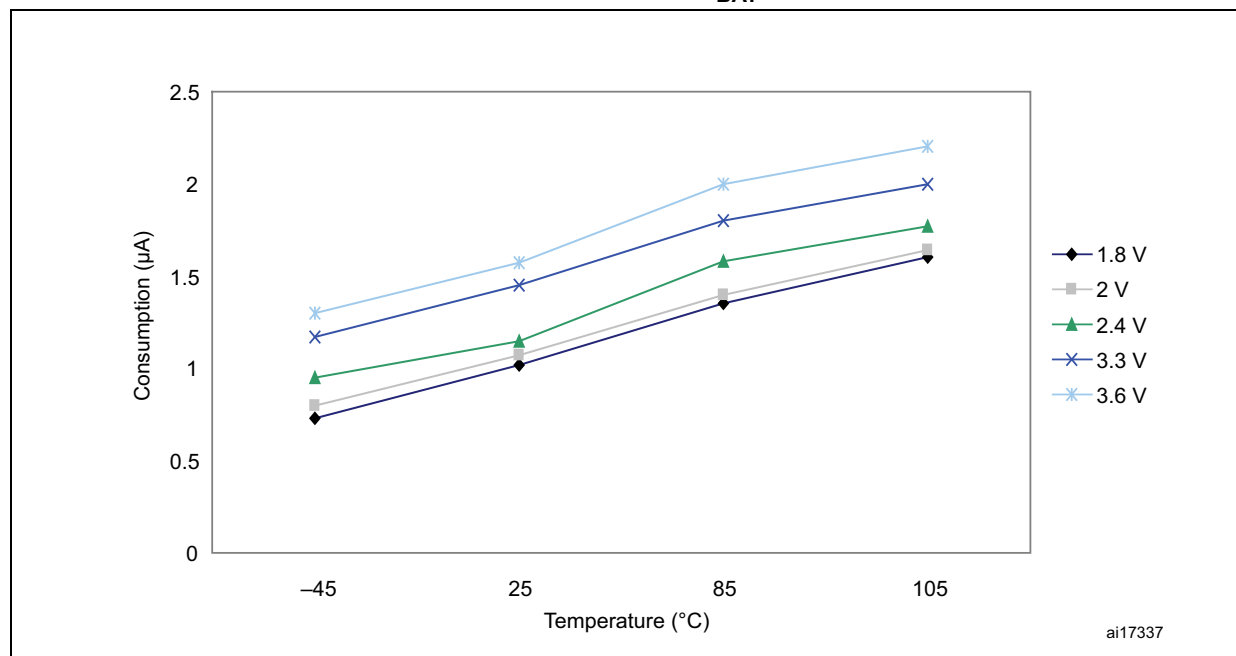


Table 20. Peripheral current consumption (continued)

Peripheral		Current consumption	Unit
APB1 (up to 36 MHz)	APB1-Bridge	7,78	μA/MHz
	TIM2	33,06	
	TIM3	31,94	
	TIM4	31,67	
	TIM5	31,94	
	TIM6	8,06	
	TIM7	8,06	
	SPI2/I2S2 ⁽²⁾	8,33	
	SPI3/I2S3 ⁽²⁾	8,33	
	USART2	12,22	
	USART3	12,22	
	UART4	12,22	
	UART5	12,22	
	I2C1	10,28	
	I2C2	10,00	
	USB	18,06	
	CAN1	18,33	
	DAC ⁽³⁾	8,06	
	WWDG	3,89	
	PWR	1,11	
	BKP	1,11	
	IWDG	5,28	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 23](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

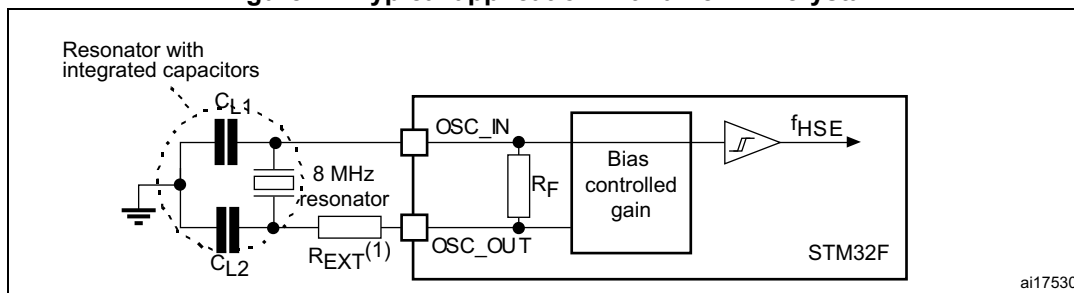
Table 23. HSE 4-16 MHz oscillator characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30 \Omega$	-	30	-	pF
i_2	HSE driving current	$V_{DD} = 3.3 \text{ V}$, $V_{IN} = V_{SS}$ with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$ ⁽⁴⁾	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

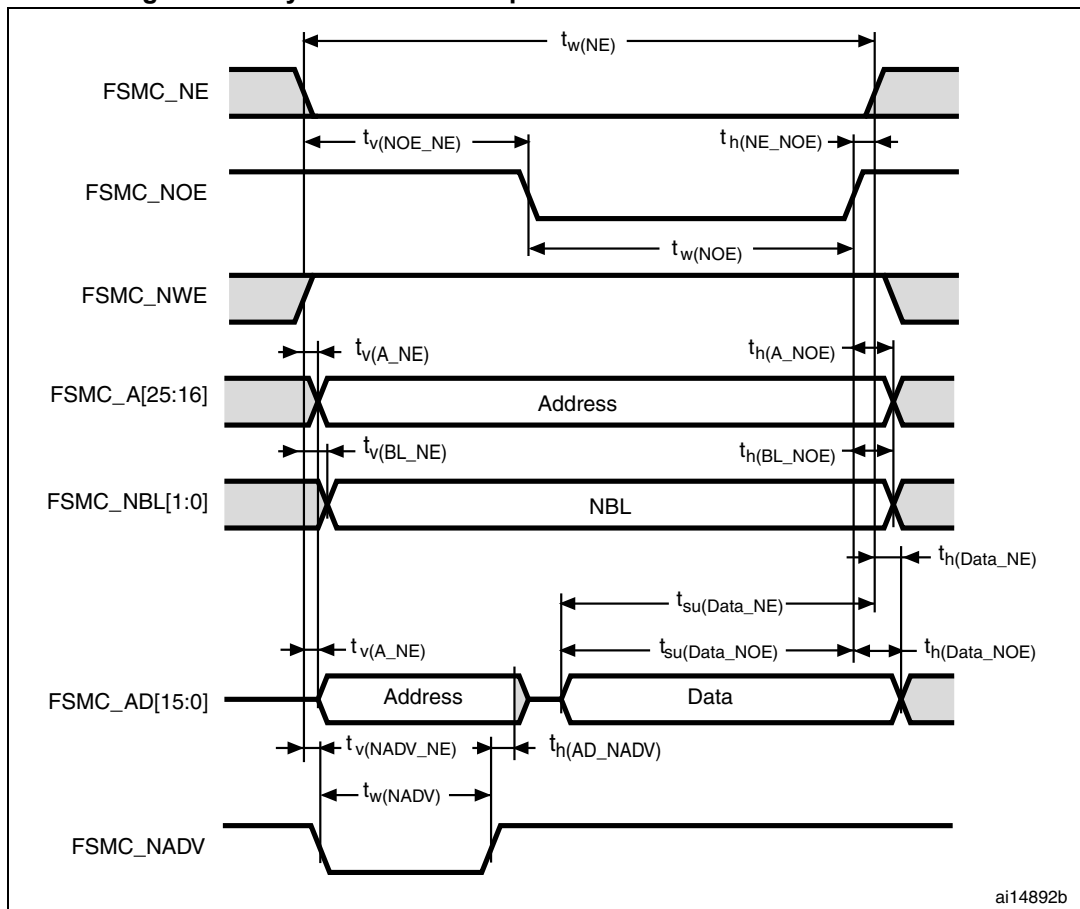
For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 22](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

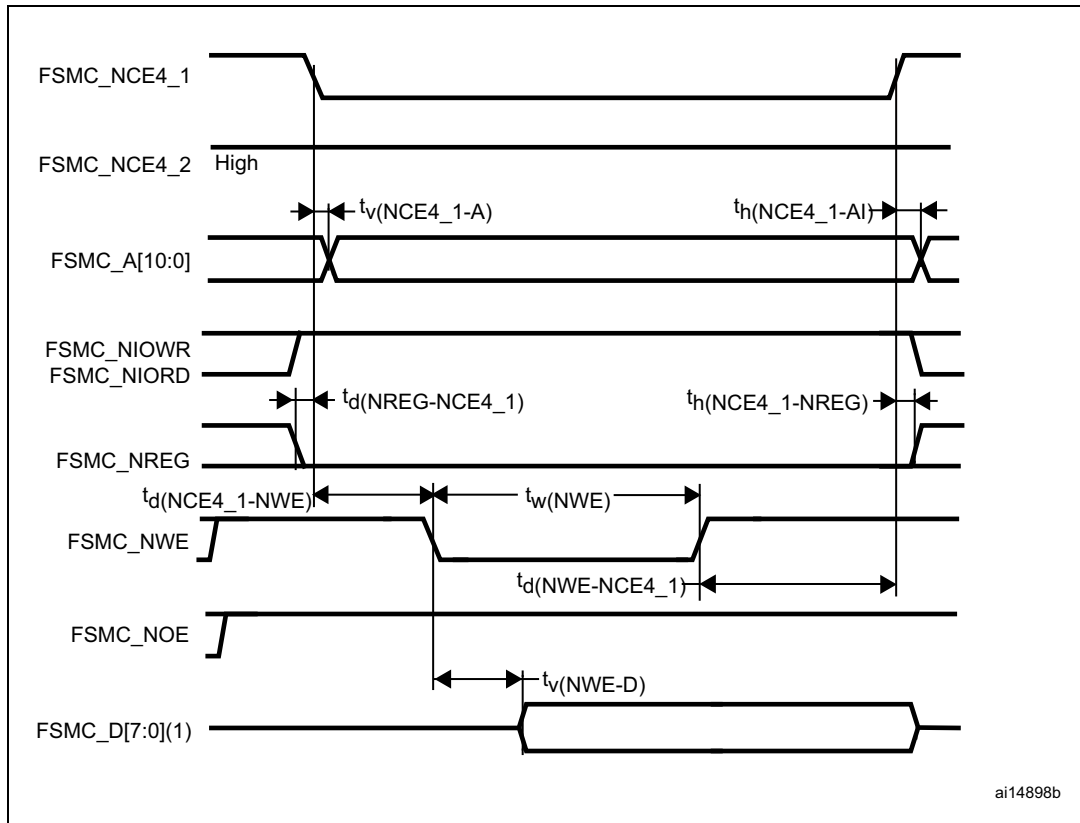
Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms



ai14892b

Table 33. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FSMC_NE low time	$7t_{HCLK} - 2$	$7t_{HCLK} + 2$	ns
$t_v(NOE_NE)$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1.5$	ns
$t_w(NOE)$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 2$	ns
$t_h(NE_NOE)$	FSMC_NOE high to FSMC_NE high hold time	-1	-	ns
$t_v(A_NE)$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_v(NADV_NE)$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_w(NADV)$	FSMC_NADV low time	$t_{HCLK} - 1.5$	$t_{HCLK} + 1.5$	ns
$t_h(AD_NADV)$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_h(A_NOE)$	Address hold time after FSMC_NOE high	$t_{HCLK} - 2$	-	ns
$t_h(BL_NOE)$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_v(BL_NE)$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su}(Data_NE)$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 24$	-	ns
$t_{su}(Data_NOE)$	Data to FSMC_NOE high setup time	$2t_{HCLK} + 25$	-	ns

Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access

1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

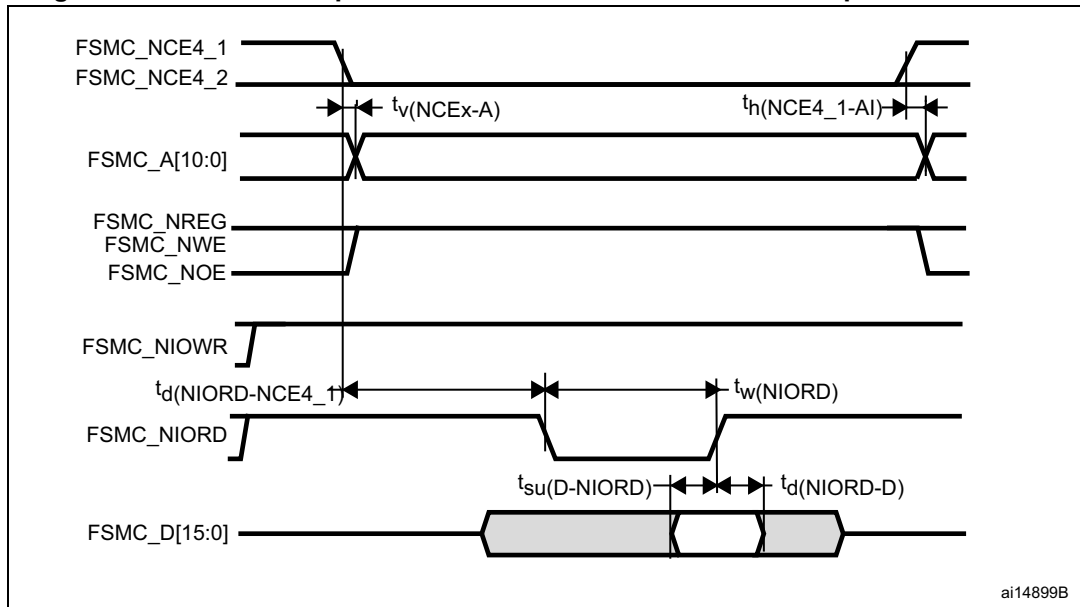
Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access

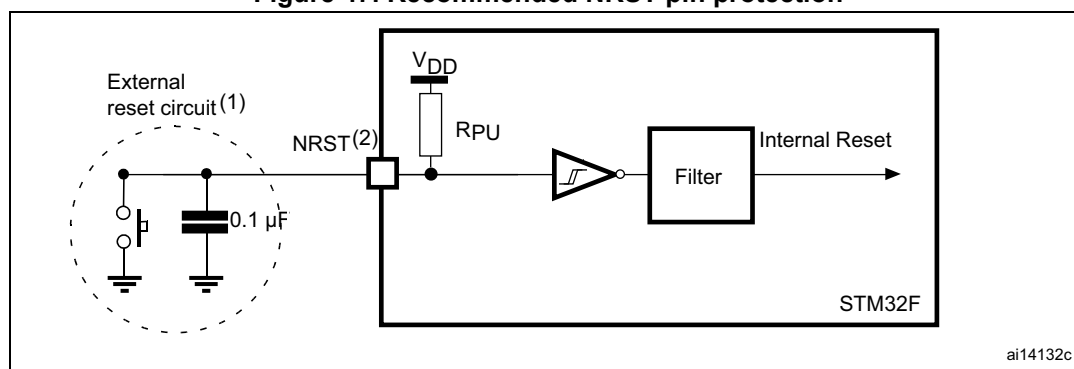
Table 39. Switching characteristics for PC Card/CF read and write cycles⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8t_{HCLK} + 3$	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5t_{HCLK} + 1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5t_{HCLK} + 3ns$	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5t_{HCLK} - 5$	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	$5t_{HCLK} + 2.5$	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5t_{HCLK} - 5$	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8t_{HCLK} + 2$	-	ns

1. $C_L = 15$ pF.

2. Guaranteed by characterization results.

Figure 47. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 49](#). Otherwise the reset will not be taken into account by the device.

5.3.16 TIM timer characteristics

The parameters given in [Table 50](#) are guaranteed by design.

Refer to [Section 5.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 50. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 72 \text{ MHz}$	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

Table 54. I²S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
f_{CK} $1/t_{c(CK)}$	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)		1.522	1.525	MHz
		Slave mode		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I ² S clock rise and fall time	Capacitive load C _L = 50 pF		-	8	ns
$t_{v(WS)}^{(1)}$	WS valid time	Master mode		3	-	
$t_{h(WS)}^{(1)}$	WS hold time	Master mode	I2S2	2	-	
			I2S3	0	-	
$t_{su(WS)}^{(1)}$	WS setup time	Slave mode		4	-	
$t_{h(WS)}^{(1)}$	WS hold time	Slave mode		0	-	
$t_{w(CKH)}^{(1)}$	CK high and low time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz		312.5	-	
$t_{w(CKL)}^{(1)}$				345	-	
$t_{su(SD_MR)}^{(1)}$	Data input setup time	Master receiver	I2S2	2	-	
			I2S3	6.5	-	
$t_{su(SD_SR)}^{(1)}$	Data input setup time	Slave receiver		1.5	-	
$t_{h(SD_MR)}^{(1)(2)}$	Data input hold time	Master receiver		0	-	
$t_{h(SD_SR)}^{(1)(2)}$		Slave receiver		0.5	-	
$t_{v(SD_ST)}^{(1)(2)}$	Data output valid time	Slave transmitter (after enable edge)		-	18	
$t_{h(SD_ST)}^{(1)}$	Data output hold time	Slave transmitter (after enable edge)		11	-	
$t_{v(SD_MT)}^{(1)(2)}$	Data output valid time	Master transmitter (after enable edge)		-	3	
$t_{h(SD_MT)}^{(1)}$	Data output hold time	Master transmitter (after enable edge)		0	-	

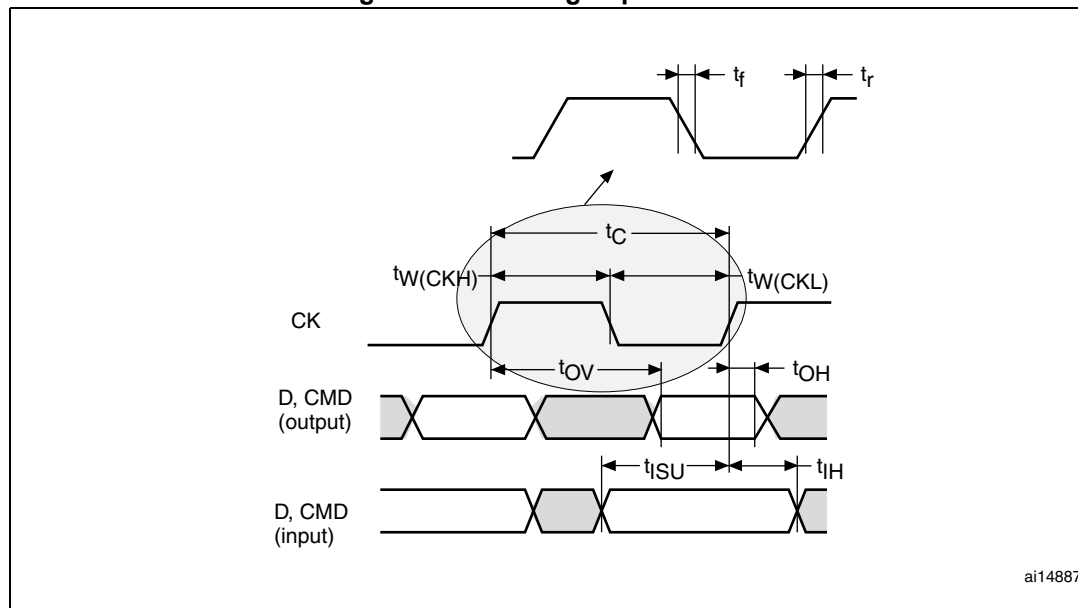
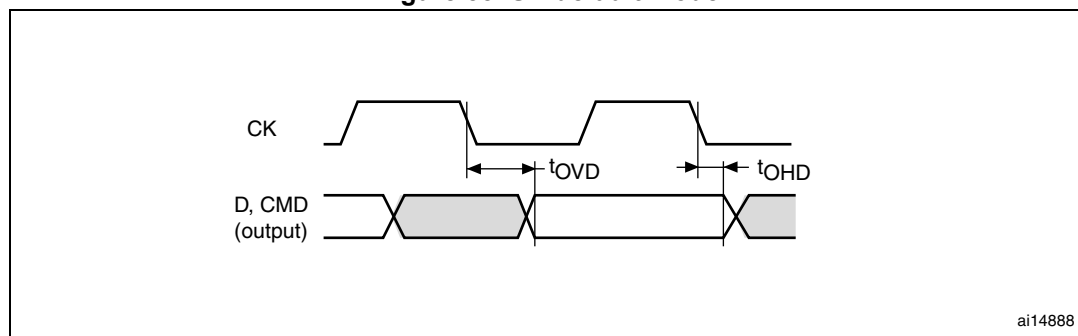
1. Guaranteed by design and/or characterization results.

2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 10](#).

Refer to [Section 5.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 54. SDIO high-speed mode**Figure 55. SD default mode****Table 55. SD / MMC characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
$t_W(CKL)$	Clock low time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	32	-	ns
$t_W(CKH)$	Clock high time, $f_{PP} = 16$ MHz	$C_L \leq 30$ pF	30	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	4	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	

5.3.20 DAC electrical specifications

Table 63. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
$R_{LOAD}^{(1)}$	Resistive load with buffer ON	5	-	-	k Ω	-
$R_O^{(2)}$	Impedance output with buffer OFF	-	-	15	k Ω	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
$C_{LOAD}^{(1)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
$DAC_OUT_{min}^{(1)}$	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x155) and (0xEAB) at $V_{REF+} = 2.4$ V
$DAC_OUT_{max}^{(1)}$	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	
$DAC_OUT_{min}^{(1)}$	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
$DAC_OUT_{max}^{(1)}$	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{REF+} - 1LSB$	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	μ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode ⁽³⁾	-	-	380	μ A	With no load, middle code (0x800) on the inputs
		-	-	480	μ A	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
$DNL^{(4)}$	Differential non linearity Difference between two consecutive code-1LSB)	-	-	± 0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	± 2	LSB	Given for the DAC in 12-bit configuration
$INL^{(3)}$	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	± 1	LSB	Given for the DAC in 10-bit configuration
		-	-	± 4	LSB	Given for the DAC in 12-bit configuration

6.7 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 10: General operating conditions on page 44](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LFBGA144 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	30	
	Thermal resistance junction-ambient LFBGA100 - 10 × 10 mm / 0.8 mm pitch	40	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient WLCSP64	50	

6.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

6.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 75: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xC, STM32F103xD and STM32F103xE at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus: $P_{Dmax} = 447\text{ mW}$

Using the values obtained in [Table 74](#) T_{Jmax} is calculated as follows:

– For LQFP100, $46\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (46\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 82\text{ }^{\circ}\text{C} + 20.6\text{ }^{\circ}\text{C} = 102.6\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 75: Ordering information scheme](#)).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 115\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 74](#) T_{Jmax} is calculated as follows:

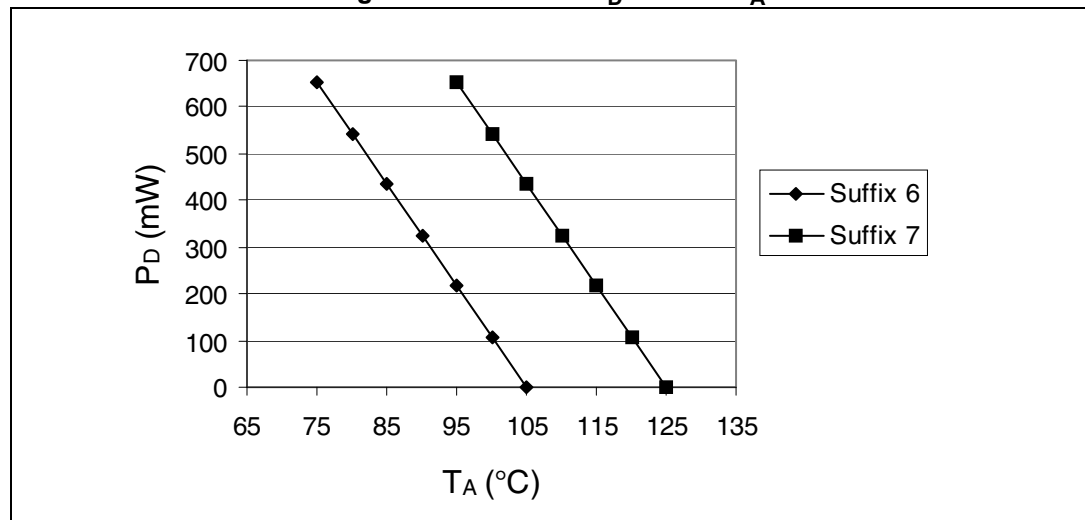
– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ($-40 < T_J < 125\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 75: Ordering information scheme](#)).

Figure 79. LQFP100 P_D max vs. T_A



7 Part numbering

Table 75. Ordering information scheme

Example:	STM32	F	103	R	C		T	6	xxx
Device family STM32 = ARM-based 32-bit microcontroller									
Product type F = general-purpose									
Device subfamily 103 = performance line									
Pin count R = 64 pins V = 100 pins Z = 144 pins									
Flash memory size C = 256 Kbytes of Flash memory D = 384 Kbytes of Flash memory E = 512 Kbytes of Flash memory									
Package H = BGA T = LQFP Y = WLCSP64									
Temperature range 6 = Industrial temperature range, -40 to 85 °C. 7 = Industrial temperature range, -40 to 105 °C.									
Options xxx = programmed parts TR = tape and real									

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 76. Document revision history

Date	Revision	Changes
07-Apr-2008	1	Initial release.
22-May-2008	2	Document status promoted from Target Specification to Preliminary Data. <i>Section 1: Introduction</i> and <i>Section 2.2: Full compatibility throughout the family</i> modified. Small text changes. <i>Note 2</i> added in <i>Table 2: STM32F103xC, STM32F103xD and STM32F103xE features and peripheral counts on page 11</i>. LQPF100/BGA100 column added to <i>Table 6: FSMC pin definition on page 38</i>. Values and Figures added to <i>Maximum current consumption on page 62</i> (see <i>Table 18, Table 19, Table 20</i> and <i>Table 21</i> and see <i>Figure 14, Figure 15, Figure 17, Figure 18</i> and <i>Figure 19</i>). Values added to <i>Typical current consumption on page 73</i> (see <i>Table 22, Table 23</i> and <i>Table 24</i>). <i>Table 19: Typical current consumption in Standby mode</i> removed. <i>Note 4</i> and <i>Note 1</i> added to <i>Table 65: USB DC electrical characteristics</i> and <i>Table 66: USB: full-speed electrical characteristics on page 129</i>, respectively. V_{USB} added to <i>Table 65: USB DC electrical characteristics on page 129</i>. <i>Figure 68: Recommended footprint⁽¹⁾ on page 143</i> corrected. <i>Equation 1</i> corrected. <i>Figure 73: LQFP100 P_D max vs. T_A on page 149</i> modified. Tolerance values corrected in <i>Table 74: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package data on page 139</i>.