STMicroelectronics - STM32F103VET7TR Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vet7tr

2 Description

The STM32F103xC, STM32F103xD and STM32F103xE performance line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer three 12-bit ADCs, four general-purpose 16-bit timers plus two PWM timers, as well as standard and advanced communication interfaces: up to two I^{2}Cs, three SPIs, two I^{2}Ss, one SDIO, five USARTs, an USB and a CAN.

The STM32F103xC/D/E high-density performance line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F103xC/D/E high-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems video intercom, and HVAC.

2.3.14 Low-power modes

The STM32F103xC, STM32F103xD and STM32F103xE performance line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I^2S, SDIO and ADC.

2.3.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a

2.3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.30 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 6. FSMC pin definition

Pins	FSMC					LQFP100 BGA100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP144	-	666	mW
		LQFP100	-	434	
		LQFP64	-	444	
		LFBGA100	-	500	
		LFBGA144	-	500	
		WLCSP64	-	400	
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(4)	–40	125	
TJ	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

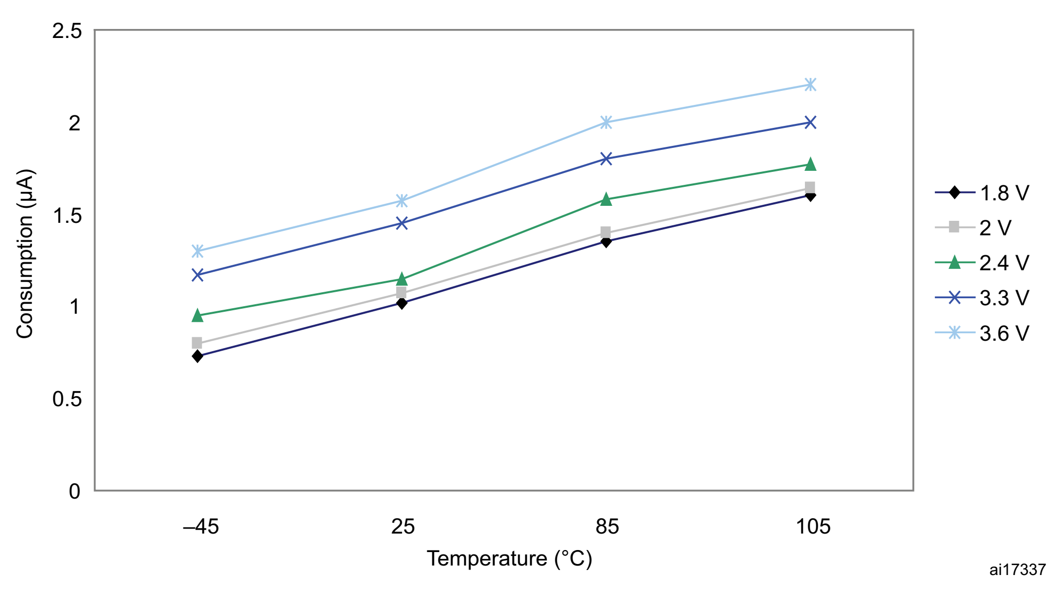
1. When the ADC is used, refer to *Table 59: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.7: Thermal characteristics on page 133*).
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.7: Thermal characteristics on page 133*).

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ[1]			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	1130	µA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	1110	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5[2]	6.5[2]	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2[2]	2.3[2]	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results.

Figure 16. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHZ and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)

When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ[1]		Unit
				All peripherals enabled[2]	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock[3]	72 MHz	51	30.5	mA
			48 MHz	34.6	20.7	
			36 MHz	26.6	16.2	
			24 MHz	18.5	11.4	
			16 MHz	12.8	8.2	
			8 MHz	7.2	5	
			4 MHz	4.2	3.1	
			2 MHz	2.7	2.1	
			1 MHz	2	1.7	
			500 kHz	1.6	1.4	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45	27	mA
			48 MHz	34	20.1	
			36 MHz	26	15.6	
			24 MHz	17.9	10.8	
			16 MHz	12.2	7.6	
			8 MHz	6.6	4.4	
			4 MHz	3.6	2.5	
			2 MHz	2.1	1.5	
			1 MHz	1.4	1.1	
			500 kHz	1	0.8	
			125 kHz	0.7	0.6	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ[1]		Unit
				All peripherals enabled[2]	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock[3]	72 MHz	29.5	6.4	mA
			48 MHz	20	4.6	
			36 MHz	15.1	3.6	
			24 MHz	10.4	2.6	
			16 MHz	7.2	2	
			8 MHz	3.9	1.3	
			4 MHz	2.6	1.2	
			2 MHz	1.85	1.15	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
			125 kHz	1.2	1.05	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	25.6	5.1	
			48 MHz	19.4	4	
			36 MHz	14.5	3	
			24 MHz	9.8	2	
			16 MHz	6.6	1.4	
			8 MHz	3.3	0.7	
			4 MHz	2	0.6	
			2 MHz	1.25	0.55	
			1 MHz	0.9	0.5	
			500 kHz	0.7	0.45	
			125 kHz	0.6	0.45	

1. Typical values are measures at $T_A = 25\ °C$, $V_{DD} = 3.3\ V$.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 20. Peripheral current consumption (continued)

Peripheral		Current consumption	Unit
APB2 (up to 72 MHz)	APB2-Bridge	4,17	µA/MHz
	GPIOA	8,47	
	GPIOB	8,47	
	GPIOC	6,53	
	GPIOD	8,47	
	GPIOE	6,53	
	GPIOF	6,53	
	GPIOG	6,11	
	SPI1	4,72	
	USART1	12,50	
	TIM1	22,92	
	TIM8	22,92	
	ADC1(4)	17,32	
	ADC2(4)	15,18	
	ADC3(4)	14,82	

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1 or DMA2).
2. When the I2S is enabled, a current consumption equal to 0.02 mA must be added.
3. When DAC_OU1 or DAC_OUT2 is enabled, a current consumption equal to 0.36 mA must be added.
4. Specific conditions for measuring ADC current consumption: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADCx_CR2 register is set to 1, a current consumption of analog part equal to 0.54 mA must be added for each ADC.

Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms

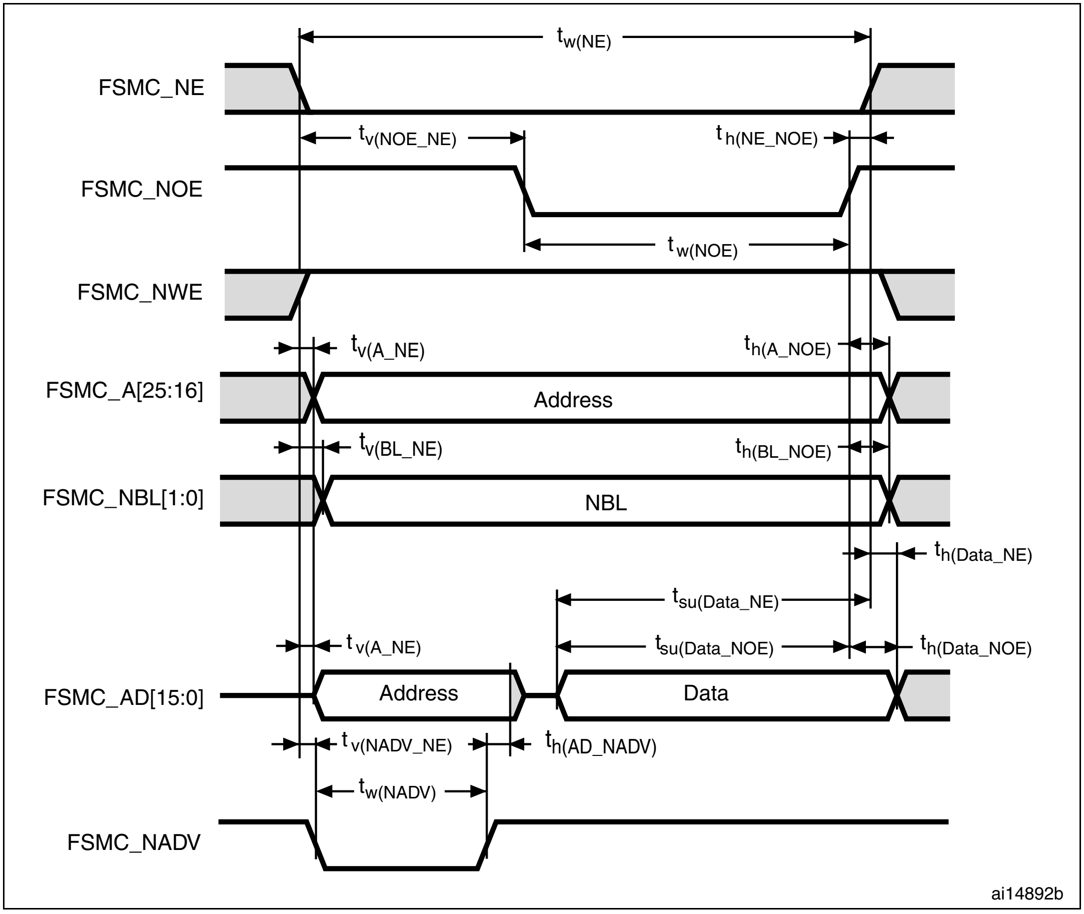


Table 33. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK} - 2$	$7t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 1.5$	$t_{HCLK} + 1.5$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	$t_{HCLK} - 2$	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 24$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2t_{HCLK} + 25$	-	ns

Table 36. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 33. PC Card/CompactFlash controller waveforms for common memory write access

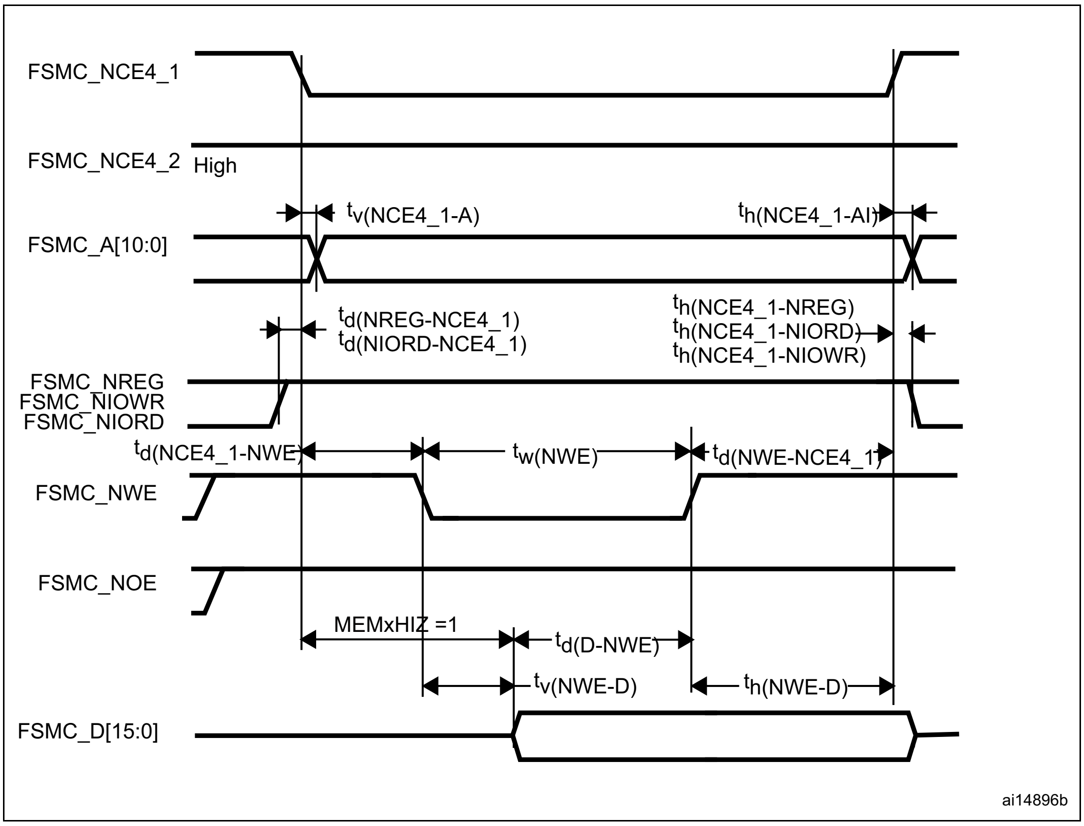
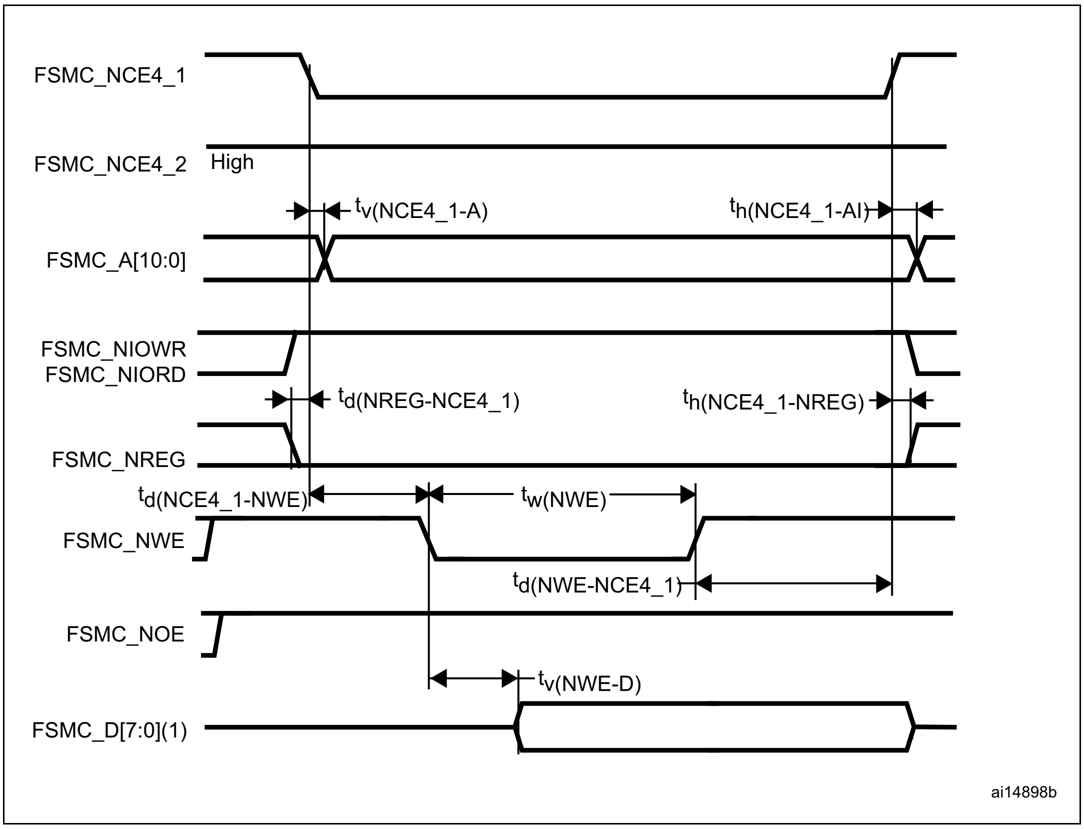
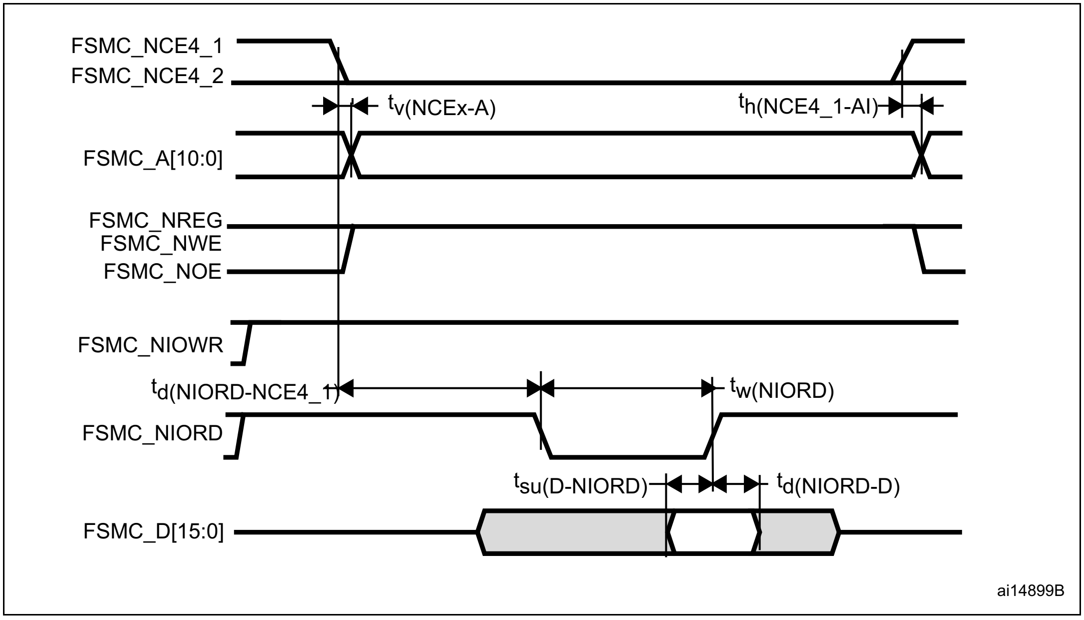


Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access



To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 42. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.3$ V, $T_A = 25$ °C, LQFP144 package compliant with IEC 61967-2	0.1 to 30 MHz	8	12	dBµV
			30 to 130 MHz	31	21	
			130 MHz to 1GHz	28	33	
			SAE EMI Level	4	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 43. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25$ °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25$ °C, conforming to JESD22-C101	III	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

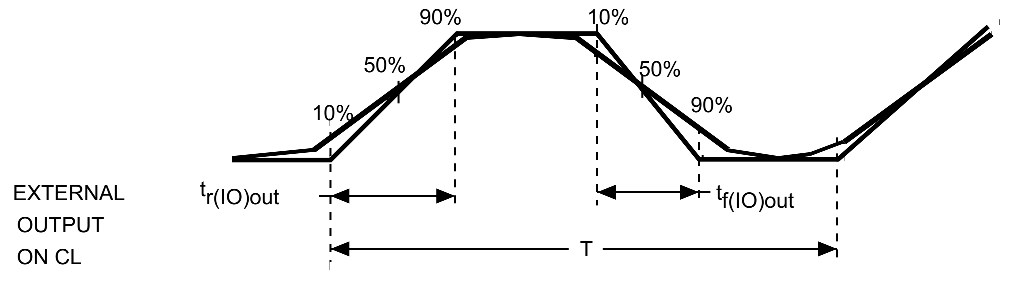
These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 47. Output voltage characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results.

Figure 46. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%)
when loaded by CL specified in the table “ *I/O AC characteristics*”.

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 46*).

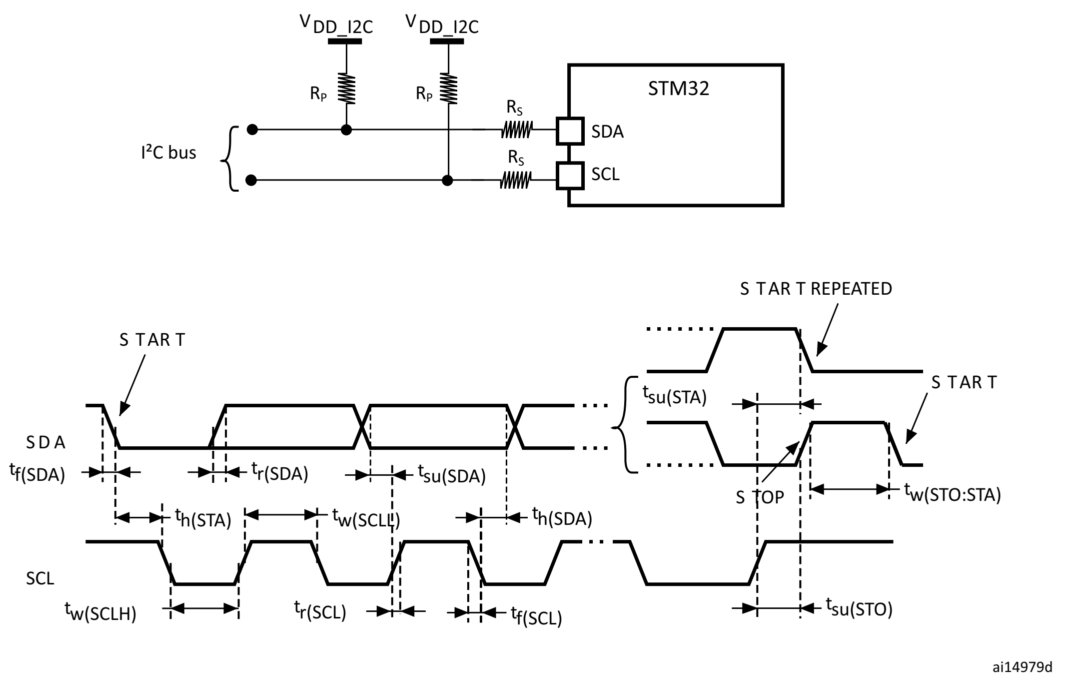
Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 48. I^2C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs: Series protection resistors.
3. Rp: Pull-up resistors.
4. VDD_I2C : I2C bus supply

Table 52. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

5.3.18 CAN (controller area network) interface

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 59* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

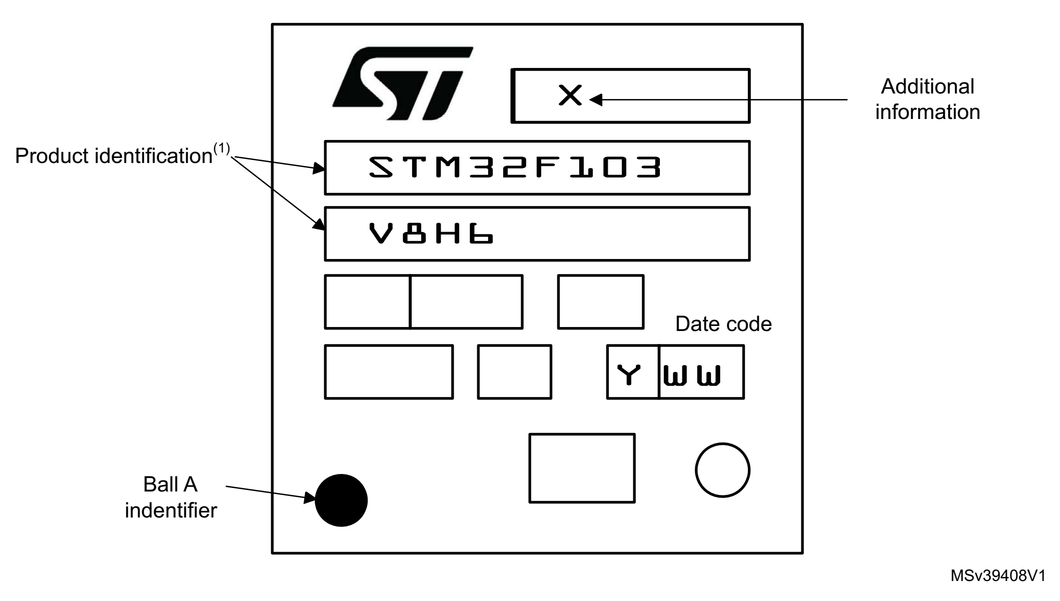
Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 60* for details	-	-	50	κΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	κΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

Device marking for LFBGA100 package

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 67. LFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 69. WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
e1	-	3.500	-	-	0.1378	-
F	-	0.447	-	-	0.0176	-
G	-	0.483	-	-	0.0190	-
D	4.446	4.466	4.486	0.1750	0.1758	0.1766
E	4.375	4.395	4.415	0.1722	0.1730	0.1738
H	-	0.250	-	-	0.0098	-
L	-	0.200	-	-	0.0079	-
eee	-	0.05	-	-	0.0020	-
aaa	-	0.10	-	-	0.0039	-
Number of balls	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum ball diameter parallel to primary datum Z.

Figure 69. WLCSP64 - 64-ball, 4.4757 x 4.4049 mm, 0.5 mm pitch wafer level chip scale package recommended footprint

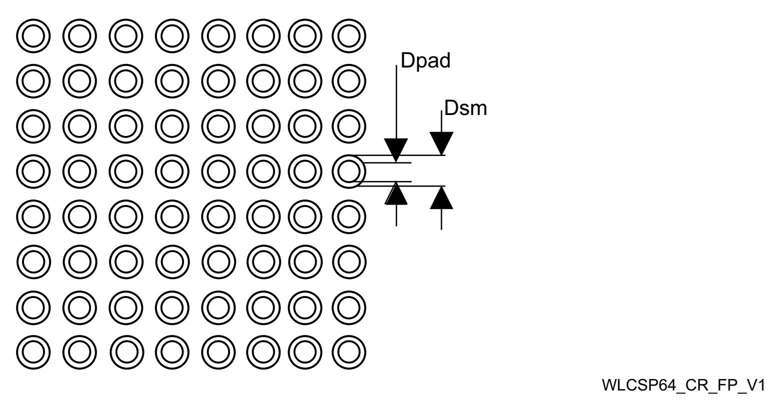


Table 70. WLCSP64 recommended PCB design rules (0.5 mm pitch)

Dimension	Recommended values
Pitch	0.5
Dpad	250 µm
Dsm	300 µm
Stencil Opening	320 µm
Stencil Thickness	Between 100 µm to 125 µm
Pad trace width	100 µm
Ball Diameter	320 µm