

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zct6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.



2.3.14 Low-power modes

The STM32F103xC, STM32F103xD and STM32F103xE performance line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

• Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

• Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

• Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I²S, SDIO and ADC.

2.3.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a



Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from



the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.21 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I²S interfaces is/are configured in master



DocID14611 Rev 12

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.3.27 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.



2.3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.30 Embedded Trace Macrocell™

The ARM[®] Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.





Figure 6. STM32F103xC/D/E performance line LQFP100 pinout

1. The above figure shows the package top view.





Figure 7. STM32F103xC/D/E performance line LQFP64 pinout

1. The above figure shows the package top view.





Figure 19. Typical current consumption in Standby mode versus temperature at different $\rm V_{DD}$ values



5.3.10 FSMC characteristics

Asynchronous waveforms and timings

Figure 24 through *Figure 27* represent asynchronous waveforms and *Table 31* through *Table 34* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 24. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.



Symbol	Parameter	Min	Мах	Unit			
t _{w(CLK)}	FSMC_CLK period	27.7	-	ns			
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x = 02)	-	1.5	ns			
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x = 02)	2	-	ns			
t _{d(CLKL-NADVL)}	FSMC_CLK low to FSMC_NADV low	-	4	ns			
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	5	-	ns			
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x = 1625)	-	0	ns			
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x = 1625)	2	-	ns			
t _{d(CLKL-NOEL)}	FSMC_CLK low to FSMC_NOE low	-	1	ns			
t _{d(CLKL-NOEH)}	FSMC_CLK low to FSMC_NOE high	1.5	-	ns			
t _{d(CLKL-ADV)}	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns			
t _{d(CLKL-ADIV)}	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns			
t _{su(ADV-CLKH)}	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns			
t _{h(CLKH-ADV)}	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns			
t _{su(NWAITV-CLKH)}	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns			
t _{h(CLKH-NWAITV)}	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns			

Table 35. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

1. C_L = 15 pF.

2. Guaranteed by characterization results.



5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Symbol	Parameter	Conditions	Level/ Class
V _{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T _A = +25 °C, f _{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V _{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$\label{eq:VDD} \begin{array}{l} V_{DD} = 3.3 \text{ V}, \text{LQFP144}, \text{T}_{\text{A}} = +25 \\ ^{\circ}\text{C}, \\ \text{f}_{\text{HCLK}} = 72 \text{ MHz} \\ \text{conforms to IEC 61000-4-4} \end{array}$	4A

Table 41. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.





Figure 47. Recommended NRST pin protection

- 1. The reset network protects the device against parasitic resets.
- The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in Table 49. Otherwise the reset will not be taken into account by the device.

5.3.16 TIM timer characteristics

The parameters given in Table 50 are guaranteed by design.

Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions	Min	Мах	Unit
+	Timer resolution time	-	1	-	t _{TIMxCLK}
^r res(TIM)		f _{TIMxCLK} = 72 MHz	13.9	-	ns
f	Timer external clock	-	0	f _{TIMxCLK} /2	MHz
^I EXT	frequency on CH1 to CH4	f _{TIMxCLK} = 72 MHz	0	36	MHz
Res _{TIM}	Timer resolution	-	-	16	bit
	16-bit counter clock period	-	1	65536	t _{TIMxCLK}
t _{COUNTER}	when internal clock is selected	f _{TIMxCLK} = 72 MHz	0.0139	910	μs
t _{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	t _{TIMxCLK}
		f _{TIMxCLK} = 72 MHz	-	59.6	S

Table 50. TIMx⁽¹⁾ characteristics

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.



Symbol	Parameter	Test conditions	Тур	Max ⁽⁴⁾	Unit
ET	Total unadjusted error	6 - 50 MUL	±2	±5	
EO	Offset error	$f_{ADC} = 14 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega,$	±1.5	±2.5	
EG	Gain error	$V_{DDA} = 2.4 V \text{ to } 3.6 V$	±1.5	±3	LSB
ED	Differential linearity error	Measurements made after	±1	±2	
EL	Integral linearity error		±1.5	±3	

Table 62. ADC accuracy^{(1) (2)(3)}

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted V_{DD} , frequency, V_{REF} and temperature ranges.

 ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 5.3.14 does not affect the ADC accuracy.

4. Guaranteed by characterization results.





- 1. Example of an actual transfer curve.
- 2. Ideal transfer curve.
- 3. End point correlation line.
- 4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves. EO = Offset Error: deviation between the first actual transition and the first ideal one. EG = Gain Error: deviation between the last ideal transition and the last actual one. ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one. EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.



DocID14611 Rev 12

5.3.20 DAC electrical specifications

Symbol	Parameter	Min	Тур	Мах	Unit	Comments
V _{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V _{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF^+} must always be below V_{DDA}
V _{SSA}	Ground	0	-	0	V	-
R _{LOAD} ⁽¹⁾	Resistive load with buffer ON	5	-	-	kΩ	-
R ₀ ⁽²⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} – 0.2	V	and (0x155) and (0xEAB) at $V_{REF+} = 3.0 \text{ V}$ 2.4 V
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	-	V _{REF+} – 1LSB	V	excursion of the DAC.
I _{DDVREF+}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
	DAC DC current	-	-	380	μA	With no load, middle code (0x800) on the inputs
I _{DDA}	consumption in quiescent mode ⁽³⁾	_	-	480	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL ⁽⁴⁾	Differential non linearity Difference between two	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	-	-	±2	LSB	Given for the DAC in 12-bit configuration
	Integral non linearity (difference between	-	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽³⁾ measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)		-	-	±4	LSB	Given for the DAC in 12-bit configuration

Tahlo	63	DAC	characteristics
Table	65.	DAC	characteristics



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

6.1 LFBGA144 package information



Figure 62. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline

1. Drawing is not to scale.

Table 65. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm,
0.8 mm pitch, package mechanical data

Symbol		millimeters		inches ⁽¹⁾		
Symbol	Min	Тур	Max	Тур	Min	Max
A ⁽²⁾	-	-	1.700	-	-	0.0669
A1	0.250	0.300	0.350	0.098	0.0118	0.0138
A2	0.810	0.910	1.010	0.0319	0.0358	0.0398
A3	0.225	0.26	0.295	0.0089	0.0102	0.0116
A4	0.585	0.650	0.715	0.0230	0.0256	0.0281



Device marking for LFBGA100 package

The following figure gives an example of topside marking orientation versus ball A1 identifier location.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



Using the values obtained in *Table 74* T_{Jmax} is calculated as follows:

- For LQFP100, 46 °C/W
- T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 75: Ordering information scheme*).







Date	Revision	Changes					
12-Dec-2008	4	Timers specified on page 1 (motor control capability mentioned). Section 2.2: Full compatibility throughout the family updated. Table 6: High-density timer feature comparison added. General-purpose timers (TIMx) and Advanced-control timers (TIM1 and TIM8) on page 27 updated. Figure 1: STM32F103xF, STM32F103xD and STM32F103xGSTM32F103xF and STM32F103xG performance line block diagram modified. Note 10 added, main function after reset and Note 5 on page 44 updated in Table 8: High-density STM32F103xx pin definitions. Note 2 modified below Table 11: Voltage characteristics on page 58, $ DV_{DDx} $ min and $ DV_{DDx} $ min removed. Note 2 and P _D values for LQFP144 and LFBGA144 packages added to Table 14: General operating conditions on page 59. Measurement conditions specified in Section 5.3.5: Supply current characteristics on page 62. Max values at T _A = 85 °C and T _A = 105 °C updated in Table 21: Typical and maximum current consumptions in Stop and Standby modes on page 68. Section 5.3.10: FSMC characteristics on page 111. I_{VREF} added to Table 67: ADC characteristics on page 130. Table 81: Package thermal characteristics on page 146 updated. Small text changes.					

Table 76.Document revision history



	Iable /6.Document revision history					
Date	Revision	Changes				
Date	Revision	Changes I/O information clarified on page 1. Figure 4: STM32F103xC and STM32F103xE performance line BGA100 ballout corrected. I/O information clarified on page 1. In Table 5: High-density STM32F103xx pin definitions: - I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated - PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column PG14 pin description modified in Table 6: FSMC pin definition. Figure 9: Memory map on page 54 modified. Note medified in Table 18: Maximum current consumption in Pun				
		Note modified in Table 18: Maximum current consumption in Run mode, code with data processing running from Flash and Table 20: Maximum current consumption in Sleep mode, code running from Flash or RAM. Figure 17, Figure 18 and Figure 19 show typical curves (titles changed). Table 25: High-speed external user clock characteristics and Table 26: Low-speed external user clock characteristics modified. ACC _{HSI} max values modified in Table 29: HSI oscillator characteristics. FSMC configuration modified for Asynchronous waveforms and timings. Notes modified below Figure 24: Asynchronous non-				
30-Mar-2009	5	multiplexed SRAM/PSRAM/NOR read waveforms and Figure 25: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms. t _{w(NADV)} values modified in Table 35: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings and Table 39: Asynchronous multiplexed PSRAM/NOR write timings. t _{h(Data_NWE)} modified in Table 36: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings In Table 41: Synchronous multiplexed PSRAM write timings and				
		Table 43: Synchronous non-multiplexed PSRAM write timings:- $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ - $t_{d(CLKL-Data)}$ min value removed and max value added- $t_{d(CLKL-Data)}$ min value removed and max value added- $t_{h(CLKL-DV)} / t_{h(CLKL-ADV)}$ removedFigure 28: Synchronous multiplexed NOR/PSRAM read timings,Figure 29: Synchronous multiplexed PSRAM write timings andFigure 31: Synchronous non-multiplexed PSRAM write timingsmodified.Figure 52: I2S slave timing diagram (Philips protocol)(1) and Figure 53:I2S master timing diagram (Philips protocol)(1) modified.WLCSP64 package added (see Figure 8: STM32F103xC andSTM32F103xE performance line WLCSP64 ballout, ball side, Table 8:High-density STM32F103xx pin definitions, Figure 65: WLCSP, 64-ball4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale packageoutline and Table 76: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mmpitch, wafer-level chip-scale package mechanical data).Small text changes.				

Table 76 Document revision histo

