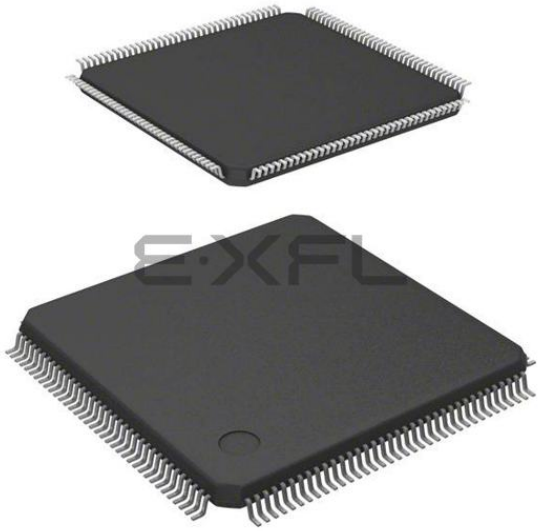

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zct7

2.1 Device overview

The STM32F103xC/D/E high-density performance line family offers devices in six different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F103xC, STM32F103xD and STM32F103xE features and peripheral counts

Peripherals		STM32F103Rx			STM32F103Vx			STM32F103Zx		
Flash memory in Kbytes		256	384	512	256	384	512	256	384	512
SRAM in Kbytes		48	64(1)		48	64		48	64	
FSMC		No			Yes(2)			Yes		
Timers	General-purpose	4								
	Advanced-control	2								
	Basic	2								
Comm	SPI(I^2S)(3)	3(2)								
	I^2C	2								
	USART	5								
	USB	1								
	CAN	1								
	SDIO	1								
GPIOs		51			80			112		
12-bit ADC Number of channels		3 16			3 16			3 21		
12-bit DAC Number of channels		2 2								
CPU frequency		72 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C (see *Table 10*) Junction temperature: –40 to + 125 °C (see *Table 10*)								
Package		LQFP64, WLCSP64			LQFP100, BGA100			LQFP144, BGA144		

1. 64 KB RAM for 256 KB Flash are available on devices delivered in CSP packages only.
2. For the LQFP100 and BGA100 packages, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
3. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I^2S audio mode.

2.2 Full compatibility throughout the family

The STM32F103xC/D/E is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices and the STM32F103xC, STM32F103xD and STM32F103xE are referred to as high-density devices.

Low-density and high-density devices are an extension of the STM32F103x8/B medium-density devices, they are specified in the STM32F103x4/6 and STM32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I^2S and DAC while remaining fully compatible with the other members of the family.

The STM32F103x4, STM32F103x6, STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for the STM32F103x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F103xx family

<table>
<tr><th rowspan="3">Pinout</th><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>6 KB RAM</th><th>10 KB RAM</th><th>20 KB RAM</th><th>20 KB RAM</th><th>48 RAM</th><th>64 KB RAM</th><th>64 KB RAM</th></tr>
<tr><td>144</td><td colspan="2" rowspan="2"></td><td colspan="2" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs, USB, CAN, 1 × PWM timer
2 × ADCs</td><td colspan="3" rowspan="2">5 × USARTs
4 × 16-bit timers, 2 × basic timers
3 × SPIs, 2 × I2Ss, 2 × I2Cs
USB, CAN, 2 × PWM timers
3 × ADCs, 2 × DACs, 1 × SDIO
FSMC (100- and 144-pin packages(2))</td></tr>
<tr><td>100</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I2C, USB, CAN, 1 × PWM timer
2 × ADCs</td><td colspan="2" rowspan="2"></td><td colspan="3" rowspan="2"></td></tr>
<tr><td>48</td></tr>
<tr><td>36</td><td colspan="2"></td><td colspan="3"></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.
2. Ports F and G are not available in devices delivered in 100-pin packages.

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xC, STM32F103xD and STM32F103xE performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

2.3.14 Low-power modes

The STM32F103xC, STM32F103xD and STM32F103xE performance line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I^2S, SDIO and ADC.

2.3.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
L4	J4	H4	26	35	46	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	F4	27	36	47	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4(9) TIM8_CH3N	TIM1_CH3N
J5	G5	H3	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	-	-	51	V_{SS_6}	S	-	V_{SS_6}	-	-
G5	-	-	-	-	52	V_{DD_6}	S	-	V_{DD_6}	-	-
K5	-	-	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	H5	-	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	-	-	61	V_{SS_7}	S	-	V_{SS_7}	-	-
G6	-	-	-	-	62	V_{DD_7}	S	-	V_{DD_7}	-	-
J7	G6	-	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	G3	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX(9)	TIM2_CH3
M10	K7	F3	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX(9)	TIM2_CH4
H7	E7	H2	31	49	71	V_{SS_1}	S	-	V_{SS_1}	-	-
G7	F7	H1	32	50	72	V_{DD_1}	S	-	V_{DD_1}	-	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	-
E5	E5	A7	63	99	143	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	F5	A8	64	100	144	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. In the WCLSP64 package, the PC3 I/O pin is not bonded and it must be configured by software to output mode (Push-pull) and writing 0 to the data register in order to avoid an extra consumption during low-power modes.
8. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
10. For the WCLSP64/LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
11. For devices delivered in LQFP64 packages, the FSMC function is not available.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

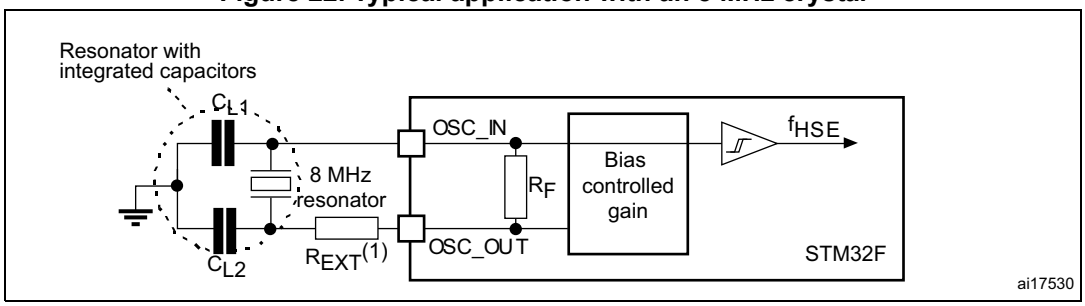
Table 23. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 22*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 22. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

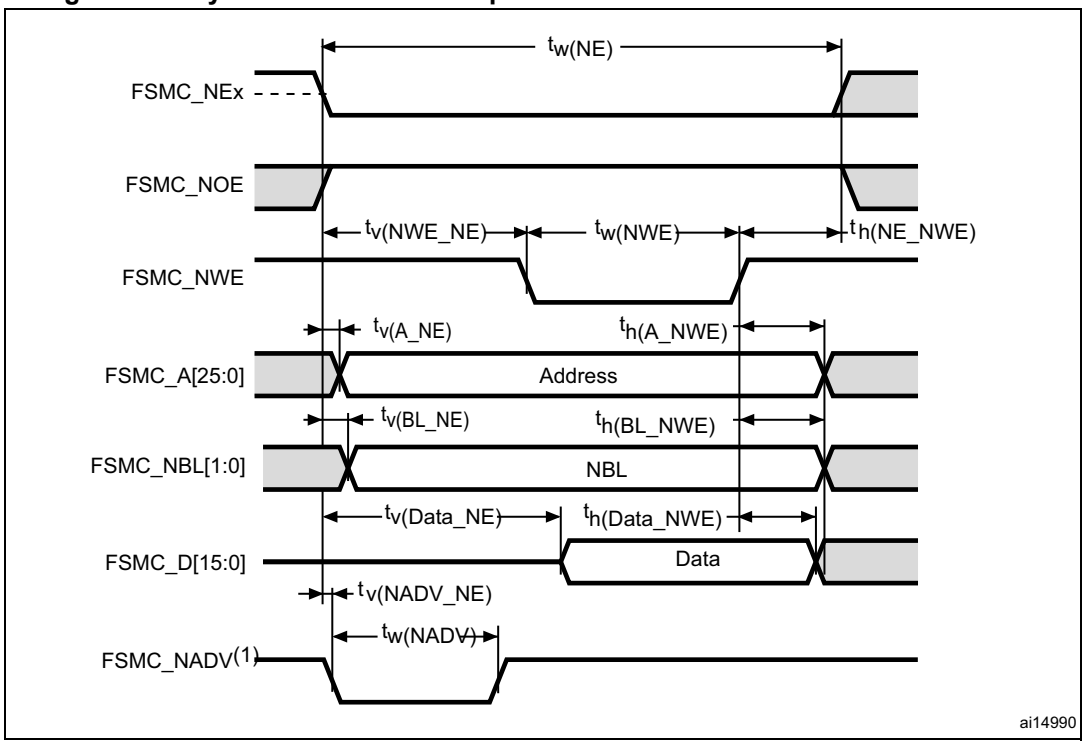
1. Guaranteed by design.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$t_{HCLK} + 1.5$	ns

1. C_L = 15 pF.

Figure 25. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Figure 30. Synchronous non-multiplexed NOR/PSRAM read timings

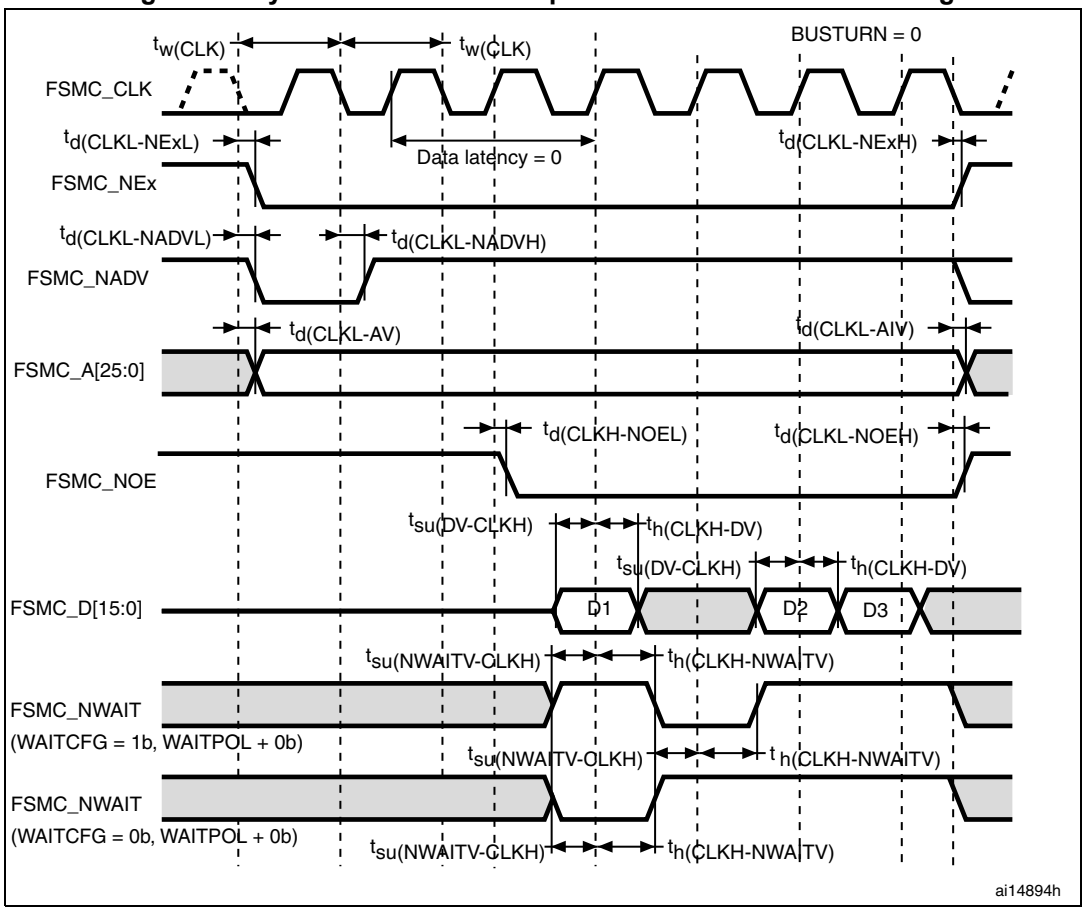


Table 37. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	4	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Table 39. Switching characteristics for PC Card/CF read and write cycles(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8t_{HCLK}$ + 3	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5t_{HCLK}$ +1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5t_{HCLK}$+3ns	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5t_{HCLK}$ – 5	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	$5t_{HCLK}$ + 2.5	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5t_{HCLK}$ – 5	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8t_{HCLK}$ + 2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	–0.3	-	0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage		–0.3	-	0.32*(V_{DD}-2 V)+0.75 V	V
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V	-	V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V	-	5.5	V
		V_{DD} ≤2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)	-	-	mV
I_{lkg}	Input leakage current (4)	V_{SS} ≤V_{IN} ≤V_{DD} Standard I/Os	-	-	±1	µA
		V_{IN}= 5 V, I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 42* and *Figure 43* for standard I/Os, and in *Figure 44* and *Figure 45* for 5 V tolerant I/Os.

Table 57. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xC/D/E USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by characterization results.
5. R_L is the load connected on the USB drivers

Figure 56. USB timings: definition of data signal rise and fall time

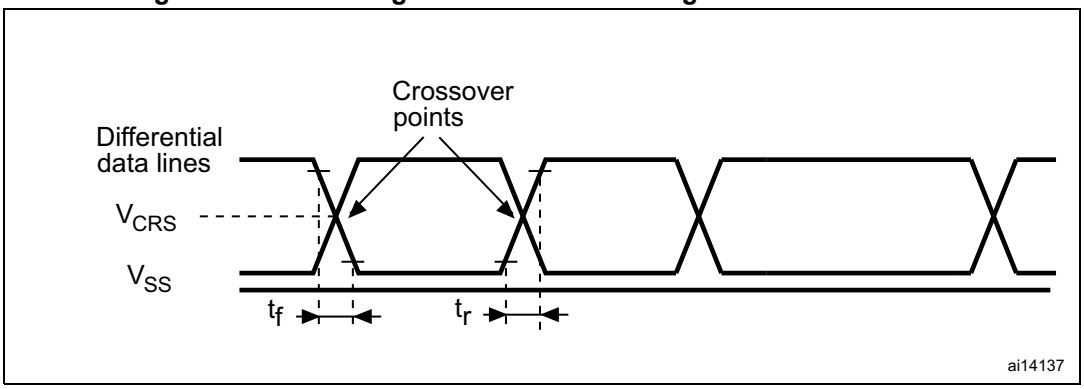
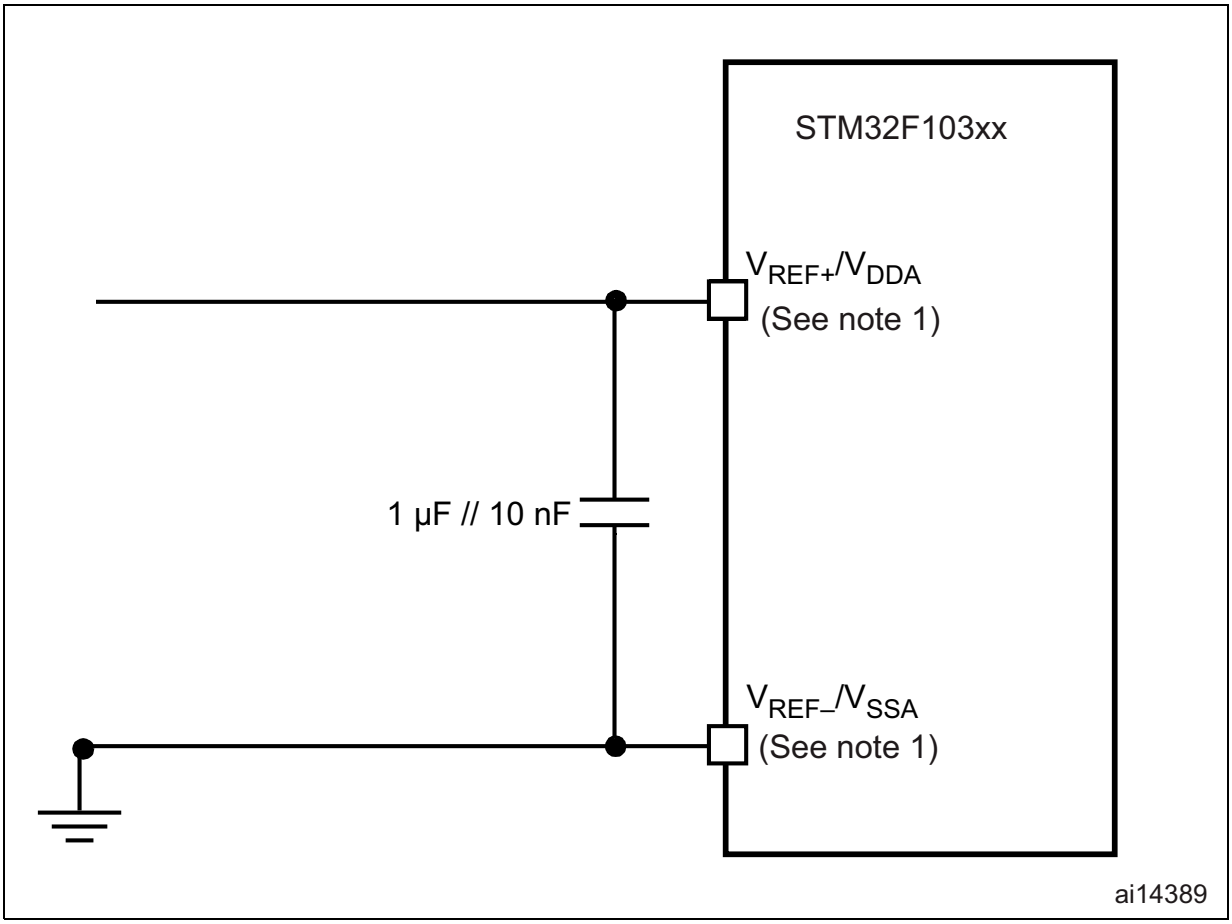


Table 58. USB: full-speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



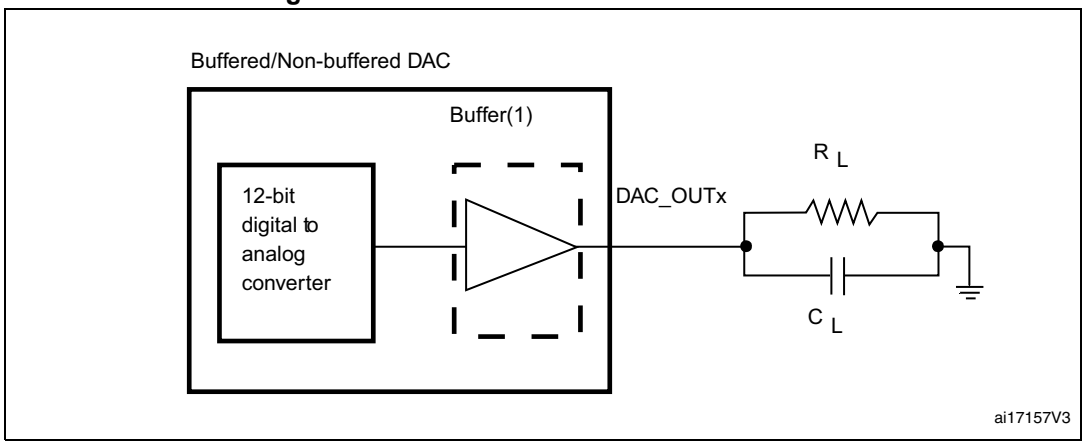
1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

Table 63. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(3)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design.
2. Guaranteed by characterization.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

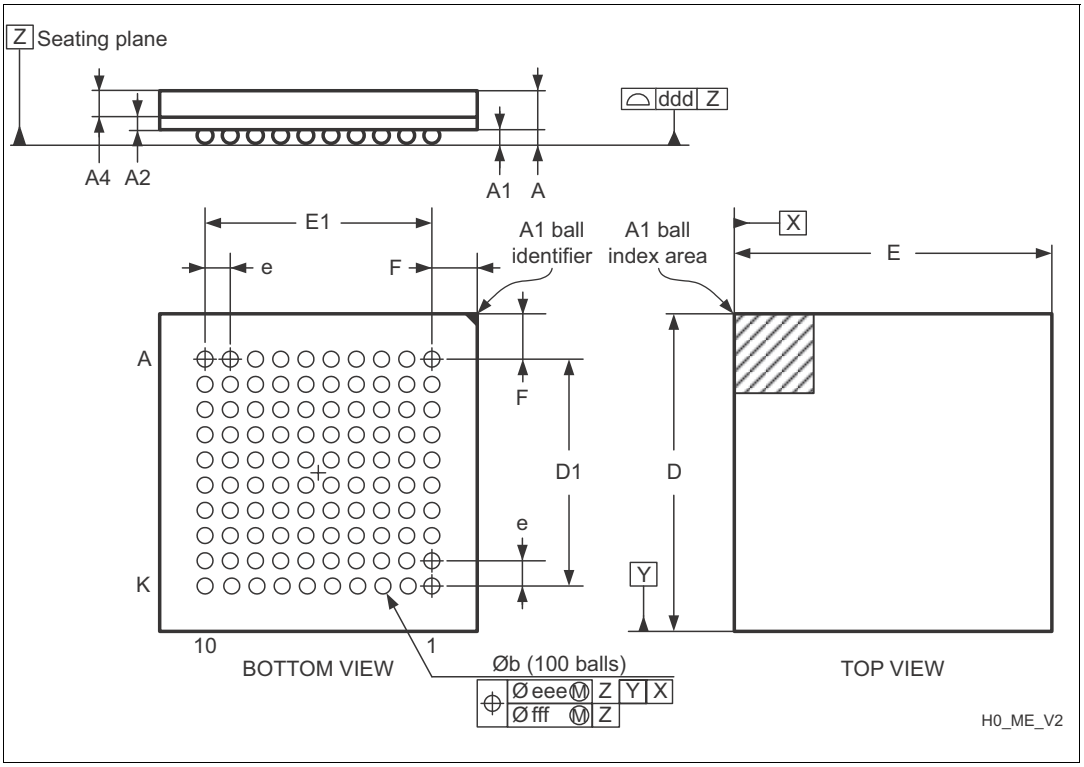
Figure 61. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.2 LFBGA100 package information

Figure 65. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline

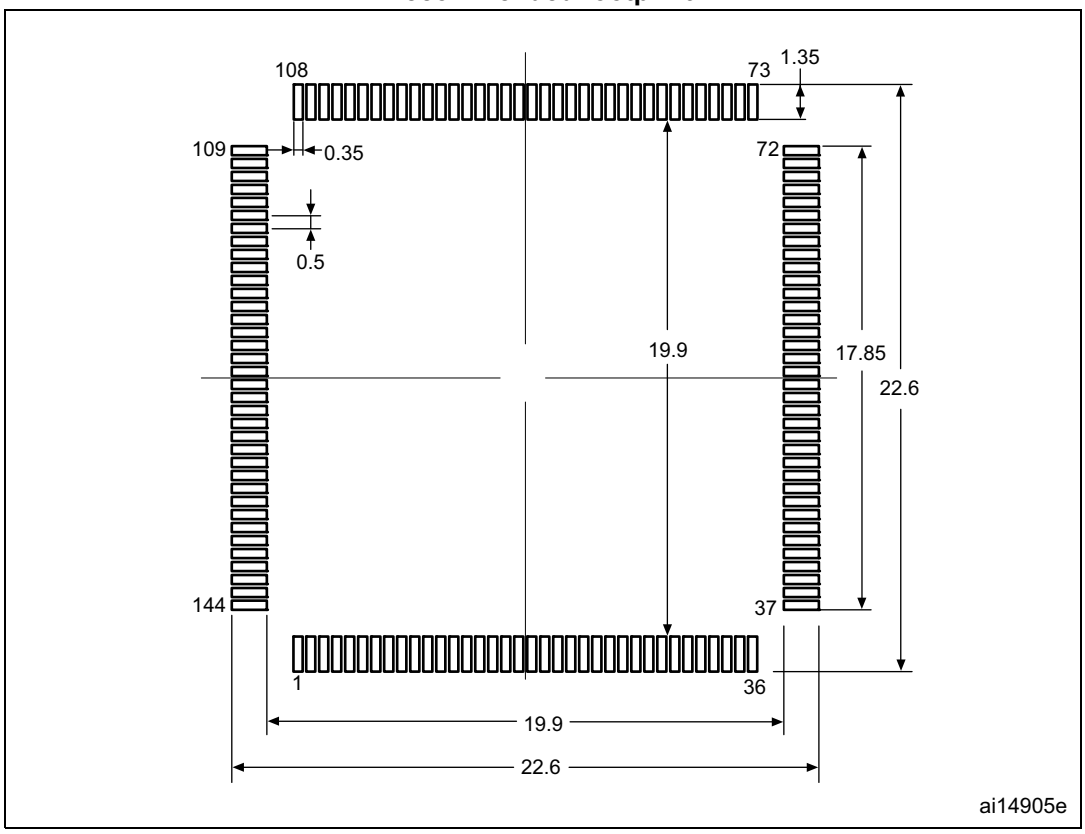


1. Drawing is not to scale.

Table 67. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.700	-	-	0.0669
A1	0.270	-	-	0.0106	-	-
A2	-	0.300	-	-	0.0118	-
A4	-	-	0.800	-	-	0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	7.200	-	-	0.2835	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	1.400	-	-	0.0551	-
ddd	-	-	0.120	-	-	0.0047

Figure 71. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint

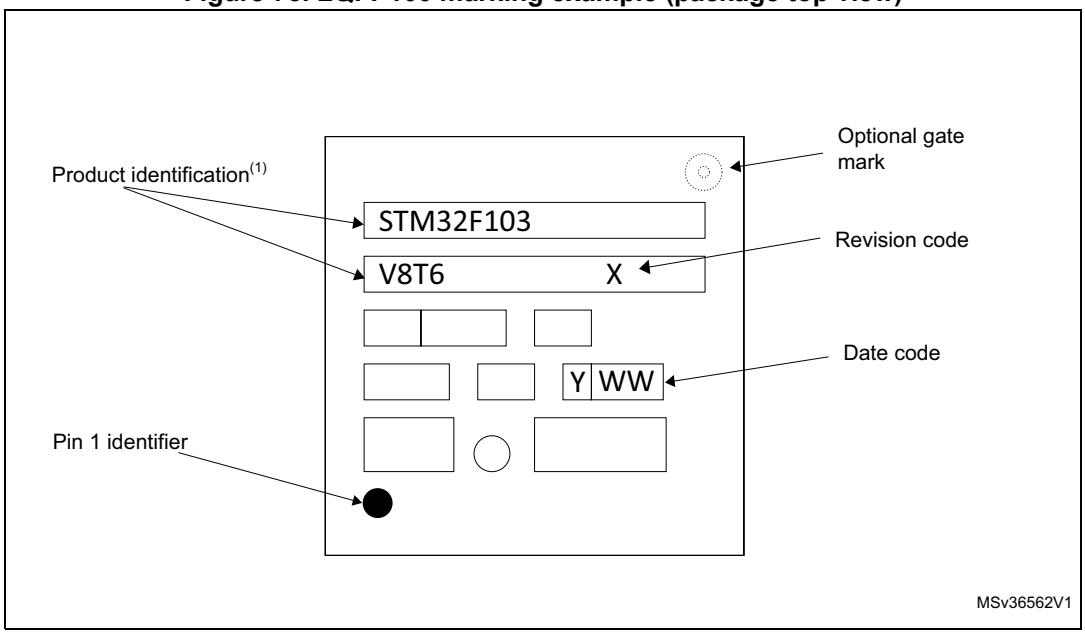


1. Dimensions are expressed in millimeters.

Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 75. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 76.Document revision history

Date	Revision	Changes
31-08-2015	11	Replaced USBDP and USBDM by USB_DP and USB_DM in the whole document. Updated: – Introduction – Reference standard in *Table 43: ESD absolute maximum ratings*. – Updated I_{DDA} description in *Table 63: DAC characteristics*. – *Section : I2C interface characteristics* – *Figure 62: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline* – Updated sentence before *Figure 78: LQFP64 marking example (package top view)*. – *Figure 65: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline* and sentence before *Figure 75: LQFP100 marking example (package top view)* – *Figure 68: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline* – *Figure 48: I2C bus AC waveforms and measurement circuit on page 98* – *Section 6.1: LFBGA144 package information* and *Section 6.2: LFBGA100 package information*. – *Table 20: Peripheral current consumption* Added: – *Figure 63: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint* – *Figure 64: LFBGA144 marking example (package top view)* – *Figure 66: LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprintoutline* – *Figure 69: WLCSP64 - 64-ball, 4.4757 x 4.4049 mm, 0.5 mm pitch wafer level chip scale package recommended footprint* – *Table 66: LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)* – *Table 68: LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)* – *Table 70: WLCSP64 recommended PCB design rules (0.5 mm pitch)*.
26-Nov-2015	12	Updated: – *Table 59: ADC characteristics* – *Table 65: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data* – *Table 66: LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)* Added: – *Note 3* on *Table 7: Voltage characteristics*