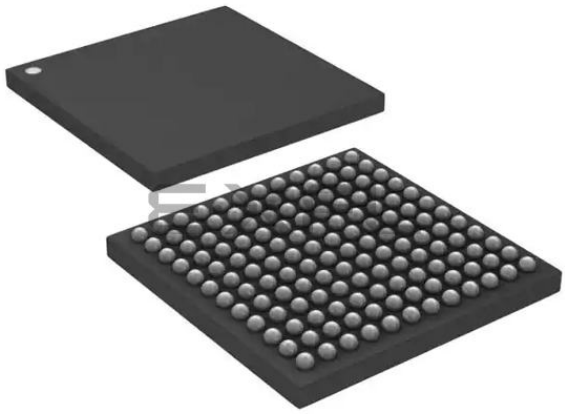

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zdh6

List of tables

Table 1. Device summary . . . 1
Table 2. STM32F103xC, STM32F103xD and STM32F103xE features and peripheral counts . . . 11
Table 3. STM32F103xx family . . . 14
Table 4. High-density timer feature comparison . . . 19
Table 5. High-density STM32F103xC/D/E pin definitions . . . 31
Table 6. FSMC pin definition . . . 38
Table 7. Voltage characteristics . . . 43
Table 8. Current characteristics . . . 43
Table 9. Thermal characteristics . . . 44
Table 10. General operating conditions . . . 44
Table 11. Operating conditions at power-up / power-down . . . 45
Table 12. Embedded reset and power control block characteristics . . . 45
Table 13. Embedded internal reference voltage . . . 46
Table 14. Maximum current consumption in Run mode, code with data processing running from Flash . . . 47
Table 15. Maximum current consumption in Run mode, code with data processing running from RAM . . . 47
Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM . . . 49
Table 17. Typical and maximum current consumptions in Stop and Standby modes . . . 50
Table 18. Typical current consumption in Run mode, code with data processing running from Flash . . . 53
Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM . . . 54
Table 20. Peripheral current consumption . . . 55
Table 21. High-speed external user clock characteristics . . . 58
Table 22. Low-speed external user clock characteristics . . . 58
Table 23. HSE 4-16 MHz oscillator characteristics . . . 60
Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 61
Table 25. HSI oscillator characteristics . . . 62
Table 26. LSI oscillator characteristics . . . 63
Table 27. Low-power mode wakeup timings . . . 63
Table 28. PLL characteristics . . . 64
Table 29. Flash memory characteristics . . . 64
Table 30. Flash memory endurance and data retention . . . 65
Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 67
Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 68
Table 33. Asynchronous multiplexed PSRAM/NOR read timings . . . 69
Table 34. Asynchronous multiplexed PSRAM/NOR write timings . . . 70
Table 35. Synchronous multiplexed NOR/PSRAM read timings . . . 73
Table 36. Synchronous multiplexed PSRAM write timings . . . 75
Table 37. Synchronous non-multiplexed NOR/PSRAM read timings . . . 76
Table 38. Synchronous non-multiplexed PSRAM write timings . . . 77
Table 39. Switching characteristics for PC Card/CF read and write cycles . . . 82
Table 40. Switching characteristics for NAND Flash read and write cycles . . . 86
Table 41. EMS characteristics . . . 87
Table 42. EMI characteristics . . . 88
Table 43. ESD absolute maximum ratings . . . 88

List of figures

Figure 1. STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram . . . 12
Figure 2. Clock tree . . . 13
Figure 3. STM32F103xC/D/E BGA144 ballout . . . 25
Figure 4. STM32F103xC/D/E performance line BGA100 ballout . . . 26
Figure 5. STM32F103xC/D/E performance line LQFP144 pinout . . . 27
Figure 6. STM32F103xC/D/E performance line LQFP100 pinout . . . 28
Figure 7. STM32F103xC/D/E performance line LQFP64 pinout . . . 29
Figure 8. STM32F103xC/D/E performance line WLCSP64 ballout, ball side . . . 30
Figure 9. Memory map . . . 40
Figure 10. Pin loading conditions . . . 41
Figure 11. Pin input voltage . . . 41
Figure 12. Power supply scheme . . . 42
Figure 13. Current consumption measurement scheme . . . 42
Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled . . . 48
Figure 15. Typical current consumption in Run mode versus frequency (at 3.6 V)- code with data processing running from RAM, peripherals disabled . . . 48
Figure 16. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values . . . 50
Figure 17. Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values . . . 51
Figure 18. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values . . . 51
Figure 19. Typical current consumption in Standby mode versus temperature at different V_{DD} values . . . 52
Figure 20. High-speed external clock source AC timing diagram . . . 59
Figure 21. Low-speed external clock source AC timing diagram . . . 59
Figure 22. Typical application with an 8 MHz crystal . . . 60
Figure 23. Typical application with a 32.768 kHz crystal . . . 62
Figure 24. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 66
Figure 25. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 67
Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 69
Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 70
Figure 28. Synchronous multiplexed NOR/PSRAM read timings . . . 72
Figure 29. Synchronous multiplexed PSRAM write timings . . . 74
Figure 30. Synchronous non-multiplexed NOR/PSRAM read timings . . . 76
Figure 31. Synchronous non-multiplexed PSRAM write timings . . . 77
Figure 32. PC Card/CompactFlash controller waveforms for common memory read access . . . 78
Figure 33. PC Card/CompactFlash controller waveforms for common memory write access . . . 79
Figure 34. PC Card/CompactFlash controller waveforms for attribute memory read access . . . 80
Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access . . . 81
Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access . . . 81
Figure 37. PC Card/CompactFlash controller waveforms for I/O space write access . . . 82
Figure 38. NAND controller waveforms for read access . . . 84
Figure 39. NAND controller waveforms for write access . . . 85

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from

the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.21 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I^2S interfaces is/are configured in master

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.3.27 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

Figure 8. STM32F103xC/D/E performance line WLCSP64 ballout, ball side

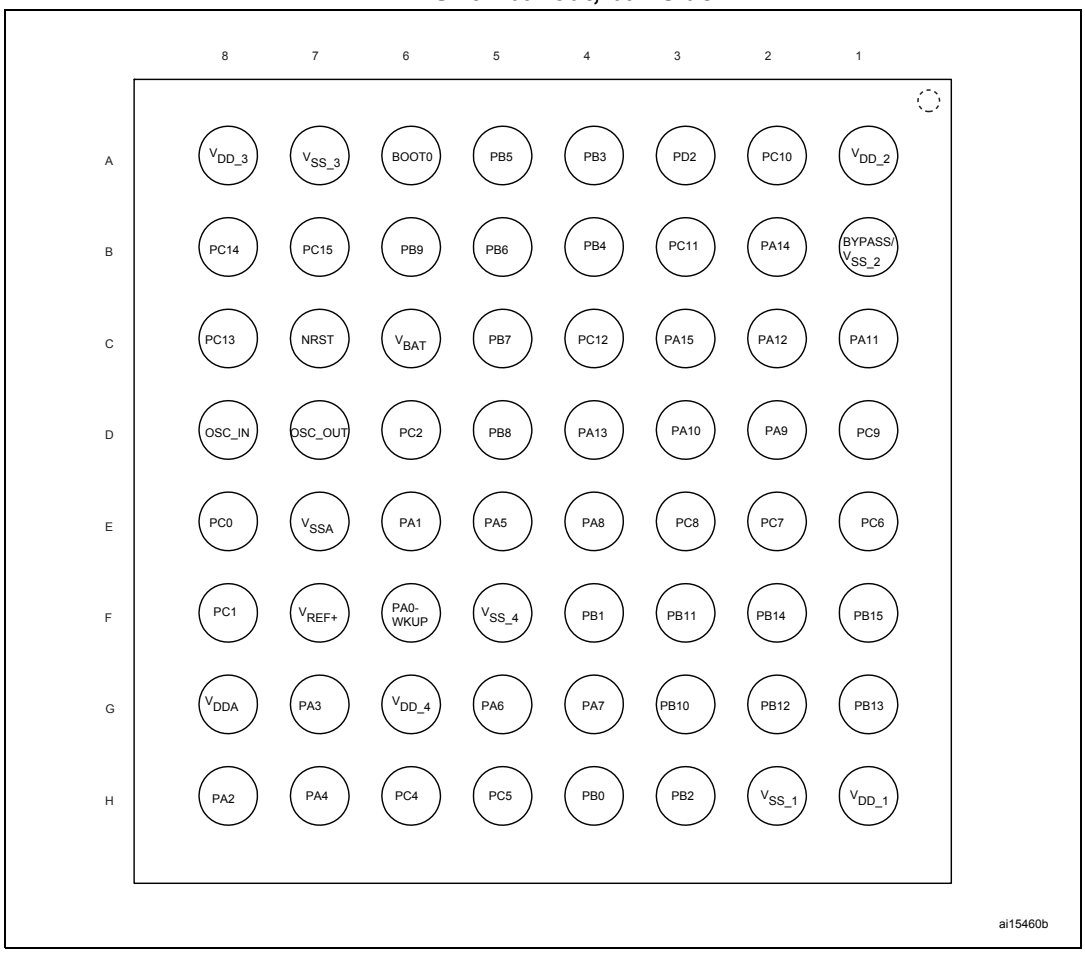
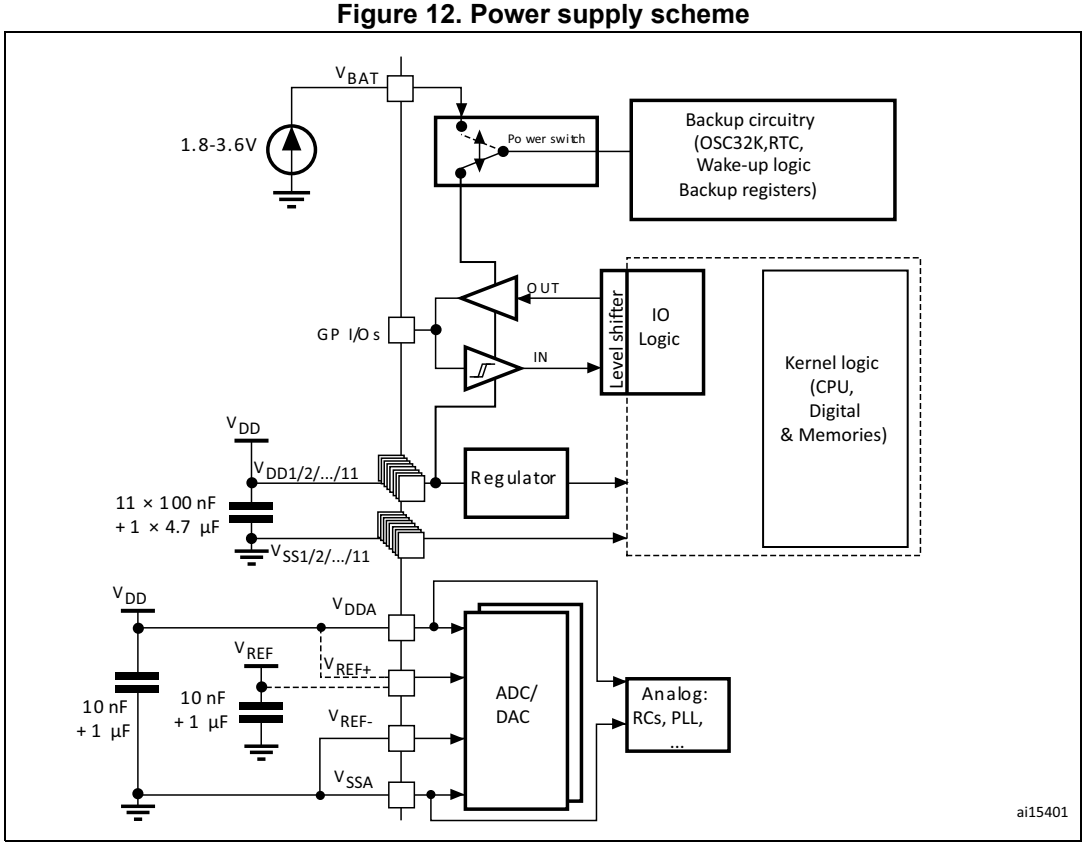


Table 5. High-density STM32F103xC/D/E pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A3	A3	-	-	1	1	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	-
A2	B3	-	-	2	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
B2	C3	-	-	3	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
B3	D3	-	-	4	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
B4	E3	-	-	5	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
C2	B2	C6	1	6	6	V_{BAT}	S	-	V_{BAT}	-	-
A1	A2	C8	2	7	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
B1	A1	B8	3	8	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
C1	B1	B7	4	9	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
C3	-	-	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	-
C4	-	-	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	-
D4	-	-	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	-
E2	-	-	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	-
E3	-	-	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	-
E4	-	-	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	-
D2	C2	-	-	10	16	V_{SS_5}	S	-	V_{SS_5}	-	-
D3	D2	-	-	11	17	V_{DD_5}	S	-	V_{DD_5}	-	-
F3	-	-	-	-	18	PF6	I/O	-	PF6	ADC3_IN4/FSMC_NIORD	-
F2	-	-	-	-	19	PF7	I/O	-	PF7	ADC3_IN5/FSMC_NREG	-
G3	-	-	-	-	20	PF8	I/O	-	PF8	ADC3_IN6/FSMC_NIOWR	-
G2	-	-	-	-	21	PF9	I/O	-	PF9	ADC3_IN7/FSMC_CD	-
G1	-	-	-	-	22	PF10	I/O	-	PF10	ADC3_IN8/FSMC_INTR	-
D1	C1	D8	5	12	23	OSC_IN	I	-	OSC_IN	-	-
E1	D1	D7	6	13	24	OSC_OUT	O	-	OSC_OUT	-	-
F1	E1	C7	7	14	25	NRST	I/O	-	NRST	-	-
H1	F1	E8	8	15	26	PC0	I/O	-	PC0	ADC123_IN10	-
H2	F2	F8	9	16	27	PC1	I/O	-	PC1	ADC123_IN11	-

5.1.6 Power supply scheme

Figure 12. Power supply scheme



Caution: In *Figure 12*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme

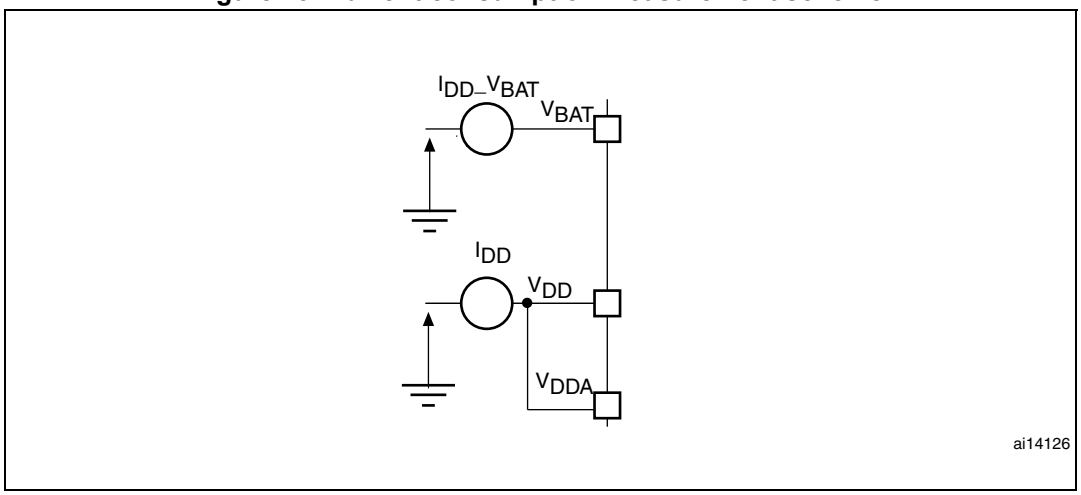


Table 35. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.7	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 33. PC Card/CompactFlash controller waveforms for common memory write access

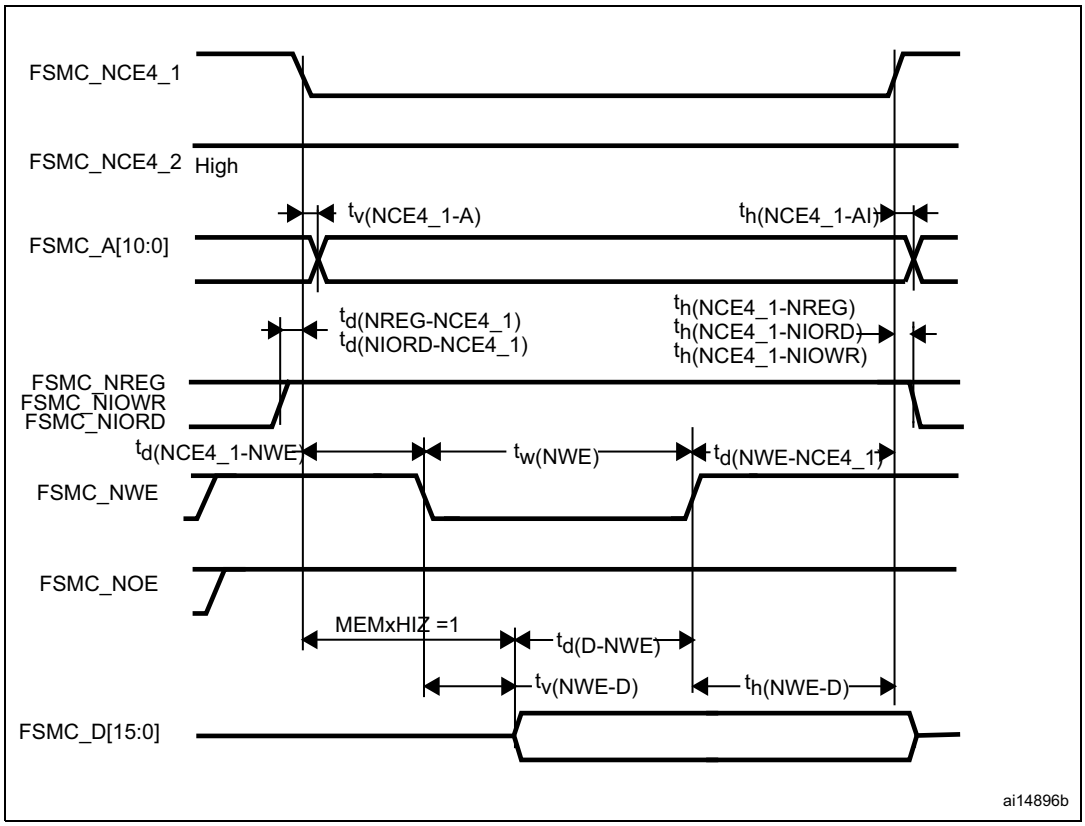
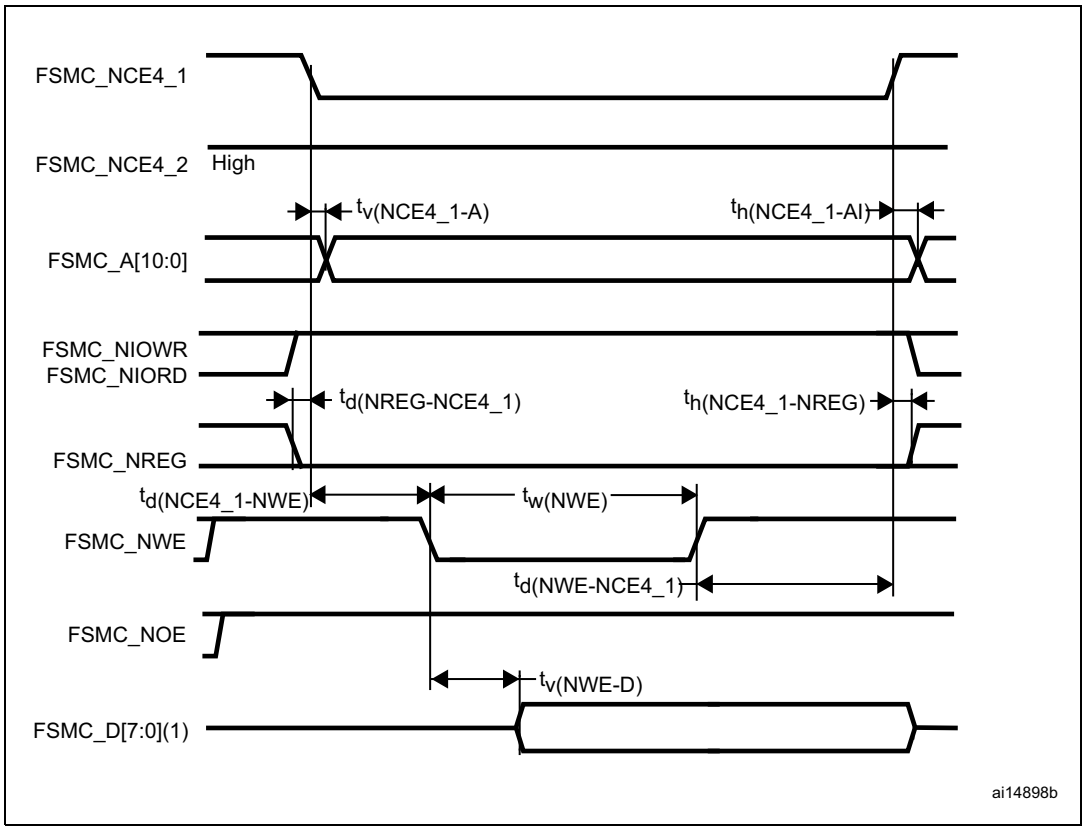
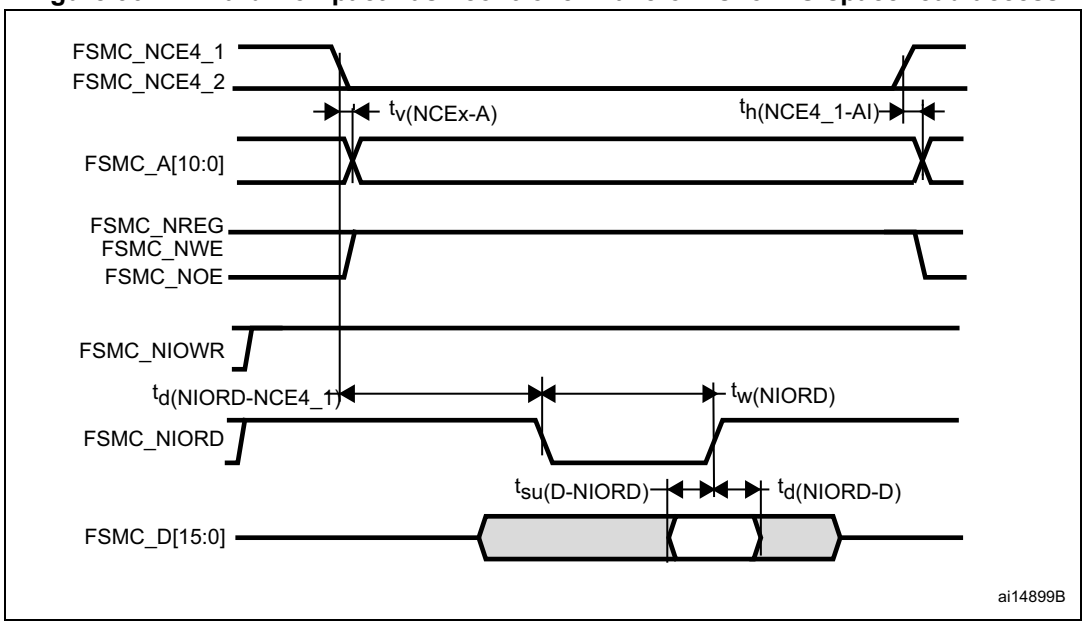


Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access



5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

Table 47. Output voltage characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results.

5.3.18 CAN (controller area network) interface

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 59* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 60* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

5.3.21 Temperature sensor characteristics

Table 64. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 67. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 66. LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprintoutline

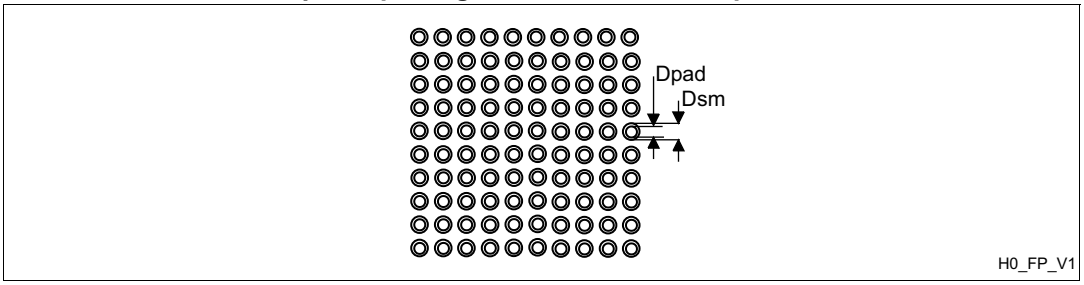


Table 68. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

7 Part numbering

Table 75. Ordering information scheme

Example: STM32 F 103 R C T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

103 = performance line

Pin count

R = 64 pins
V = 100 pins
Z = 144 pins

Flash memory size

C = 256 Kbytes of Flash memory
D = 384 Kbytes of Flash memory
E = 512 Kbytes of Flash memory

Package

H = BGA
T = LQFP
Y = WLCSP64

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 76.Document revision history

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified *on page 1*. *Figure 4: STM32F103xC and STM32F103xE performance line BGA100 ballout* corrected. I/O information clarified *on page 1*. In *Table 5: High-density STM32F103xx pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column PG14 pin description modified in *Table 6: FSMC pin definition*. *Figure 9: Memory map on page 54* modified. Note modified in *Table 18: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 20: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 17*, *Figure 18* and *Figure 19* show typical curves (titles changed). *Table 25: High-speed external user clock characteristics* and *Table 26: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 29: HSI oscillator characteristics*. FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 24: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 25: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 35: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 39: Asynchronous multiplexed PSRAM/NOR write timings*. $t_{h(Data\_NWE)}$ modified in *Table 36: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings* In *Table 41: Synchronous multiplexed PSRAM write timings* and *Table 43: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 28: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 29: Synchronous multiplexed PSRAM write timings* and *Figure 31: Synchronous non-multiplexed PSRAM write timings* modified. *Figure 52: I2S slave timing diagram (Philips protocol)(1)* and *Figure 53: I2S master timing diagram (Philips protocol)(1)* modified. WLCSP64 package added (see *Figure 8: STM32F103xC and STM32F103xE performance line WLCSP64 ballout, ball side*, *Table 8: High-density STM32F103xx pin definitions*, *Figure 65: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline* and *Table 76: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data*). Small text changes.

Table 76.Document revision history

Date	Revision	Changes
19-Apr-2011	8	Updated package choice for 103Rx in *Table 2* Updated footnotes below *Table 7: Voltage characteristics on page 43* and *Table 8: Current characteristics on page 43* Updated tw min in *Table 21: High-speed external user clock characteristics on page 58* Updated startup time in *Table 24: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 61* Updated note 2 in *Table 51: I2C characteristics on page 97* Updated *Figure 48: I2C bus AC waveforms and measurement circuit* Updated *Figure 47: Recommended NRST pin protection* Updated *Section 5.3.14: I/O port characteristics* Updated *Table 35: Synchronous multiplexed NOR/PSRAM read timings on page 73* Updated FSMC *Figure 26* thru *Figure 31* Updated *Figure 41.: NAND controller waveforms for common memory write access* and *Figure 48.: I2C bus AC waveforms and measurement circuit* Added *Section 5.3.13: I/O current injection characteristics* Updated *Figure 67* and added *Table 69: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data on page 121* LQFP64 package mechanical data updated: see *Figure 73.: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 73: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data on page 130*.
30-Sept-2014	9	Added *Note 7* in *Table 5: High-density STM32F103xC/D/E pin definitions on page 31*. Updated *Note 10* in *Table 5: High-density STM32F103xC/D/E pin definitions on page 31*. Modified *Note 2* in *Table 62: ADC accuracy on page 109* Modified *Note 3* in *Table 62: ADC accuracy on page 109* Modified notes in *Table 51: I2C characteristics on page 97* Updated *Figure 51: SPI timing diagram - master mode(1) on page 101*
23-Feb-2015	10	Updated *Figure 66.: BGA pad footprint*, *Figure 70: LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline*, *Figure 73.: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 74.: LQFP100 recommended footprint*, *Figure 76.: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 77.: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* Added *Figure 72.: LQFP144 marking example (package top view)*, *Figure 75.: LQFP100 marking example (package top view)*, *Figure 78.: LQFP64 marking example (package top view)* Updated *Table 72: LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*