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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zeh6

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xC, STM32F103xD and STM32F103xE high-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xC/D/E family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The high-density STM32F103xC/D/E datasheet should be read in conjunction with the STM32F10xxx reference manual.

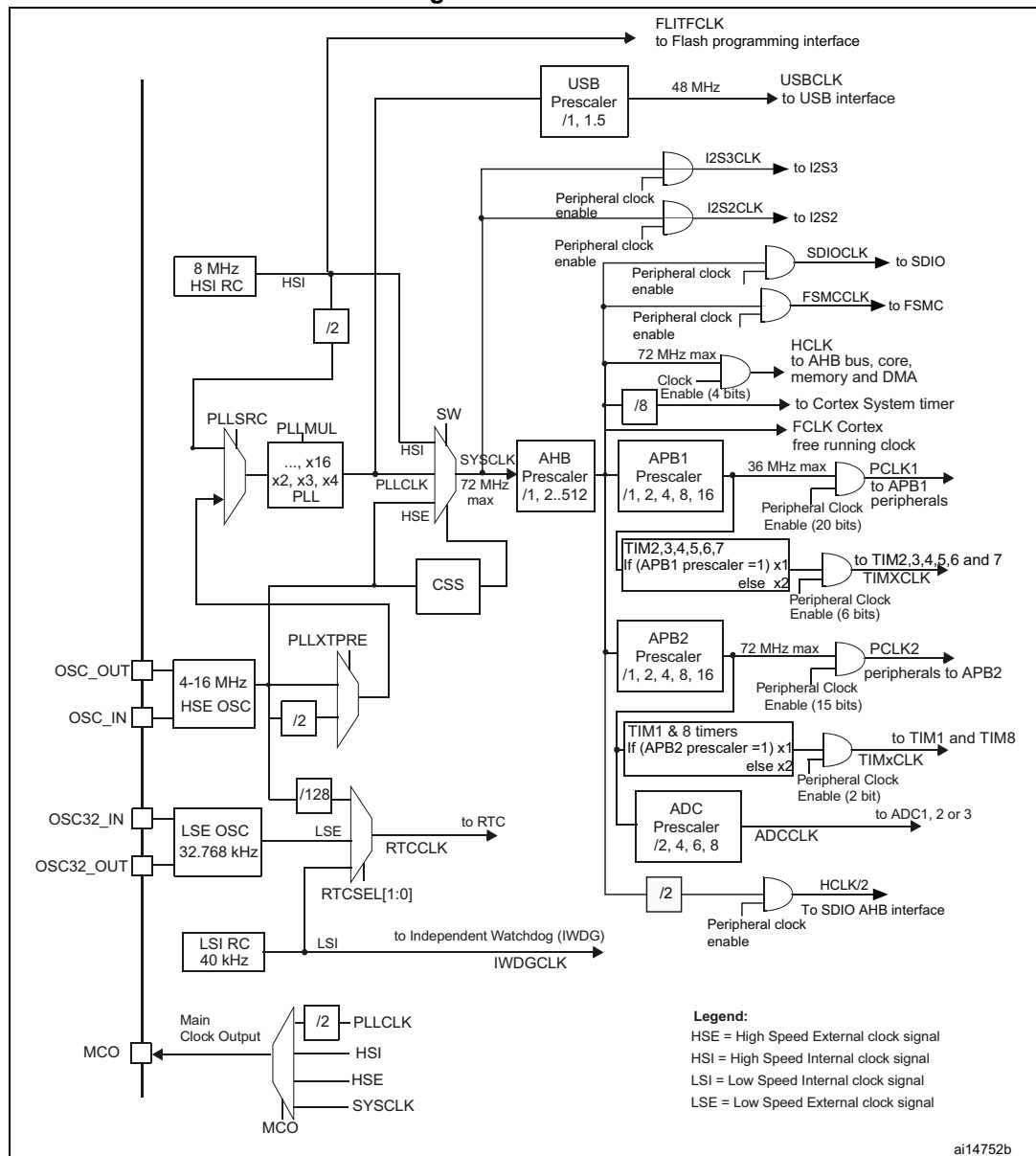
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex[®]-M3 core please refer to the Cortex[®]-M3 Technical Reference Manual, available from the www.arm.com website at the following address:
<http://infocenter.arm.com>.



Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the USBCLK at 48 MHz.
3. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

2.2 Full compatibility throughout the family

The STM32F103xC/D/E is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices and the STM32F103xC, STM32F103xD and STM32F103xE are referred to as high-density devices.

Low-density and high-density devices are an extension of the STM32F103x8/B medium-density devices, they are specified in the STM32F103x4/6 and STM32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I²S and DAC while remaining fully compatible with the other members of the family.

The STM32F103x4, STM32F103x6, STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for the STM32F103x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F103xx family

Pinout	Low-density devices		Medium-density devices		High-density devices		
	16 KB Flash	32 KB Flash ⁽¹⁾	64 KB Flash	128 KB Flash	256 KB Flash	384 KB Flash	512 KB Flash
	6 KB RAM	10 KB RAM	20 KB RAM	20 KB RAM	48 RAM	64 KB RAM	64 KB RAM
144					5 × USARTs 4 × 16-bit timers, 2 × basic timers 3 × SPIs, 2 × I ² Ss, 2 × I ² Cs USB, CAN, 2 × PWM timers 3 × ADCs, 2 × DACs, 1 × SDIO FSMC (100- and 144-pin packages ⁽²⁾)		
100							
64	2 × USARTs 2 × 16-bit timers 1 × SPI, 1 × I ² C, USB, CAN, 1 × PWM timer 2 × ADCs		3 × USARTs 3 × 16-bit timers 2 × SPIs, 2 × I ² Cs, USB, CAN, 1 × PWM timer 2 × ADCs				
48							
36							

- For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.
- Ports F and G are not available in devices delivered in 100-pin packages.

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xC, STM32F103xD and STM32F103xE performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK} , is $HCLK/2$, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from

2.3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

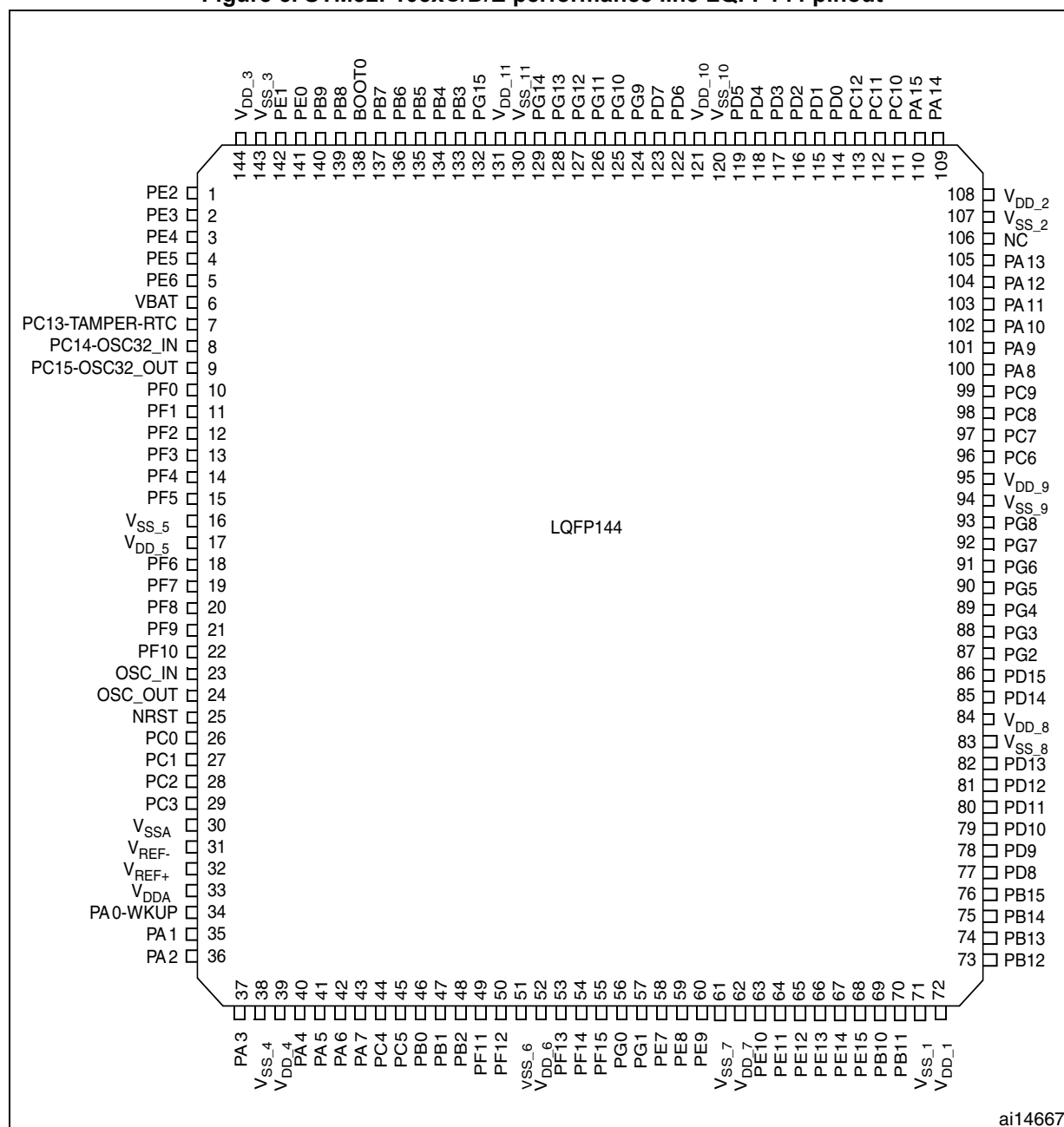
2.3.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.30 Embedded Trace Macrocell™

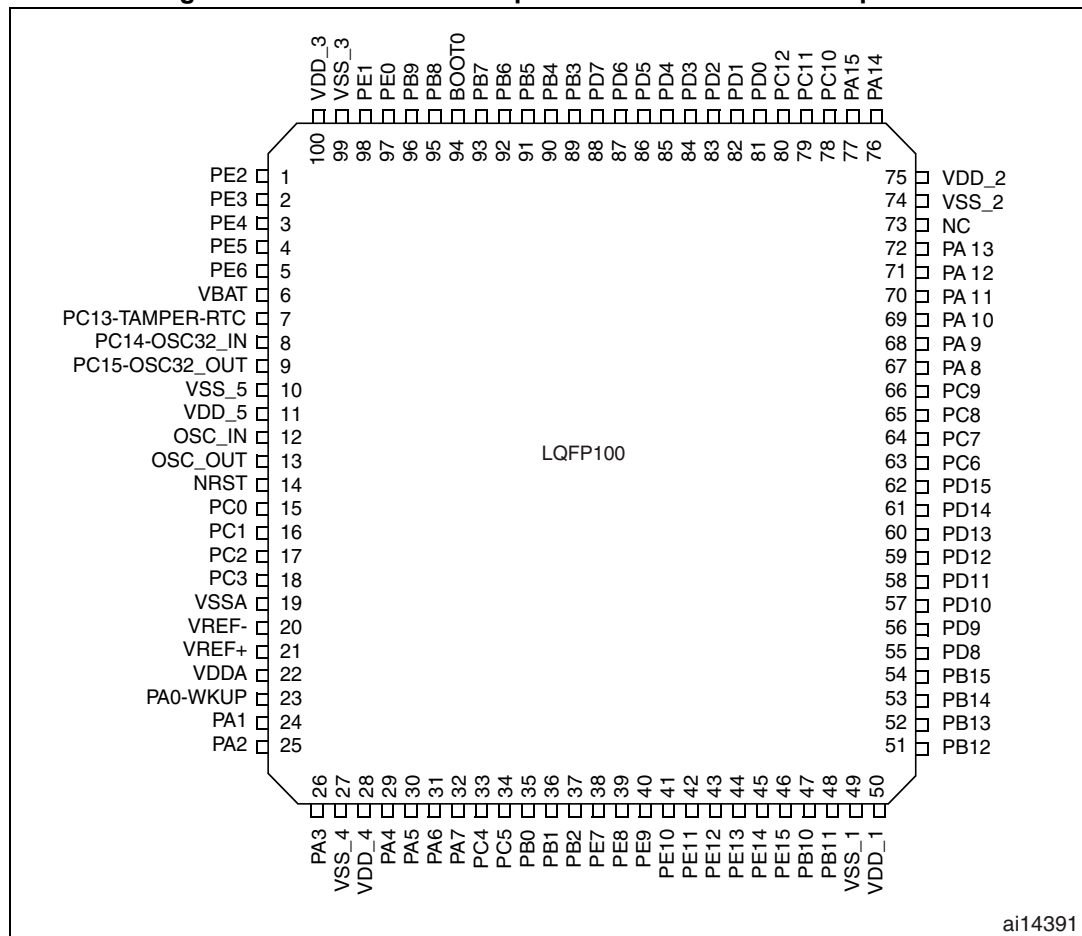
The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 5. STM32F103xC/D/E performance line LQFP144 pinout



1. The above figure shows the package top view.

Figure 6. STM32F103xC/D/E performance line LQFP100 pinout



1. The above figure shows the package top view.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 7: Voltage characteristics](#), [Table 8: Current characteristics](#), and [Table 9: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN} ⁽²⁾	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins ⁽³⁾	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 5.3.12: Absolute maximum ratings (electrical sensitivity)		-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 8: Current characteristics](#) for the maximum allowed injected current values.
3. Include V_{REF} pin.

Table 8. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ ⁽²⁾	Injected current on five volt tolerant pins ⁽³⁾	-5/+0	
	Injected current on any other pin ⁽⁴⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁵⁾	± 25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note 3 below [Table 62 on page 109](#).
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 7: Voltage characteristics](#) for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 7: Voltage characteristics](#) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 11](#) are derived from tests performed under the ambient temperature condition summarized in [Table 10](#).

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 12](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 ⁽¹⁾	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}^{(2)}$	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design.

Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM

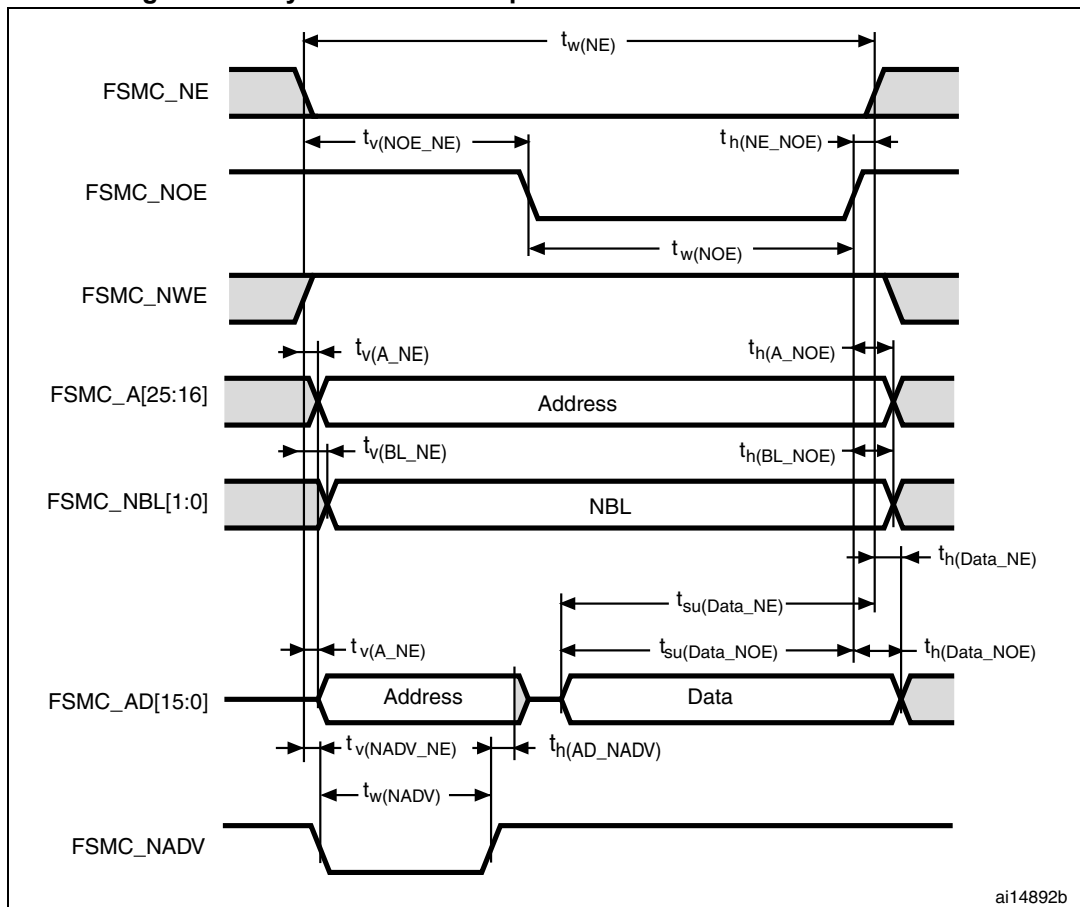
Symbol	Parameter	Conditions	f_{HCLK}	Typ ⁽¹⁾		Unit
				All peripherals enabled ⁽²⁾	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock ⁽³⁾	72 MHz	29.5	6.4	mA
			48 MHz	20	4.6	
			36 MHz	15.1	3.6	
			24 MHz	10.4	2.6	
			16 MHz	7.2	2	
			8 MHz	3.9	1.3	
			4 MHz	2.6	1.2	
			2 MHz	1.85	1.15	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
			125 kHz	1.2	1.05	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	25.6	5.1	
			48 MHz	19.4	4	
			36 MHz	14.5	3	
			24 MHz	9.8	2	
			16 MHz	6.6	1.4	
			8 MHz	3.3	0.7	
			4 MHz	2	0.6	
			2 MHz	1.25	0.55	
			1 MHz	0.9	0.5	
			500 kHz	0.7	0.45	
			125 kHz	0.6	0.45	

1. Typical values are measures at $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$.

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8\text{ MHz}$.

Figure 26. Asynchronous multiplexed PSRAM/NOR read waveforms



ai14892b

Table 33. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FSMC_NE low time	$7t_{HCLK} - 2$	$7t_{HCLK} + 2$	ns
$t_v(NOE_NE)$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1.5$	ns
$t_w(NOE)$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 2$	ns
$t_h(NE_NOE)$	FSMC_NOE high to FSMC_NE high hold time	-1	-	ns
$t_v(A_NE)$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_v(NADV_NE)$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_w(NADV)$	FSMC_NADV low time	$t_{HCLK} - 1.5$	$t_{HCLK} + 1.5$	ns
$t_h(AD_NADV)$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_h(A_NOE)$	Address hold time after FSMC_NOE high	$t_{HCLK} - 2$	-	ns
$t_h(BL_NOE)$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_v(BL_NE)$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su}(Data_NE)$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 24$	-	ns
$t_{su}(Data_NOE)$	Data to FSMC_NOE high setup time	$2t_{HCLK} + 25$	-	ns

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 46](#) are derived from tests performed under the conditions summarized in [Table 10](#). All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	-0.3	-	$0.28 \cdot (V_{DD} - 2 \text{ V}) + 0.8 \text{ V}$	V
	IO FT ⁽¹⁾ input low level voltage		-0.3	-	$0.32 \cdot (V_{DD} - 2 \text{ V}) + 0.75 \text{ V}$	V
V_{IH}	Standard IO input high level voltage	-	$0.41 \cdot (V_{DD} - 2 \text{ V}) + 1.3 \text{ V}$	-	$V_{DD} + 0.3$	V
	IO FT ⁽¹⁾ input high level voltage	$V_{DD} > 2 \text{ V}$	$0.42 \cdot (V_{DD} - 2 \text{ V}) + 1 \text{ V}$	-	5.5	V
		$V_{DD} \leq 2 \text{ V}$			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis ⁽²⁾	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis ⁽²⁾		$5\% V_{DD}^{(3)}$	-	-	mV
I_{Ikg}	Input leakage current ⁽⁴⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	± 1	μA
		$V_{IN} = 5 \text{ V}$, I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	30	40	50	k Ω
C_{IO}	I/O pin capacitance	-	-	5	-	pF

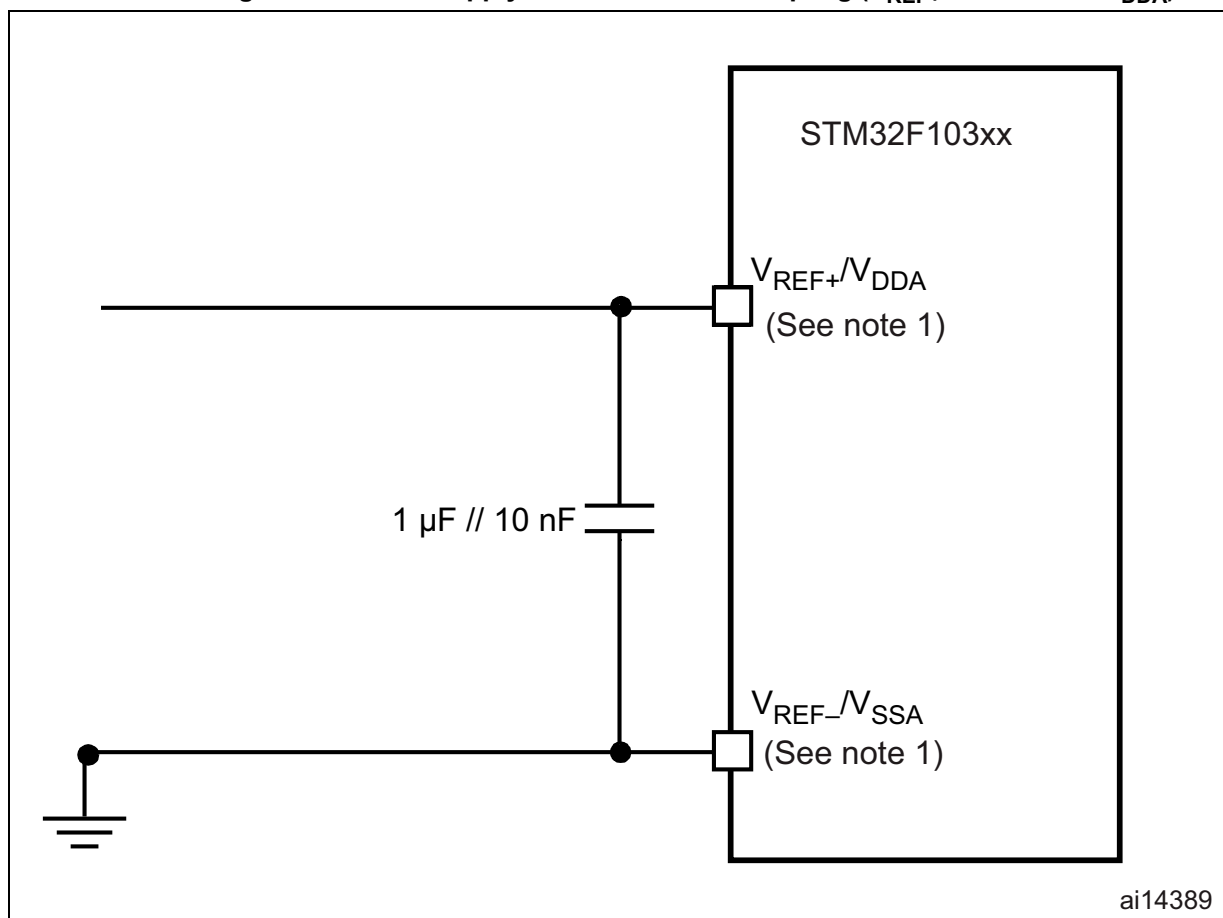
1. FT = Five-volt tolerant. In order to sustain a voltage higher than $V_{DD} + 0.3$ the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 42](#) and [Figure 43](#) for standard I/Os, and in [Figure 44](#) and [Figure 45](#) for 5 V tolerant I/Os.

Table 47. Output voltage characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(2)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(2)(4)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$	-	

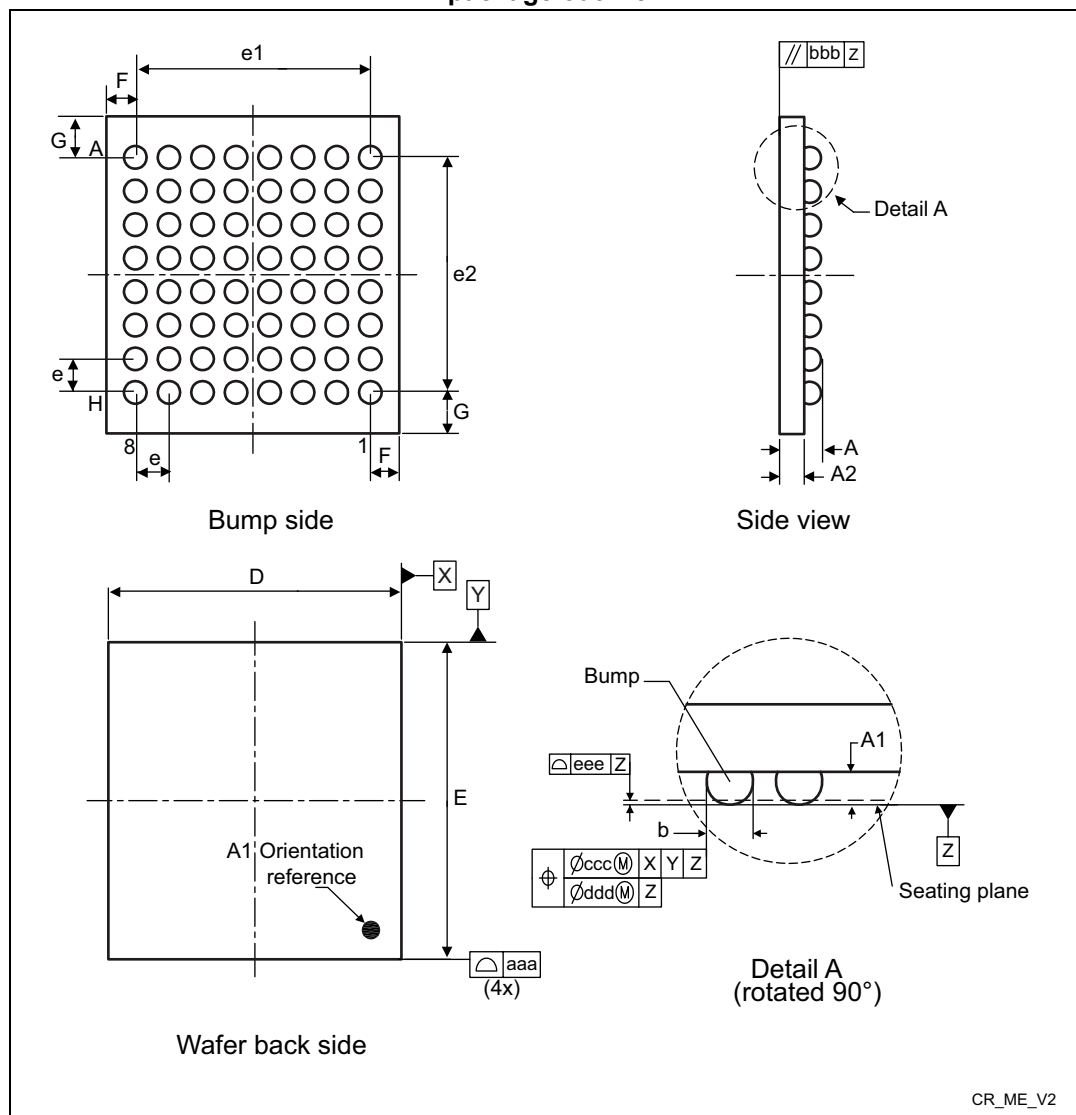
1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 8](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 8](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results.

Figure 60. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

6.3 WLCSP64 package information

Figure 68. WLCSP, 64-ball 4.466×4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline



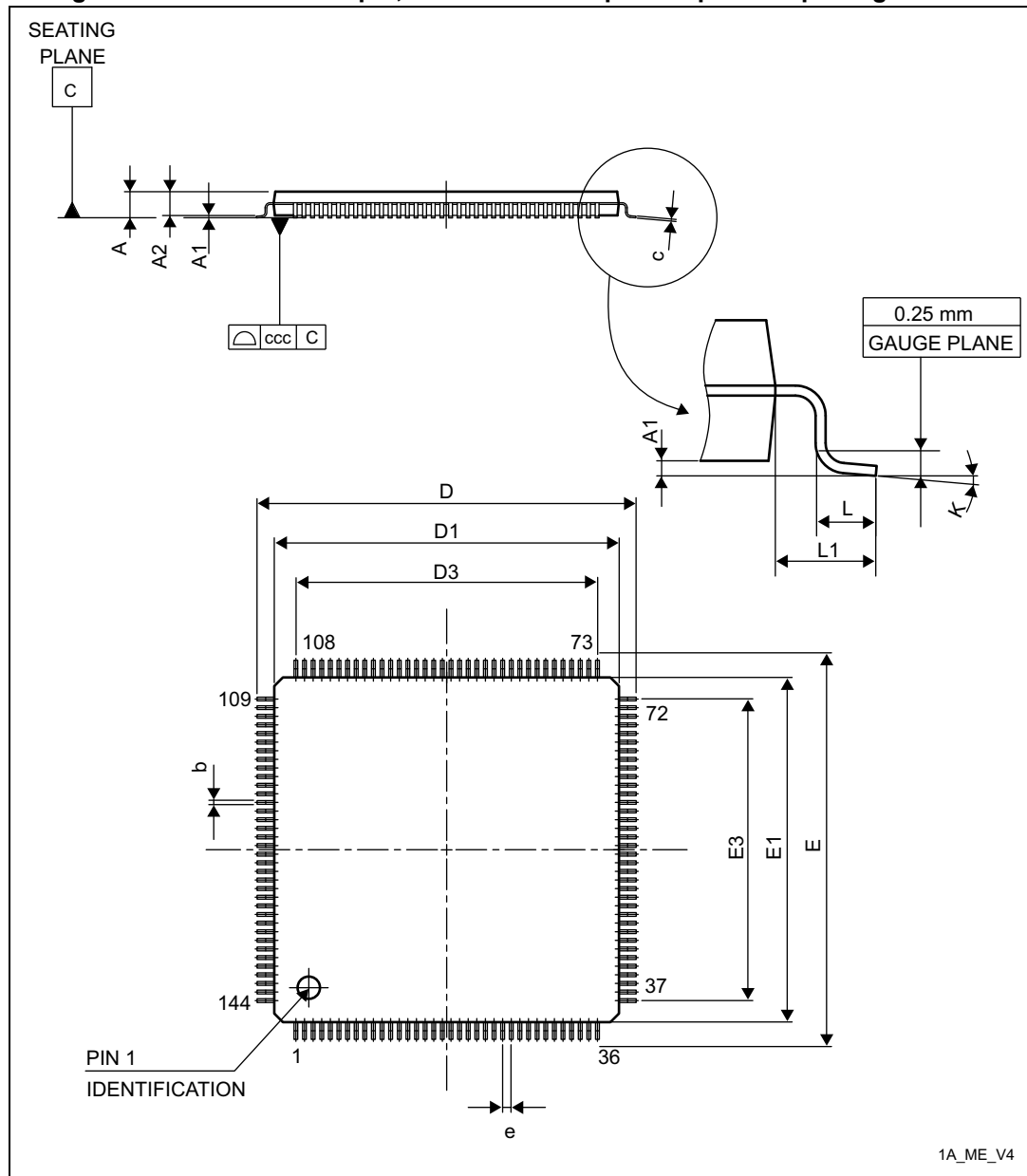
1. Drawing is not to scale.
2. Primary datum Z and seating plane are defined by the spherical crowns of the ball.

Table 69. WLCSP, 64-ball 4.466×4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.535	0.585	0.635	0.0211	0.0230	0.0250
A1	0.205	0.230	0.255	0.0081	0.0091	0.0100
A2	0.330	0.355	0.380	0.0130	0.0140	0.0150
b ⁽²⁾	0.290	0.320	0.350	0.0114	0.0126	0.0138

6.4 LQFP144 package information

Figure 70. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

6.7 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 10: General operating conditions on page 44](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LFBGA144 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	30	
	Thermal resistance junction-ambient LFBGA100 - 10 × 10 mm / 0.8 mm pitch	40	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient WLCSP64	50	

6.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

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