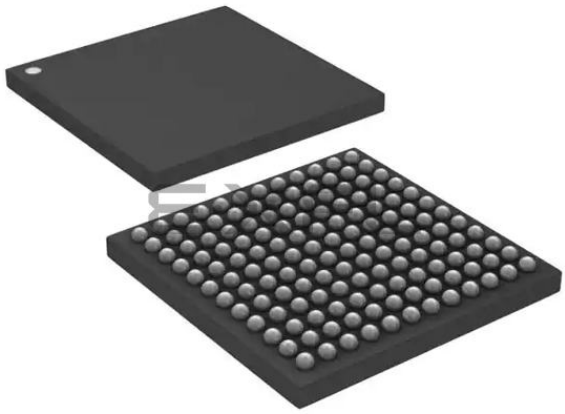

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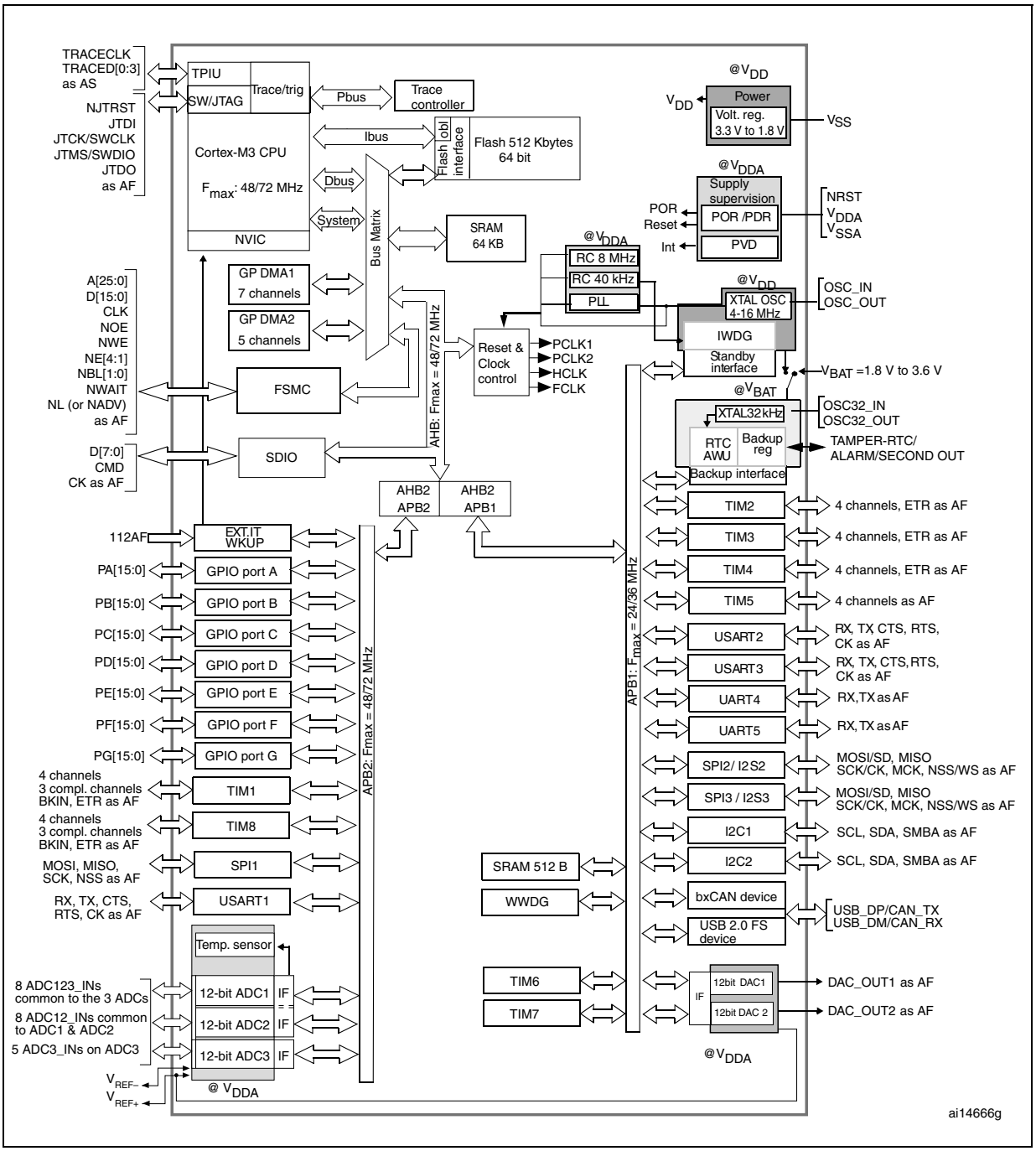
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zeh7

Figure 1. STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 75*) or –40 °C to +105 °C (suffix 7, see *Table 75*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.9

periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.17 Timers and watchdogs

The high-density STM32F103xC/D/E performance line devices include up to two advanced-control timers, up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. High-density timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 5. High-density STM32F103xC/D/E pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A3	A3	-	-	1	1	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	-
A2	B3	-	-	2	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
B2	C3	-	-	3	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
B3	D3	-	-	4	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
B4	E3	-	-	5	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
C2	B2	C6	1	6	6	V_{BAT}	S	-	V_{BAT}	-	-
A1	A2	C8	2	7	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
B1	A1	B8	3	8	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
C1	B1	B7	4	9	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
C3	-	-	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	-
C4	-	-	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	-
D4	-	-	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	-
E2	-	-	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	-
E3	-	-	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	-
E4	-	-	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	-
D2	C2	-	-	10	16	V_{SS_5}	S	-	V_{SS_5}	-	-
D3	D2	-	-	11	17	V_{DD_5}	S	-	V_{DD_5}	-	-
F3	-	-	-	-	18	PF6	I/O	-	PF6	ADC3_IN4/FSMC_NIORD	-
F2	-	-	-	-	19	PF7	I/O	-	PF7	ADC3_IN5/FSMC_NREG	-
G3	-	-	-	-	20	PF8	I/O	-	PF8	ADC3_IN6/FSMC_NIOWR	-
G2	-	-	-	-	21	PF9	I/O	-	PF9	ADC3_IN7/FSMC_CD	-
G1	-	-	-	-	22	PF10	I/O	-	PF10	ADC3_IN8/FSMC_INTR	-
D1	C1	D8	5	12	23	OSC_IN	I	-	OSC_IN	-	-
E1	D1	D7	6	13	24	OSC_OUT	O	-	OSC_OUT	-	-
F1	E1	C7	7	14	25	NRST	I/O	-	NRST	-	-
H1	F1	E8	8	15	26	PC0	I/O	-	PC0	ADC123_IN10	-
H2	F2	F8	9	16	27	PC1	I/O	-	PC1	ADC123_IN11	-

Table 6. FSMC pin definition

Pins	FSMC					LQFP100 BGA100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 8: Current characteristics* for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 8. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note 3 below *Table 62 on page 109*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 20*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 7*

Table 20. Peripheral current consumption

Peripheral		Current consumption	Unit
AHB (up to 72 MHz)	DMA1	20,42	µA/MHz
	DMA2	19,03	
	FSMC	52,36	
	CRC	2,36	
	SDIO	33,33	
	BusMatrix(1)	9,72	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

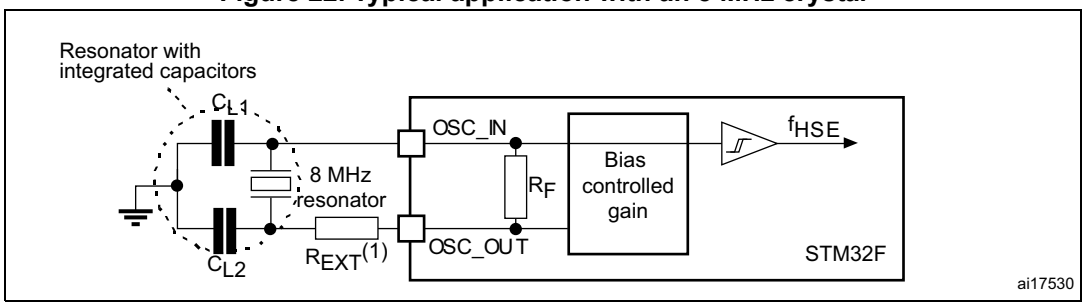
Table 23. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 22*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 22. Typical application with an 8 MHz crystal



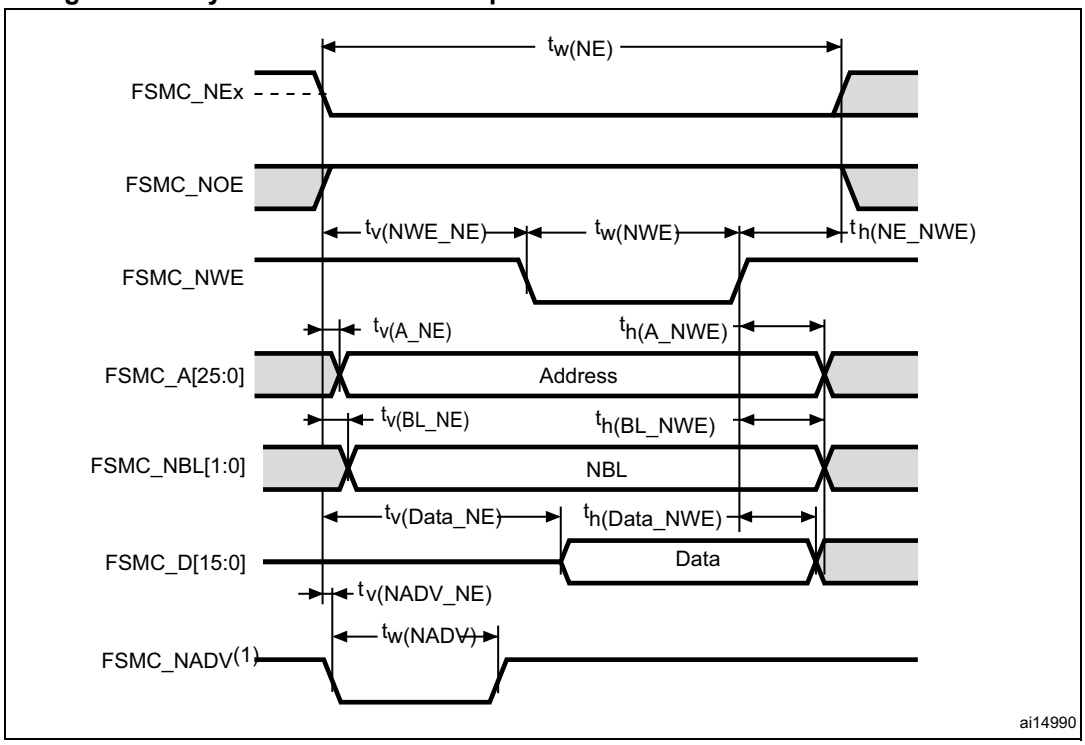
1. R_{EXT} value depends on the crystal characteristics.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$t_{HCLK} + 1.5$	ns

1. C_L = 15 pF.

Figure 25. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 33. Asynchronous multiplexed PSRAM/NOR read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 27. Asynchronous multiplexed PSRAM/NOR write waveforms

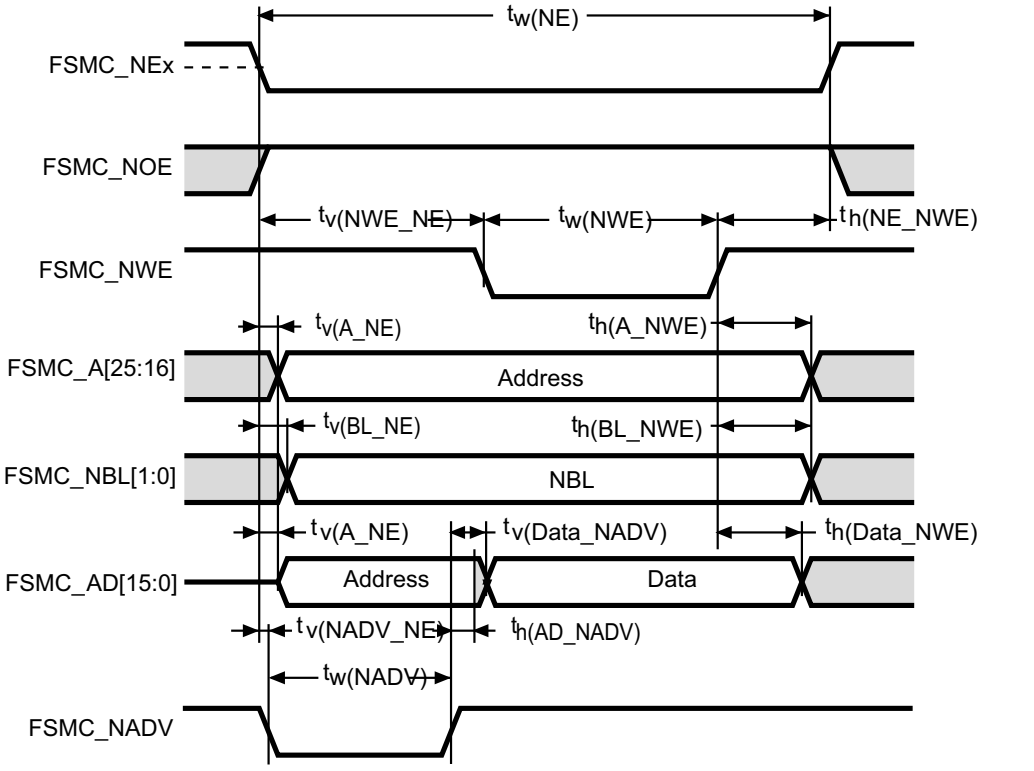


Table 34. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1$	$5t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$2t_{HCLK}$	$2t_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2t_{HCLK} - 1$	$2t_{HCLK} + 2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$t_{HCLK} - 1$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	ns

Synchronous waveforms and timings

Figure 28 through *Figure 31* represent synchronous waveforms and *Table 36* through *Table 38* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 28. Synchronous multiplexed NOR/PSRAM read timings

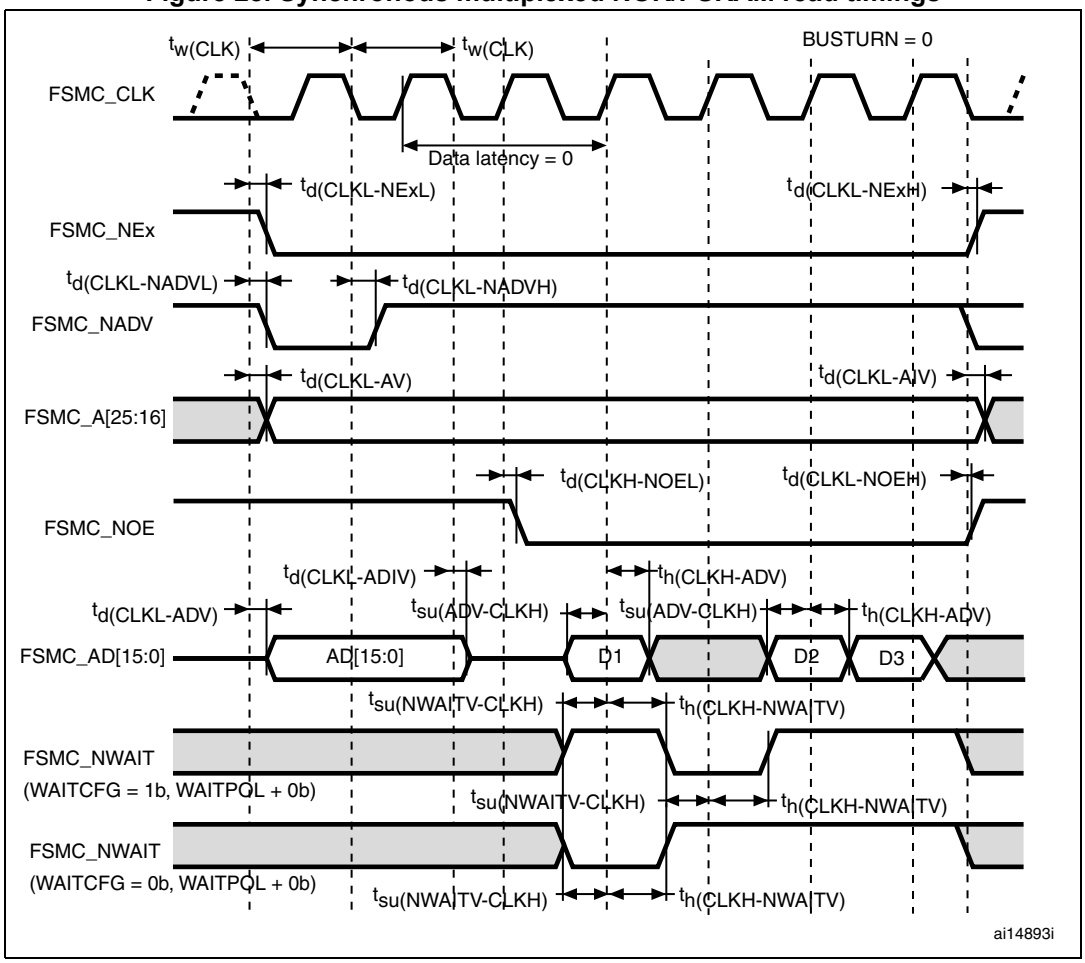
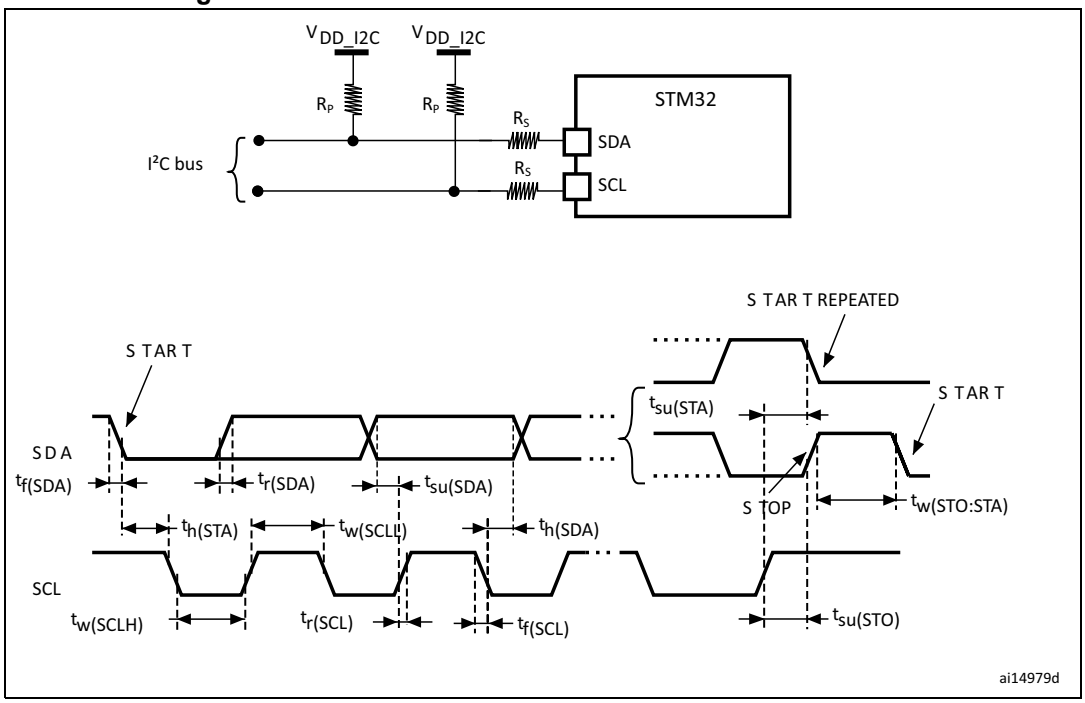


Figure 48. I²C bus AC waveforms and measurement circuit



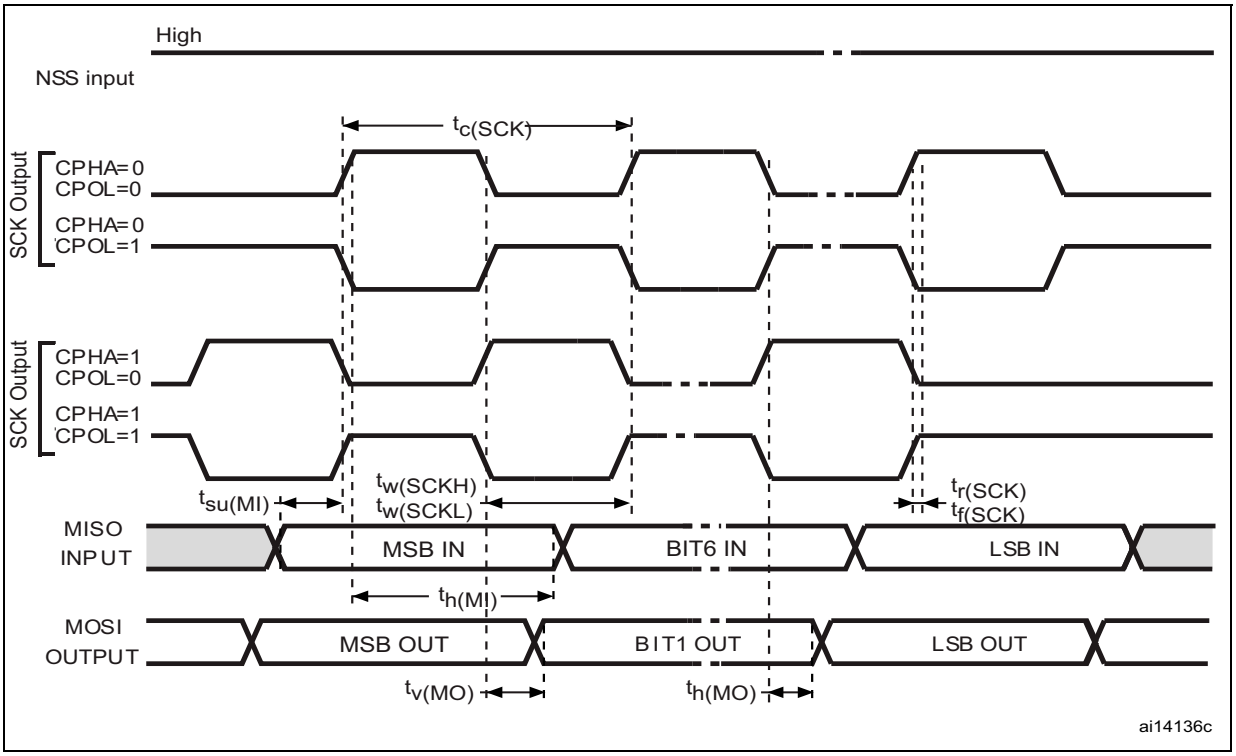
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs: Series protection resistors.
3. Rp: Pull-up resistors.
4. VDD_I2C : I2C bus supply

Table 52. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 51. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 55. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 56. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

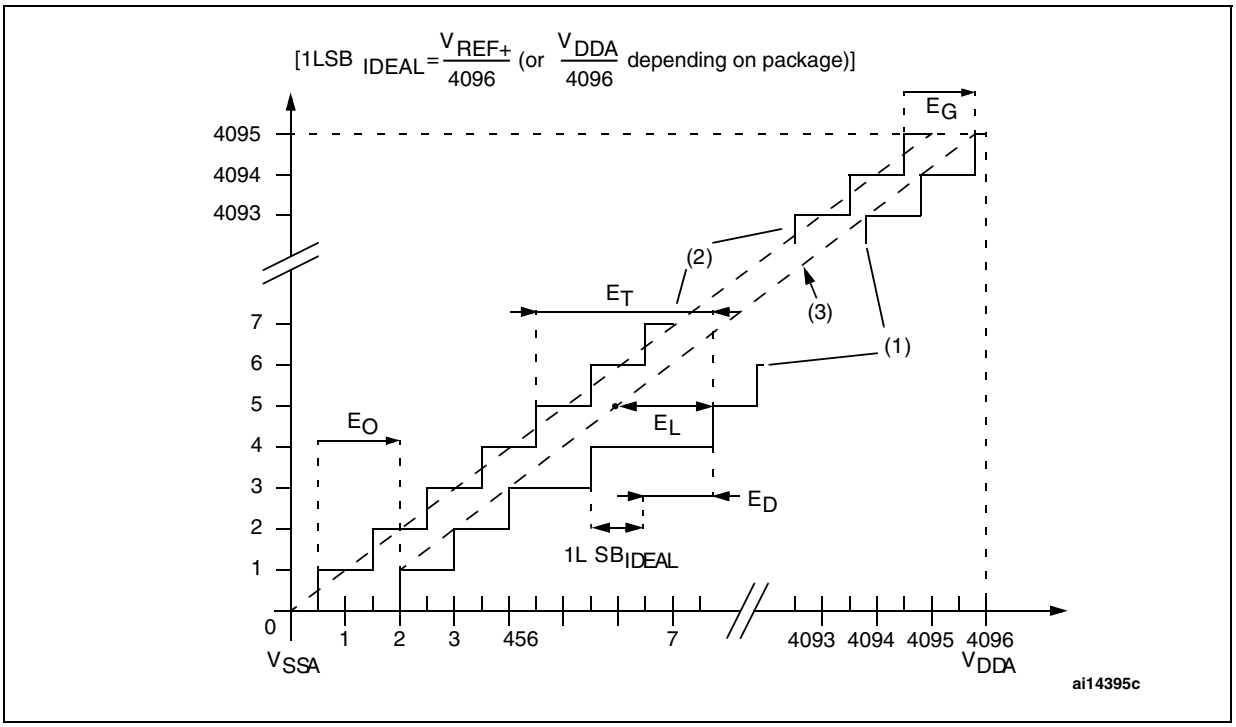
1. Guaranteed by design.

Table 62. ADC accuracy(1) (2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.14* does not affect the ADC accuracy.
4. Guaranteed by characterization results.

Figure 57. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Table 67. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 66. LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprintoutline

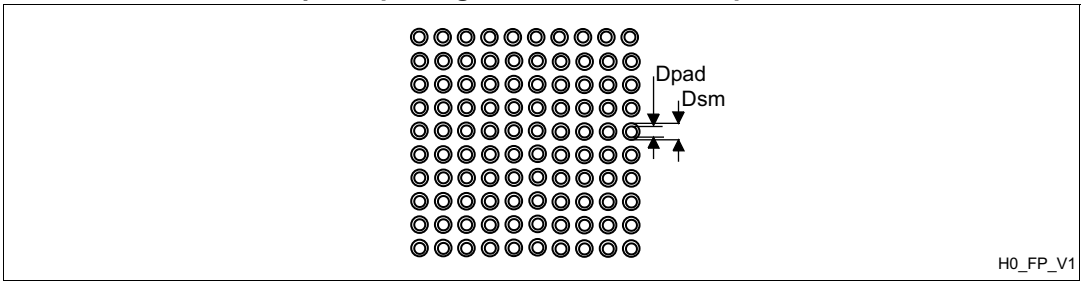


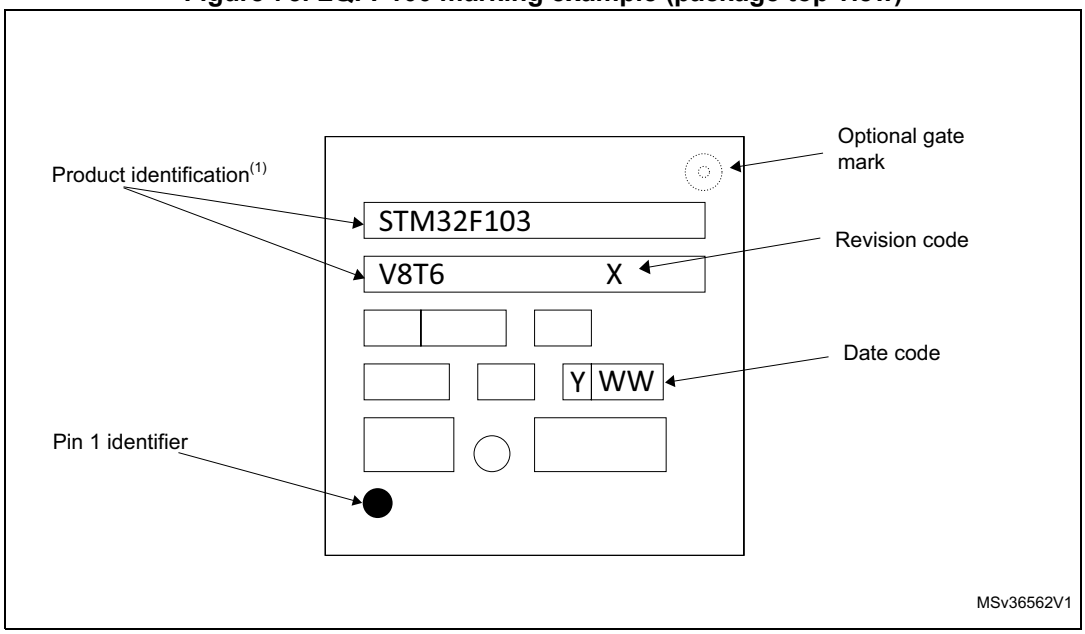
Table 68. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 75. LQFP100 marking example (package top view)

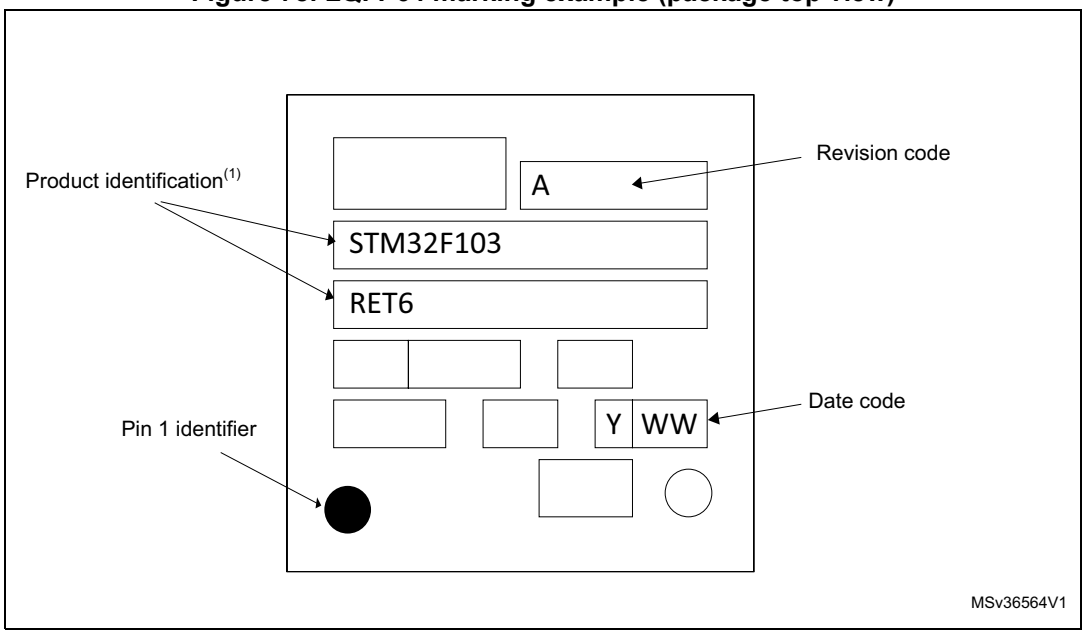


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP64 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 78. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Using the values obtained in *Table 74* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 75: Ordering information scheme*).

Figure 79. LQFP100 P_D max vs. T_A

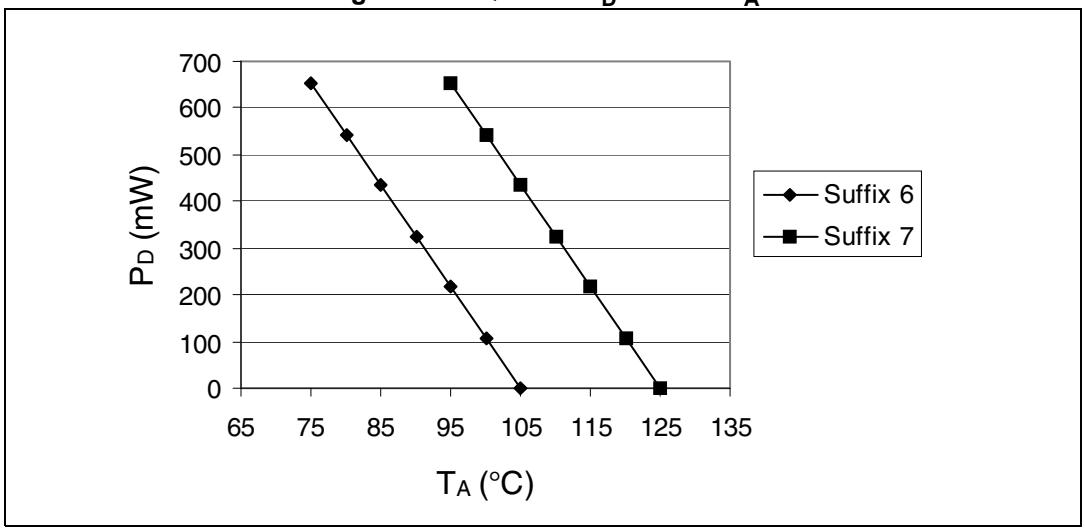


Table 76.Document revision history

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified *on page 1*. *Figure 4: STM32F103xC and STM32F103xE performance line BGA100 ballout* corrected. I/O information clarified *on page 1*. In *Table 5: High-density STM32F103xx pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column PG14 pin description modified in *Table 6: FSMC pin definition*. *Figure 9: Memory map on page 54* modified. Note modified in *Table 18: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 20: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 17*, *Figure 18* and *Figure 19* show typical curves (titles changed). *Table 25: High-speed external user clock characteristics* and *Table 26: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 29: HSI oscillator characteristics*. FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 24: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 25: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 35: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 39: Asynchronous multiplexed PSRAM/NOR write timings*. $t_{h(Data\_NWE)}$ modified in *Table 36: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings* In *Table 41: Synchronous multiplexed PSRAM write timings* and *Table 43: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 28: Synchronous multiplexed NOR/PSRAM read timings*, *Figure 29: Synchronous multiplexed PSRAM write timings* and *Figure 31: Synchronous non-multiplexed PSRAM write timings* modified. *Figure 52: I2S slave timing diagram (Philips protocol)(1)* and *Figure 53: I2S master timing diagram (Philips protocol)(1)* modified. WLCSP64 package added (see *Figure 8: STM32F103xC and STM32F103xE performance line WLCSP64 ballout, ball side*, *Table 8: High-density STM32F103xx pin definitions*, *Figure 65: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline* and *Table 76: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data*). Small text changes.

Table 76.Document revision history

Date	Revision	Changes
31-08-2015	11	Replaced USBDP and USBDM by USB_DP and USB_DM in the whole document. Updated: – Introduction – Reference standard in *Table 43: ESD absolute maximum ratings*. – Updated I_{DDA} description in *Table 63: DAC characteristics*. – *Section : I2C interface characteristics* – *Figure 62: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline* – Updated sentence before *Figure 78: LQFP64 marking example (package top view)*. – *Figure 65: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline* and sentence before *Figure 75: LQFP100 marking example (package top view)* – *Figure 68: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package outline* – *Figure 48: I2C bus AC waveforms and measurement circuit on page 98* – *Section 6.1: LFBGA144 package information* and *Section 6.2: LFBGA100 package information*. – *Table 20: Peripheral current consumption* Added: – *Figure 63: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint* – *Figure 64: LFBGA144 marking example (package top view)* – *Figure 66: LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprintoutline* – *Figure 69: WLCSP64 - 64-ball, 4.4757 x 4.4049 mm, 0.5 mm pitch wafer level chip scale package recommended footprint* – *Table 66: LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)* – *Table 68: LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)* – *Table 70: WLCSP64 recommended PCB design rules (0.5 mm pitch)*.
26-Nov-2015	12	Updated: – *Table 59: ADC characteristics* – *Table 65: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data* – *Table 66: LFBGA144 recommended PCB design rules (0.8 mm pitch BGA)* Added: – *Note 3* on *Table 7: Voltage characteristics*