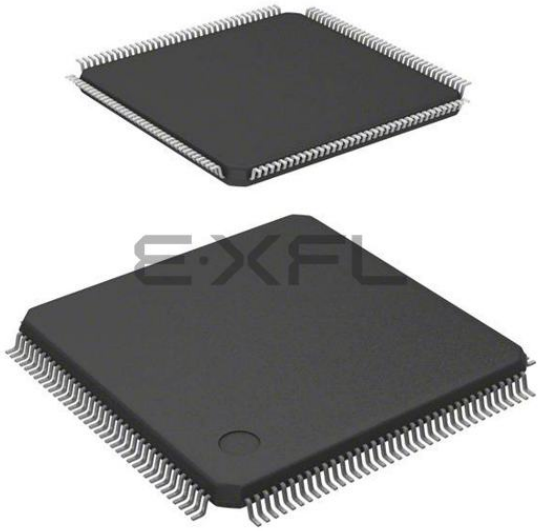

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zet7

2.2 Full compatibility throughout the family

The STM32F103xC/D/E is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices and the STM32F103xC, STM32F103xD and STM32F103xE are referred to as high-density devices.

Low-density and high-density devices are an extension of the STM32F103x8/B medium-density devices, they are specified in the STM32F103x4/6 and STM32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I^2S and DAC while remaining fully compatible with the other members of the family.

The STM32F103x4, STM32F103x6, STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for the STM32F103x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F103xx family

<table>
<tr><th rowspan="3">Pinout</th><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>6 KB RAM</th><th>10 KB RAM</th><th>20 KB RAM</th><th>20 KB RAM</th><th>48 RAM</th><th>64 KB RAM</th><th>64 KB RAM</th></tr>
<tr><td>144</td><td colspan="2" rowspan="2"></td><td colspan="2" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs, USB, CAN, 1 × PWM timer
2 × ADCs</td><td colspan="3" rowspan="2">5 × USARTs
4 × 16-bit timers, 2 × basic timers
3 × SPIs, 2 × I2Ss, 2 × I2Cs
USB, CAN, 2 × PWM timers
3 × ADCs, 2 × DACs, 1 × SDIO
FSMC (100- and 144-pin packages(2))</td></tr>
<tr><td>100</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I2C, USB, CAN, 1 × PWM timer
2 × ADCs</td><td colspan="2" rowspan="2"></td><td colspan="3" rowspan="2"></td></tr>
<tr><td>48</td></tr>
<tr><td>36</td><td colspan="2"></td><td colspan="3"></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.
2. Ports F and G are not available in devices delivered in 100-pin packages.

2.3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

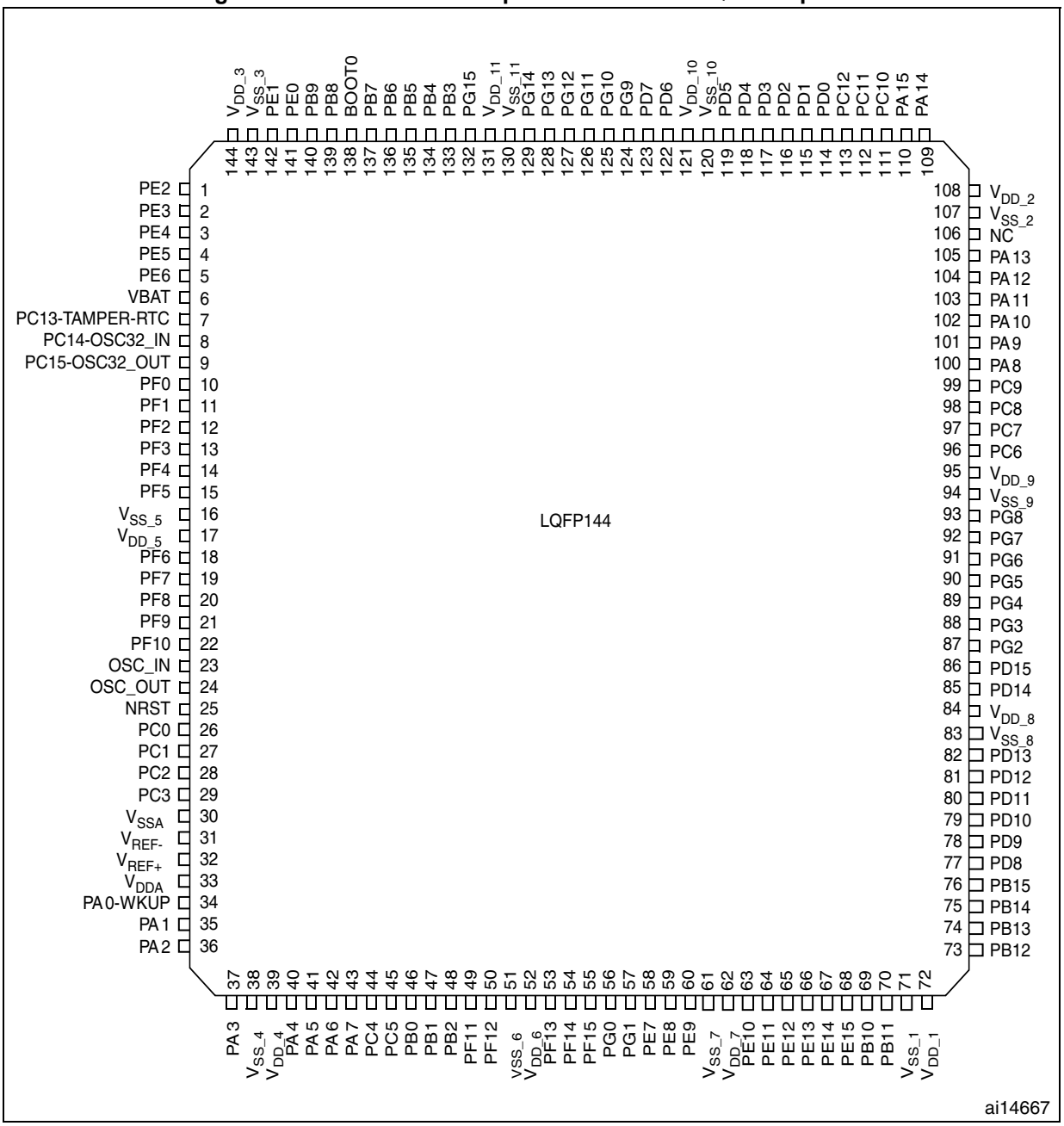
2.3.29 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.30 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 5. STM32F103xC/D/E performance line LQFP144 pinout



1. The above figure shows the package top view.

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
M11	K8	G2	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK[9]/ TIM1_BKIN[9]	-
M12	J8	G1	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS[9]/ TIM1_CH1N	-
L11	H8	F2	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS[9]/	-
L12	G8	F1	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N[9]/	-
L9	K9	-	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	J9	-	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	H9	-	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	G9	-	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	K10	-	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	J10	-	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	-	-	83	V_{SS_8}	S	-	V_{SS_8}	-	-
F8	-	-	-	-	84	V_{DD_8}	S	-	V_{DD_8}	-	-
K11	H10	-	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	G10	-	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	-	-	87	PG2	I/O	FT	PG2	FSMC_A12	-
J11	-	-	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	-
J10	-	-	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	-
H12	-	-	-	-	90	PG5	I/O	FT	PG5	FSMC_A15	-
H11	-	-	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	-
H10	-	-	-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	-
G11	-	-	-	-	93	PG8	I/O	FT	PG8	-	-
G10	-	-	-	-	94	V_{SS_9}	S	-	V_{SS_9}	-	-
F10	-	-	-	-	95	V_{DD_9}	S	-	V_{DD_9}	-	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
C9	D7	-	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	B6	-	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	-	-	120	V_{SS_10}	S	-	V_{SS_10}	-	-
F7	-	-	-	-	121	V_{DD_10}	S	-	V_{DD_10}	-	-
A8	C6	-	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
A9	D6	-	-	88	123	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK
E8	-	-	-	-	124	PG9	I/O	FT	PG9	FSMC_NE2/FSMC_NCE3	-
D8	-	-	-	-	125	PG10	I/O	FT	PG10	FSMC_NCE4_1/ FSMC_NE3	-
C8	-	-	-	-	126	PG11	I/O	FT	PG11	FSMC_NCE4_2	-
B8	-	-	-	-	127	PG12	I/O	FT	PG12	FSMC_NE4	-
D7	-	-	-	-	128	PG13	I/O	FT	PG13	FSMC_A24	-
C7	-	-	-	-	129	PG14	I/O	FT	PG14	FSMC_A25	-
E6	-	-	-	-	130	V_{SS_11}	S	-	V_{SS_11}	-	-
F6	-	-	-	-	131	V_{DD_11}	S	-	V_{DD_11}	-	-
B7	-	-	-	-	132	PG15	I/O	FT	PG15	-	-
A7	A7	A4	55	89	133	PB3	I/O	FT	JTDO	SPI3_SCK / I2S3_CK/	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
A6	A6	B4	56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
B6	C5	A5	57	91	135	PB5	I/O	-	PB5	I2C1_SMBA/ SPI3_MOSI I2S3_SD	TIM3_CH2 / SPI1_MOSI
C6	B5	B5	58	92	136	PB6	I/O	FT	PB6	I2C1_SCL(9)/ TIM4_CH1(9)	USART1_TX
D6	A5	C5	59	93	137	PB7	I/O	FT	PB7	I2C1_SDA(9) / FSMC_NADV / TIM4_CH2(9)	USART1_RX
D5	D5	A6	60	94	138	BOOT0	I	-	BOOT0	-	-
C5	B4	D5	61	95	139	PB8	I/O	FT	PB8	TIM4_CH3(9)/SDIO_D4	I2C1_SCL/ CAN_RX
B5	A4	B6	62	96	140	PB9	I/O	FT	PB9	TIM4_CH4(9)/SDIO_D5	I2C1_SDA / CAN_TX

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 8: Current characteristics* for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 8. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note 3 below *Table 62 on page 109*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

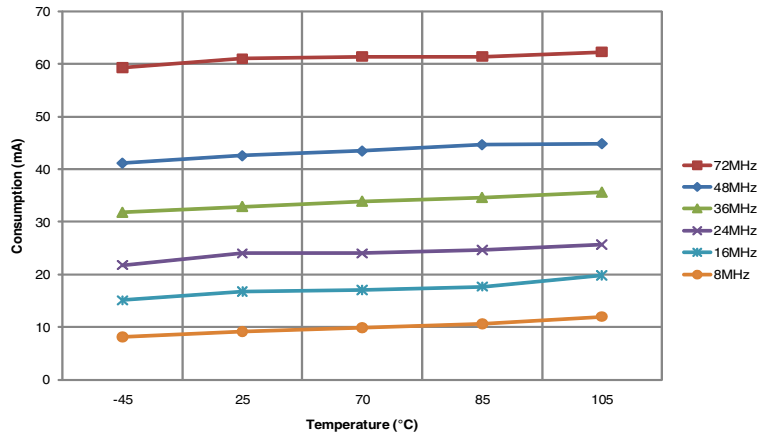


Figure 15. Typical current consumption in Run mode versus frequency (at 3.6 V)- code with data processing running from RAM, peripherals disabled

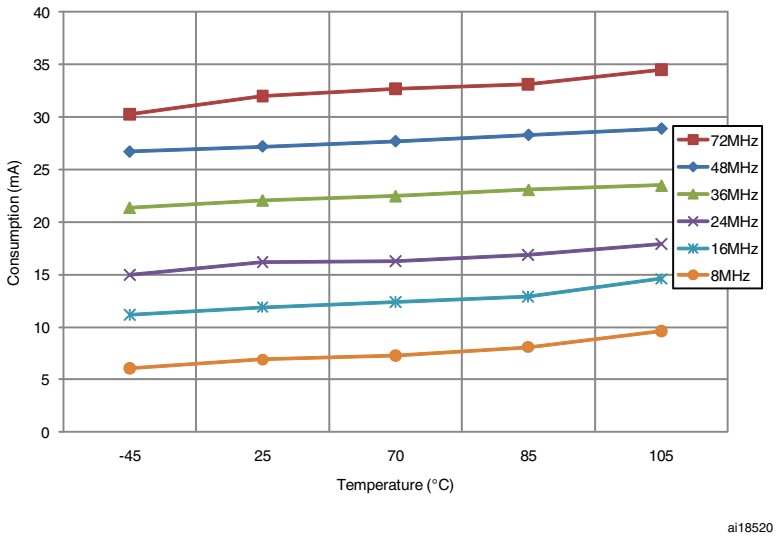


Figure 20. High-speed external clock source AC timing diagram

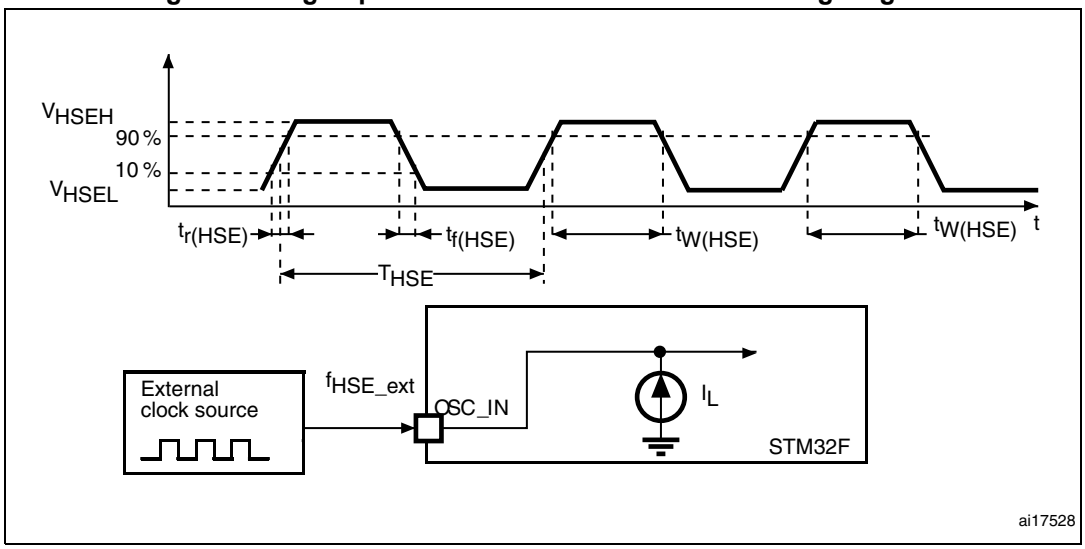


Figure 21. Low-speed external clock source AC timing diagram

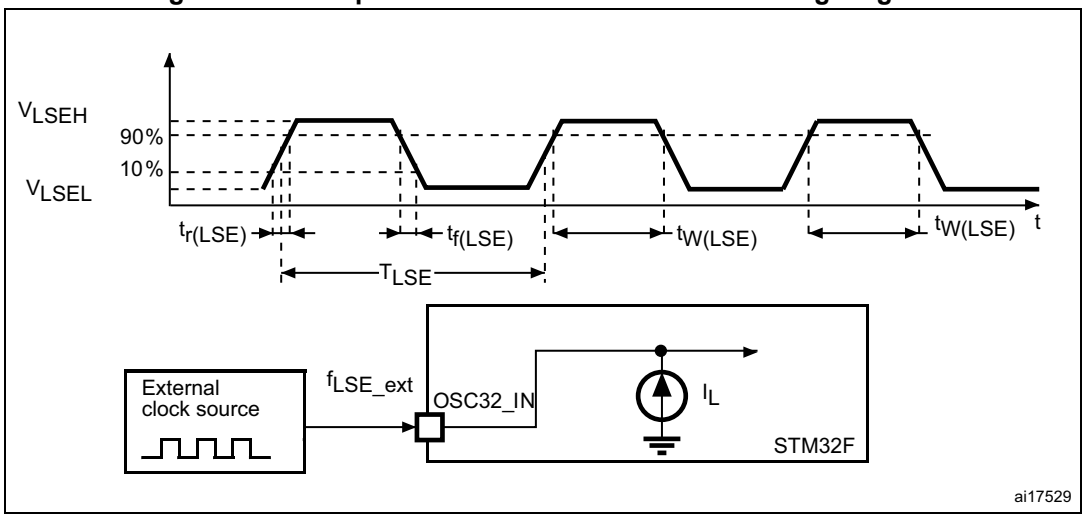
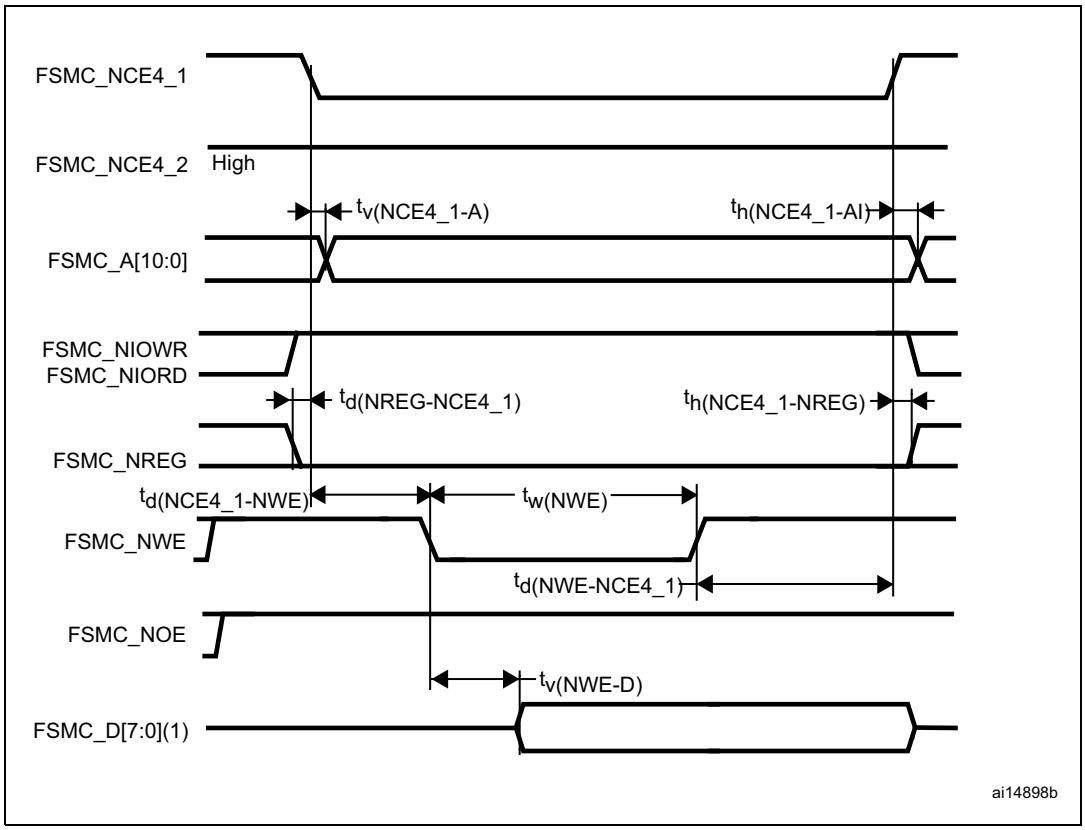


Figure 35. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 36. PC Card/CompactFlash controller waveforms for I/O space read access

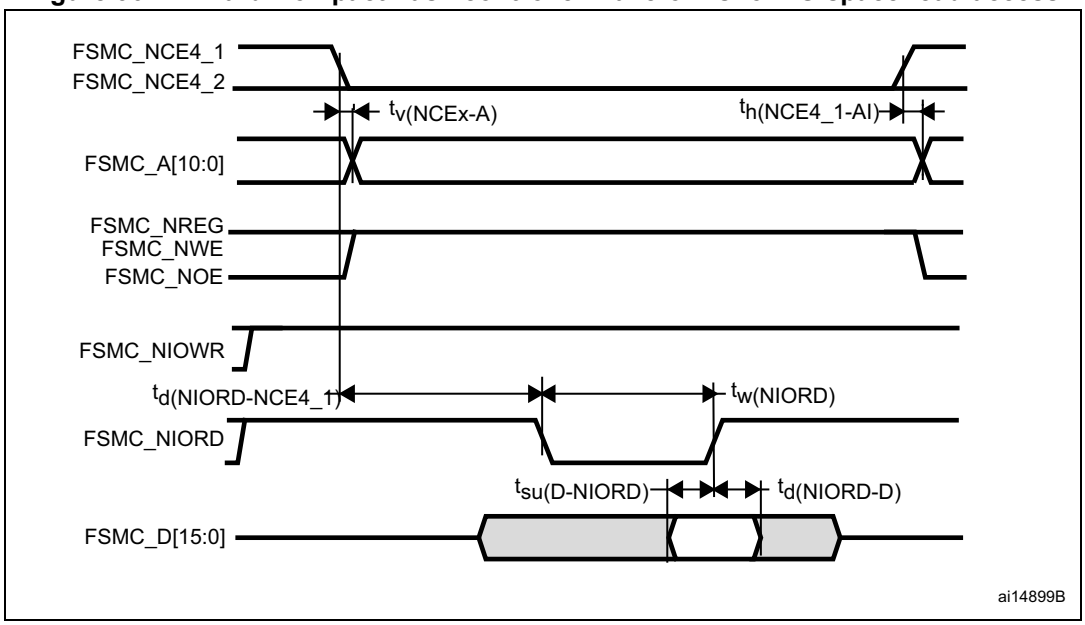


Table 39. Switching characteristics for PC Card/CF read and write cycles(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8t_{HCLK}$ + 3	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5t_{HCLK}$ +1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5t_{HCLK}$+3ns	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5t_{HCLK}$ – 5	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	$5t_{HCLK}$ + 2.5	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5t_{HCLK}$ – 5	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8t_{HCLK}$ + 2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Table 47. Output voltage characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 46* and *Table 48*, respectively.

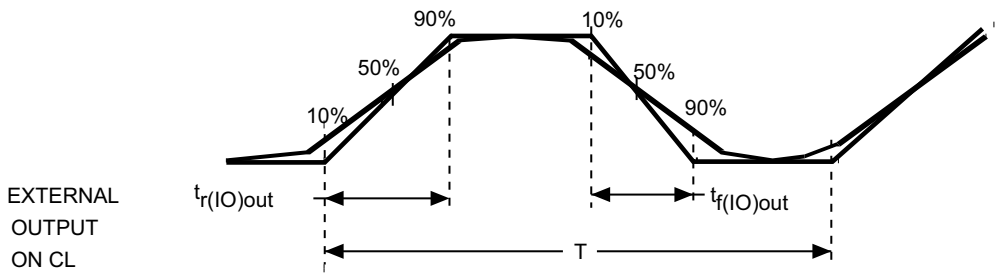
Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 46*.
3. Guaranteed by design.

Figure 46. I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 46*).

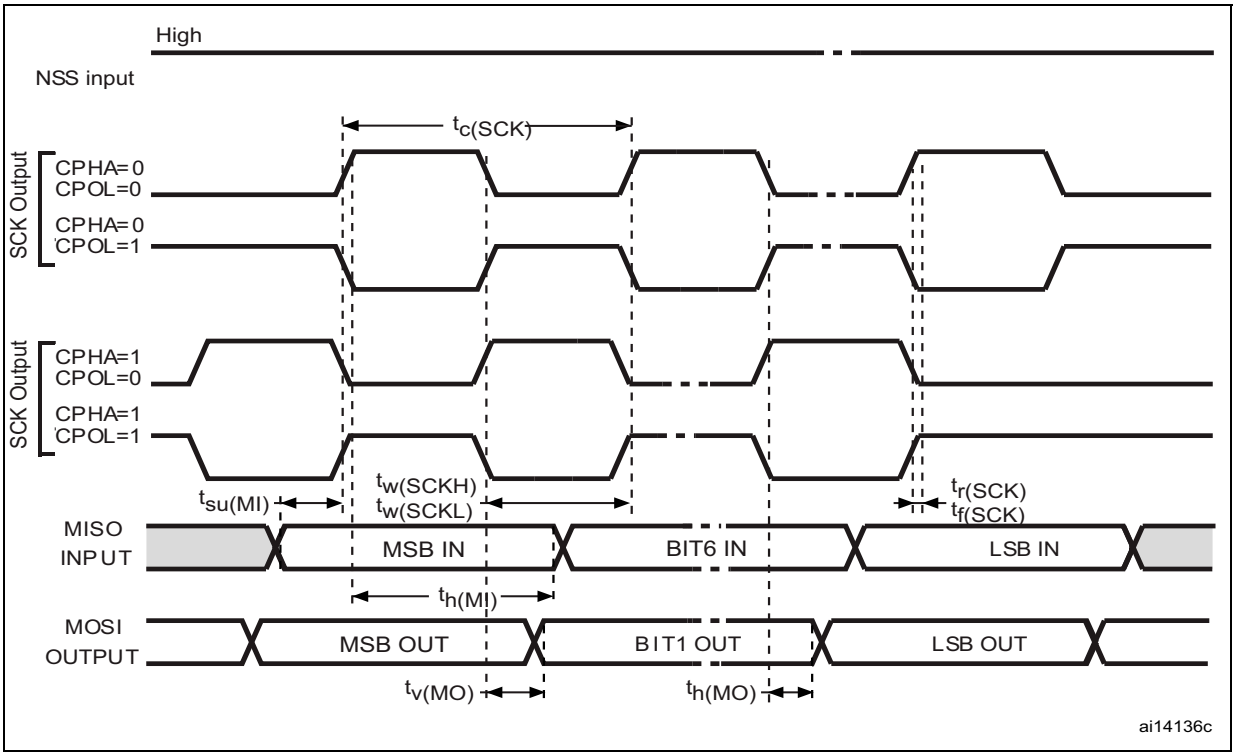
Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 49. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 51. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 54. SDIO high-speed mode

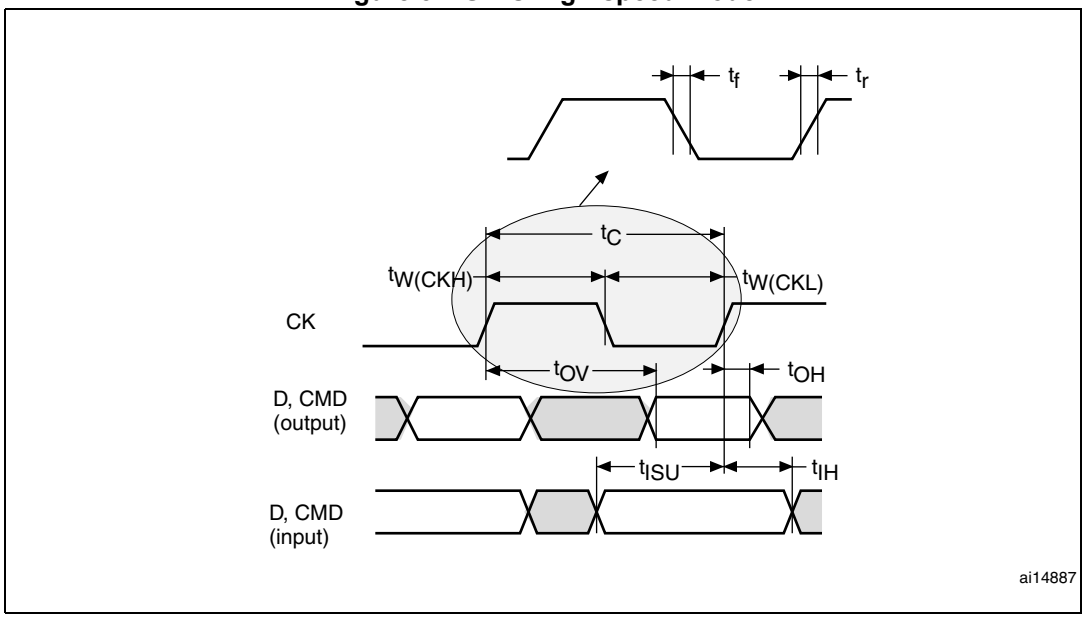


Figure 55. SD default mode

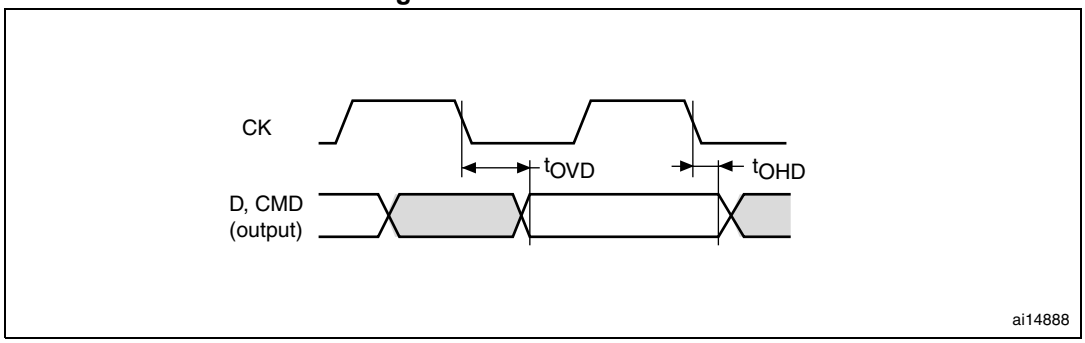
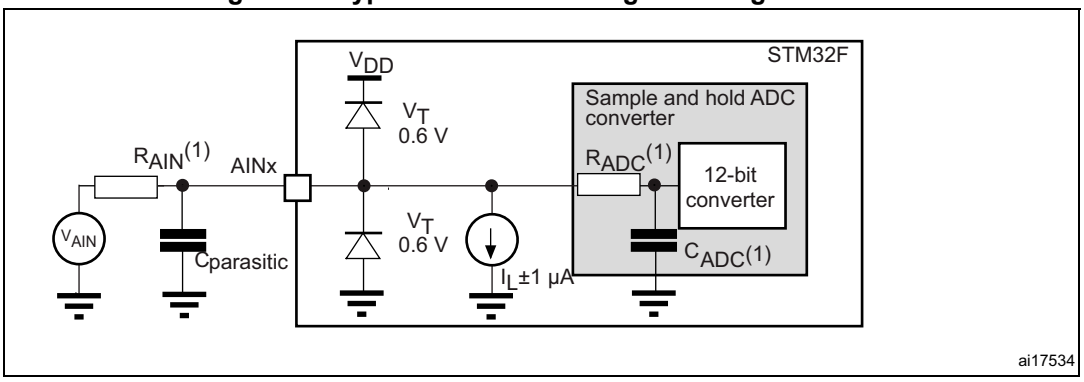


Table 55. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq 30$ pF	0	48	MHz
tW(CKL)	Clock low time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	32	-	ns
tW(CKH)	Clock high time, f_{PP} = 16 MHz	$C_L \leq 30$ pF	30	-	
t_r	Clock rise time	$C_L \leq 30$ pF	-	4	
t_f	Clock fall time	$C_L \leq 30$ pF	-	5	

Figure 58. Typical connection diagram using the ADC

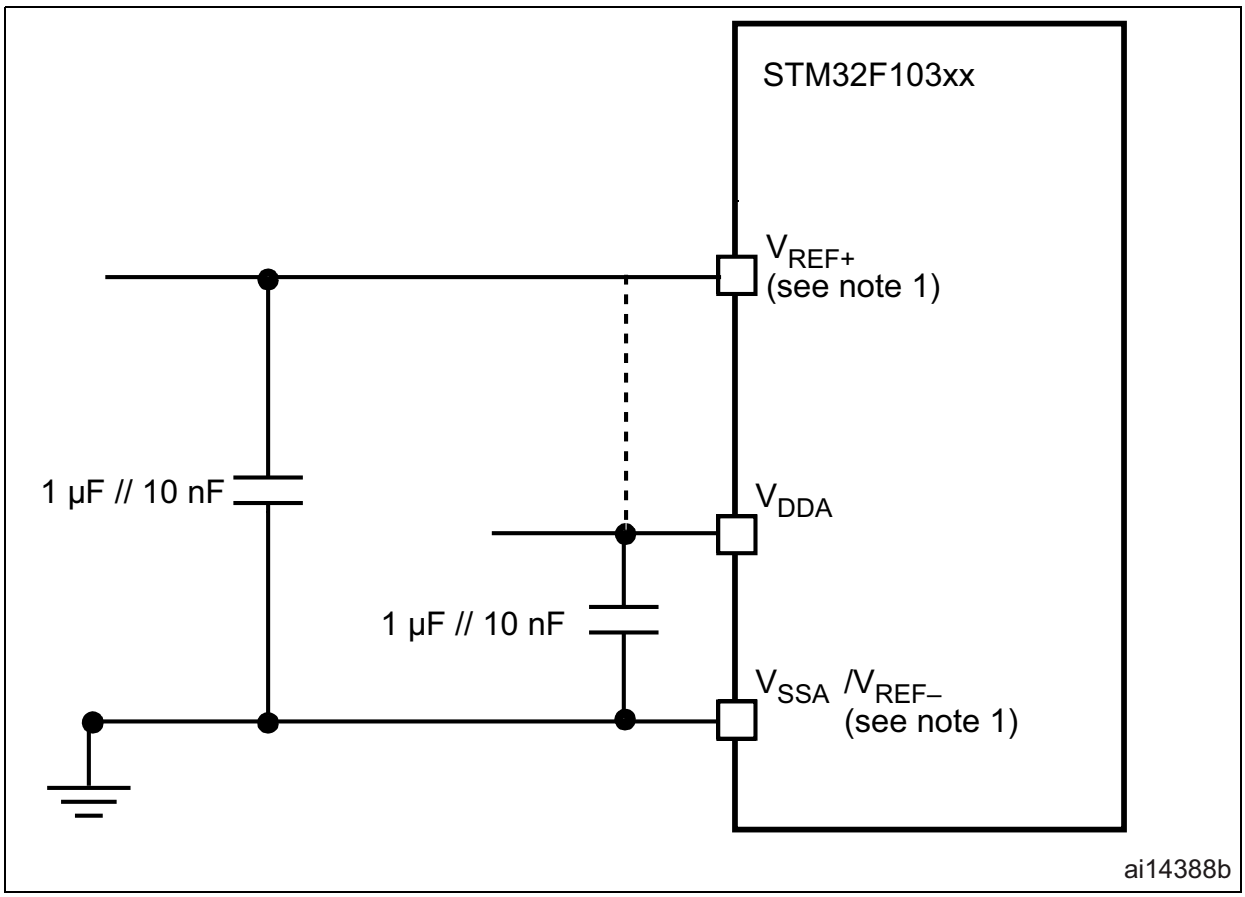


1. Refer to *Table 59* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 59* or *Figure 60*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 59. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.21 Temperature sensor characteristics

Table 64. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 76.Document revision history

Date	Revision	Changes
21-Jul-2009	6	*Figure 1: STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram* updated. *Note 5* updated and *Note 4* added in *Table 5: High-density STM32F103xC/D/E pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 13: Embedded internal reference voltage*. *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM* modified. f_{HSE_ext} min modified in *Table 21: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 23: HSE 4-16 MHz oscillator characteristics* and *Table 24: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 29: Synchronous multiplexed PSRAM write timings*. *Table 25: HSI oscillator characteristics* modified. Conditions removed from *Table 27: Low-power mode wakeup timings*. Jitter added to *Table 28: PLL characteristics*. *Figure 47: Recommended NRST pin protection* modified. In *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings*: $t_{h(BL\_NOE)}$ and $t_{h(A\_NOE)}$ modified. In *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*: $t_{h(A\_NWE)}$ and $t_{h(Data\_NWE)}$ modified. In *Table 33: Asynchronous multiplexed PSRAM/NOR read timings*: $t_{h(AD\_NADV)}$ and $t_{h(A\_NOE)}$ modified. In *Table 34: Asynchronous multiplexed PSRAM/NOR write timings*: $t_{h(A\_NWE)}$ modified. In *Table 35: Synchronous multiplexed NOR/PSRAM read timings*: $t_{h(CLKH-NWAITV)}$ modified. In *Table 40: Switching characteristics for NAND Flash read and write cycles*: $t_{h(NOE-D)}$ modified. *Table 53: SPI characteristics* modified. Values added to *Table 54: I2S characteristics* and *Table 55: SD / MMC characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 59: ADC characteristics*. R_{AIN} max values modified in *Table 60: RAIN max for fADC = 14 MHz*. *Table 71: DAC characteristics* modified. *Figure 61: 12-bit buffered /non-buffered DAC* added. *Figure 63: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline* and *Table 75: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package mechanical data* updated.
24-Sep-2009	7	Number of DACs corrected in *Table 3: STM32F103xx family*. I_{DD_VBAT} updated in *Table 17: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 16: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* added. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.11: EMC characteristics on page 87*. *Table 63: DAC characteristics* modified. Small text changes.

Table 76.Document revision history

Date	Revision	Changes
19-Apr-2011	8	Updated package choice for 103Rx in *Table 2* Updated footnotes below *Table 7: Voltage characteristics on page 43* and *Table 8: Current characteristics on page 43* Updated tw min in *Table 21: High-speed external user clock characteristics on page 58* Updated startup time in *Table 24: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 61* Updated note 2 in *Table 51: I2C characteristics on page 97* Updated *Figure 48: I2C bus AC waveforms and measurement circuit* Updated *Figure 47: Recommended NRST pin protection* Updated *Section 5.3.14: I/O port characteristics* Updated *Table 35: Synchronous multiplexed NOR/PSRAM read timings on page 73* Updated FSMC *Figure 26* thru *Figure 31* Updated *Figure 41.: NAND controller waveforms for common memory write access* and *Figure 48.: I2C bus AC waveforms and measurement circuit* Added *Section 5.3.13: I/O current injection characteristics* Updated *Figure 67* and added *Table 69: WLCSP, 64-ball 4.466 × 4.395 mm, 0.500 mm pitch, wafer-level chip-scale package mechanical data on page 121* LQFP64 package mechanical data updated: see *Figure 73.: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 73: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data on page 130*.
30-Sept-2014	9	Added *Note 7* in *Table 5: High-density STM32F103xC/D/E pin definitions on page 31*. Updated *Note 10* in *Table 5: High-density STM32F103xC/D/E pin definitions on page 31*. Modified *Note 2* in *Table 62: ADC accuracy on page 109* Modified *Note 3* in *Table 62: ADC accuracy on page 109* Modified notes in *Table 51: I2C characteristics on page 97* Updated *Figure 51: SPI timing diagram - master mode(1) on page 101*
23-Feb-2015	10	Updated *Figure 66.: BGA pad footprint*, *Figure 70: LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline*, *Figure 73.: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 74.: LQFP100 recommended footprint*, *Figure 76.: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 77.: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* Added *Figure 72.: LQFP144 marking example (package top view)*, *Figure 75.: LQFP100 marking example (package top view)*, *Figure 78.: LQFP64 marking example (package top view)* Updated *Table 72: LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*