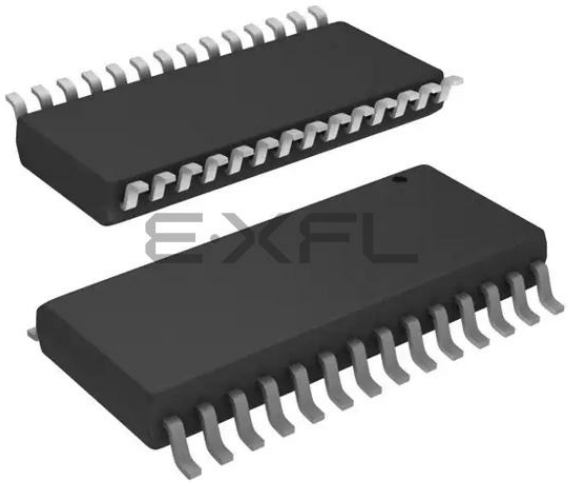

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 12x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs202-e-so |

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## 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXGS202 Digital Signal Controller (DSC) devices.

The dsPIC33EPXXGS202 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: dsPIC33EPXXGS202 FAMILY BLOCK DIAGRAM**

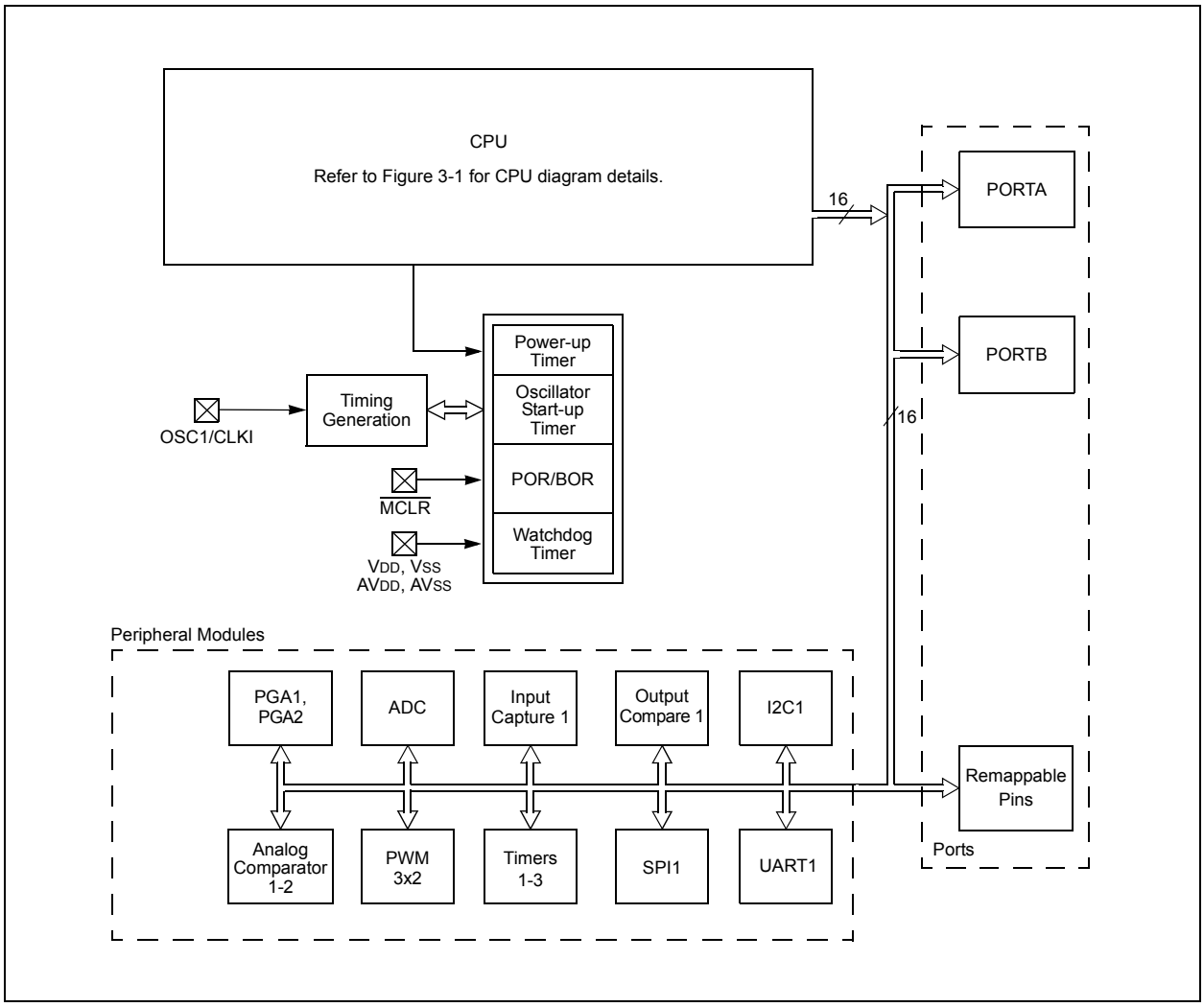

**TABLE 4-9: PWM GENERATOR 2 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON2 | 0C40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC1 | DTC0 | — | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON2 | 0C42 | PENH | PENL | POLH | POLL | PMOD1 | PMOD0 | OVRENH | OVRENL | OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | C000 |
| FCLCON2 | 0C44 | IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMOD0 | 00F8 |
| PDC2 | 0C46 | PWM Generator 2 Duty Cycle Register (PDC2<15:0>) | | | | | | | | | | | | | | | | 0000 |
| PHASE2 | 0C48 | PWM Phase-Shift Value or Independent Time Base Period for the PWM Generator 2 Register (PHASE2<15:0>) | | | | | | | | | | | | | | | | 0000 |
| DTR2 | 0C4A | — | — | DTR2<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR2 | 0C4C | — | — | ALTDTR2<13:0> | | | | | | | | | | | | | | 0000 |
| SDC2 | 0C4E | SDC2<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE2 | 0C50 | SPHASE2<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG2 | 0C52 | TRGCMP<12:0> | | | | | | | | | | | | | — | — | — | 0000 |
| TRGCON2 | 0C54 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — | DTM | — | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 | 0000 |
| STRIG2 | 0C56 | STRGCMP<12:0> | | | | | | | | | | | | | — | — | — | 0000 |
| PWMCAP2 | 0C58 | PWMCAP<12:0> | | | | | | | | | | | | | — | — | — | 0000 |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY2 | 0C5C | — | — | — | — | LEB<8:0> | | | | | | | | | — | — | — | 0000 |
| AUXCON2 | 0C5E | HRPDIS | HRDDIS | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 | — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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## 4.6 Instruction Addressing Modes

The addressing modes shown in Table 4-25 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

### 4.6.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

### 4.6.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

**Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

**TABLE 4-25: FUNDAMENTAL ADDRESSING MODES SUPPORTED**

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn form the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |

### 4.7.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

| | |
|---|---|
| **Note:** | The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged. |

## 4.8 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

### 4.8.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all of these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

| | |
|---|---|
| **Note:** | All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses. |

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

| | |
|---|---|
| **Note:** | Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled. |

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.


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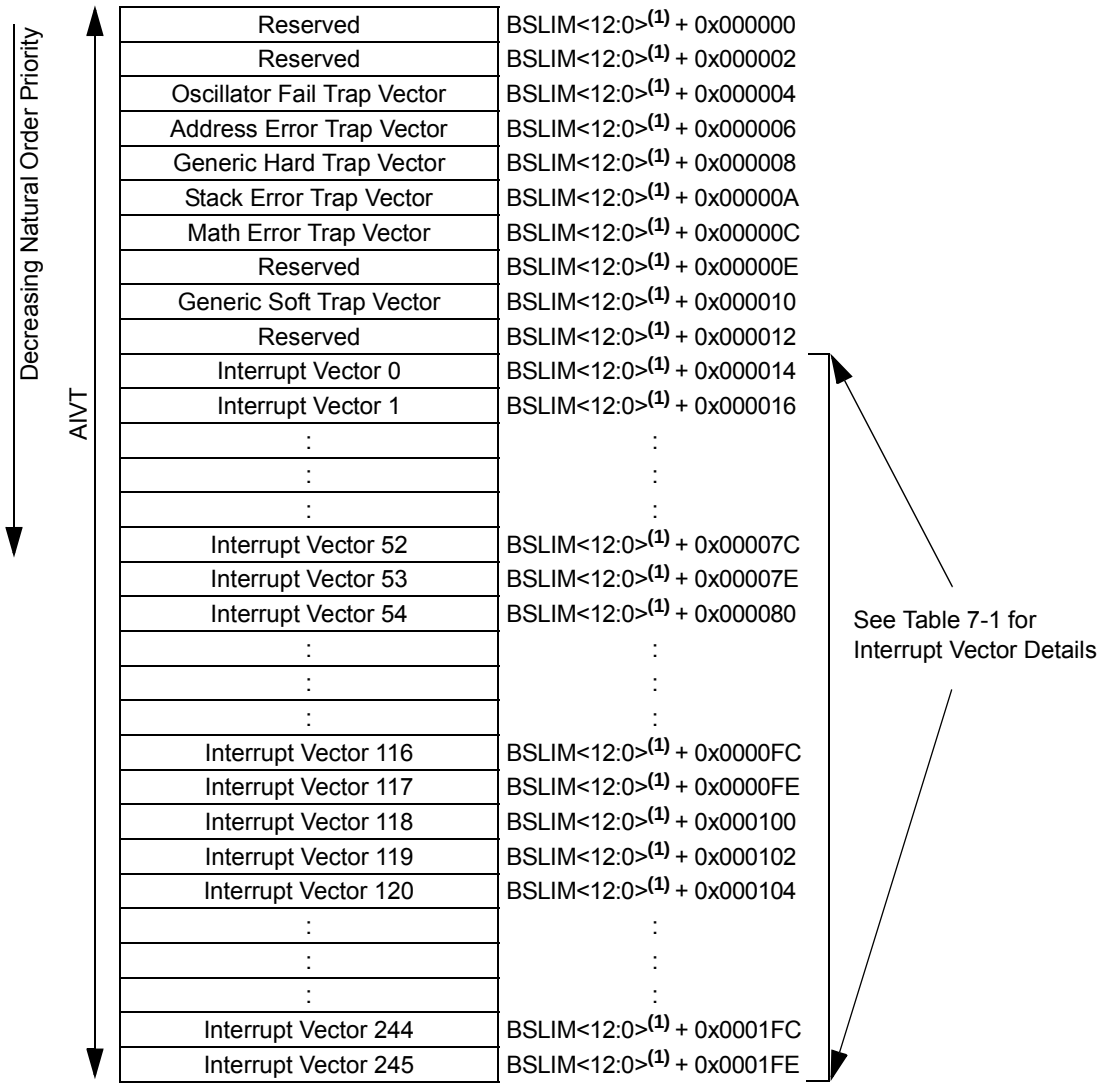
**FIGURE 7-2: dsPIC33EPXXGS202 FAMILY ALTERNATE INTERRUPT VECTOR TABLE**




**Note 1:** The address depends on the size of the Boot Segment defined by BSLIM<12:0>. [(BSLIM<12:0> – 1) x 0x400] + Offset.

## 9.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com)

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXGS202 family devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

### 9.1 Clock Frequency and Clock Switching

The dsPIC33EPXXGS202 family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 "Oscillator Configuration"**.

### 9.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXGS202 family devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 9-1.

**Note:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

**EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX**

```
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
```

## 10.7 Peripheral Pin Select Registers

**REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INT1R<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **INT1R<7:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as ‘0’

**REGISTER 10-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INT2R<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **INT2R<7:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits
10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

**REGISTER 15-3: PTPER: PWM PRIMARY MASTER TIME BASE PERIOD REGISTER(1,2)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| PTPER<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTPER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

**Note 1:** The PWM time base has a minimum value of 0x0010 and a maximum value of 0xFFF8.

**2:** Any period value that is less than 0x0028 must have the Least Significant 3 bits set to '0', thus yielding a period resolution at 8.32 ns (at fastest auxiliary clock rate).

**REGISTER 15-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP<12:5> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP<4:0> | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-3 **SEVTCMP<12:0>:** Special Event Compare Count Value bits

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** One LSB = 1.04 ns (at fastest auxiliary clock rate); therefore, the minimum SEVTCMP resolution is 8.32 ns.

**REGISTER 15-19: TRGCONx: PWMx TRIGGER CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTM(1) | — | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **TRGDIV<3:0>:** Trigger # Output Divider bits
1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **DTM:** Dual Trigger Mode bit(1)
1 = Secondary trigger event is combined with the primary trigger event to create a PWM trigger
0 = Secondary trigger event is not combined with the primary trigger event to create a PWM trigger; two separate PWM triggers are generated

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT<5:0>:** Trigger Postscaler Start Enable Select bits
111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

**Note 1:** The secondary PWMx generator cannot generate PWM trigger interrupts.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## 16.3 SPI Control Registers

**REGISTER 16-1: SPI1STAT: SPI1 STATUS AND CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SPIEN | — | SPISIDL | — | — | SPIBEC2 | SPIBEC1 | SPIBEC0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/C-0, HS | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0, HS, HC | R-0, HS, HC |
|---|---|---|---|---|---|---|---|
| SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISEL0 | SPITBF | SPIRBF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HS = Hardware Settable bit | HC = Hardware Clearable bit |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **SPIEN:** SPI1 Enable bit
1 = Enables the module and configures SCK1, SDO1, SDI1 and $\overline{SS1}$ as serial port pins
0 = Disables the module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPI1 Stop in Idle Mode bit
1 = Discontinues the module operation when device enters Idle mode
0 = Continues the module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **SPIBEC<2:0>:** SPI1 Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPI1 transfers that are pending.
Slave mode:
Number of SPI1 transfers that are unread.

bit 7 **SRMPT:** SPI1 Shift Register (SPI1SR) Empty bit (valid in Enhanced Buffer mode)
1 = SPI1 Shift register is empty and ready to send or receive the data
0 = SPI1 Shift register is not empty

bit 6 **SPIROV:** SPI1 Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPI1BUF register
0 = No overflow has occurred

bit 5 **SRXMPT:** SPI1 Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty

bit 4-2 **SISEL<2:0>:** SPI1 Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPI1 transmit buffer is full (SPITBF bit is set)
110 = Interrupt when last bit is shifted into SPI1SR, and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPI1SR and the transmit is complete
100 = Interrupt when one data is shifted into the SPI1SR, and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPI1 receive buffer is full (SPIRBF bit is set)
010 = Interrupt when the SPI1 receive buffer is 3/4 or more full
001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

**REGISTER 18-2: U1STA: UART1 STATUS AND CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R/W-0 | R-0 | R-1 |
|---|---|---|---|---|---|---|---|
| UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN(1) | UTXBF | TRMT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/C-0 | R-0 |
|---|---|---|---|---|---|---|---|
| URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15,13 **UTXISEL<1:0>:** UART1 Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UART1 Transmit Polarity Inversion bit

If IREN = 0:
- 1 = U1TX Idle state is '0'
- 0 = U1TX Idle state is '1'

If IREN = 1:
- 1 = IrDA® encoded, U1TX Idle state is '1'
- 0 = IrDA encoded, U1TX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UART1 Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UART1 Transmit Enable bit(1)
- 1 = Transmit is enabled, U1TX pin is controlled by UART1
- 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; U1TX pin is controlled by the PORT

bit 9 **UTXBF:** UART1 Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UART1 Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on U1RSR transfer, making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on U1RSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the U1RSR to the receive buffer; receive buffer has one or more characters

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART1 module for transmit operation.

**REGISTER 19-7: ADCON4L: ADC CONTROL REGISTER 4 LOW**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | SYNCTRG1(1) | SYNCTRG0(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | SAMC1EN | SAMC0EN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-8 **SYNCTRG<1:0>** Dedicated ADC Core x Trigger Synchronization bits(1)

1 = All triggers are synchronized with the Core Source Clock (TCORESRC)
0 = The ADC core triggers are not synchronized

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **SAMC1EN:SAMC0EN:** Dedicated ADC Core x Conversion Delay Enable bits

1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCOREXL register
0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle.

**Note 1:** For proper ADC performance, this bit must be set when using level-sensitive triggers and cleared for edge-sensitive triggers.


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## 22.2 Device Calibration and Identification

The PGAx modules on the dsPIC33EPXXGS202 family devices require Calibration Data registers to improve performance of the module over a wide operating range. These Calibration registers are read-only and are stored in configuration memory space. Prior to enabling the module, the calibration data must be read (TBLPAG and Table Read instruction) and loaded into their respective SFR registers. The device calibration addresses are shown in Table 22-3.

The dsPIC33EPXXGS202 devices have two Identification registers near the end of configuration memory space that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the mask, variant and manufacturing information about the device. These registers are read-only and are shown in Register 22-1 and Register 22-2.

**TABLE 22-3: DEVICE CALIBRATION ADDRESSES(1)**

| Calibration Name | Address | Bits 23-16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PGA1CAL | 800E48 | — | — | — | — | — | — | — | — | — | — | — | PGA1 Calibration Data bits | | | | | |
| PGA2CAL | 800E4C | — | — | — | — | — | — | — | — | — | — | — | PGA2 Calibration Data bits | | | | | |

**Note 1:** The calibration data must be copied into its respective registers prior to enabling the module.


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## 24.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 24.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®


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**TABLE 25-25: TIMER2 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TB10 | TtxH | T2CK High Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TB15, N = Prescale Value (1, 8, 64, 256) |
| TB11 | TtxL | T2CK Low Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TB15, N = Prescale Value (1, 8, 64, 256) |
| TB15 | TtxP | T2CK Input Period | Synchronous mode | Greater of: 40 or (2 TCY + 40)/N | — | — | ns | N = Prescale Value (1, 8, 64, 256) |
| TB20 | TCKEXTMRL | Delay from External T2CK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 25-26: TIMER3 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TC10 | TtxH | T3CK High Time | Synchronous | TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC11 | TtxL | T3CK Low Time | Synchronous | TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC15 | TtxP | T3CK Input Period | Synchronous with Prescaler | 2 TCY + 40 | — | — | ns | N = Prescale Value (1, 8, 64, 256) |
| TC20 | TCKEXTMRL | Delay from External T3CK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.


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**TABLE 25-38: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 11 | MHz | **(Note 3)** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid After SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | **(Note 4)** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SS1}$ ↑ After SCK1 Edge | 1.5 TCY + 40 | — | — | ns | **(Note 4)** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

## 26.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 26-1: VOH – 4x DRIVER PINS**

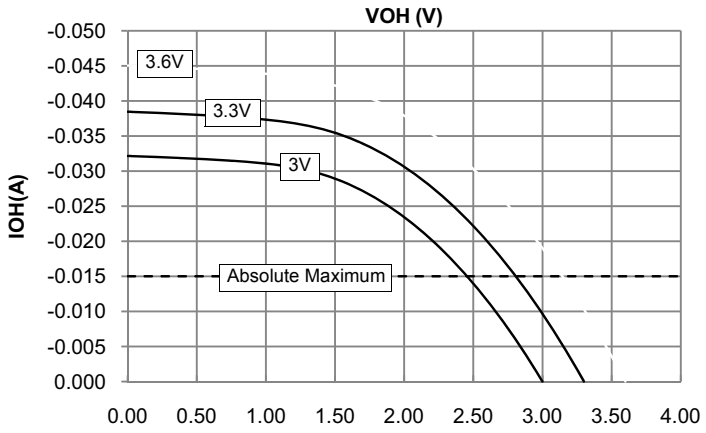



**FIGURE 26-2: VOH – 8x DRIVER PINS**

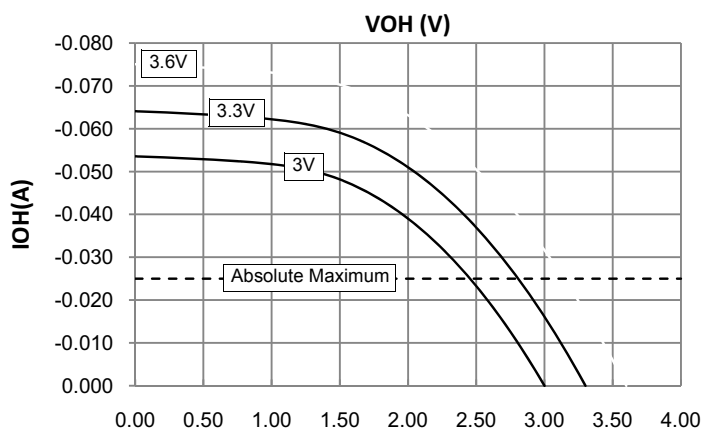



**FIGURE 26-3: VOL – 4x DRIVER PINS**

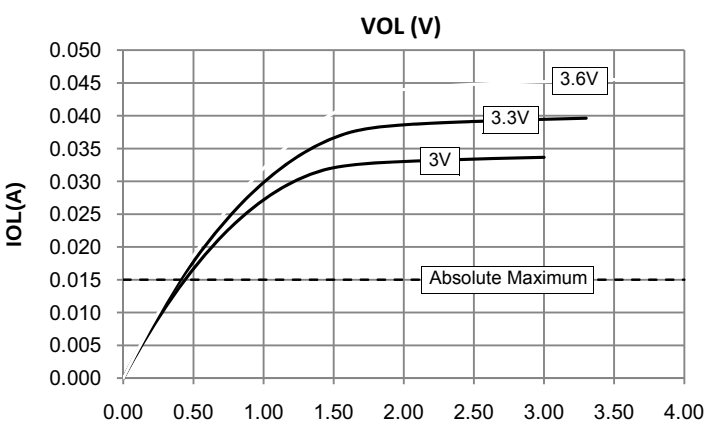
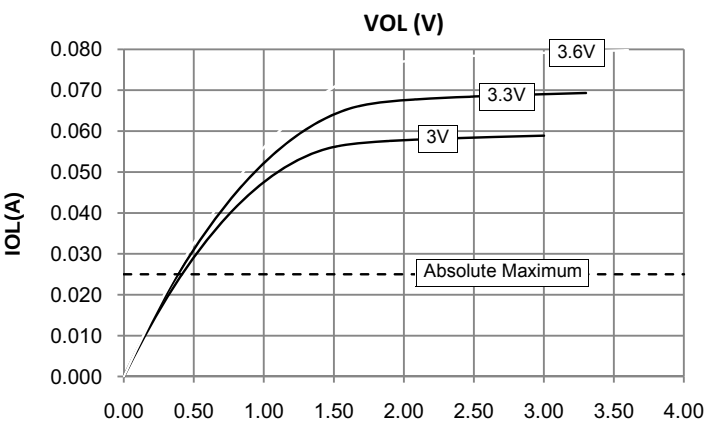



**FIGURE 26-4: VOL – 8x DRIVER PINS**

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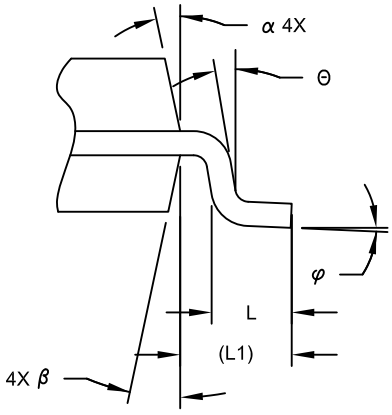
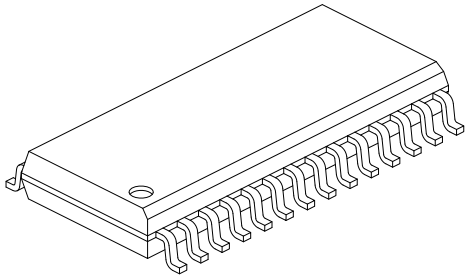
## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




VIEW C



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | | 10.30 BSC | |
| Molded Package Width | E1 | | 7.50 BSC | |
| Overall Length | D | | 17.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.40 REF | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

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