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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs202t-e-m6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name	Pin Type	Buffer Type	PPS	Description
PGA1P1-PGA1P3	I	Analog	No	PGA1 Positive Inputs 1 through 3.
PGA1N2	I	Analog	No	PGA1 Negative Input 2.
PGA2P1-PGA2P3	I	Analog	No	PGA2 Positive Inputs 1 through 3.
PGA2N2	I	Analog	No	PGA2 Negative Input 2.
ADTRG31	I	ST	No	External ADC trigger source.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3 MCLR AVDD	I/O I I/O I I/P P	ST ST ST ST ST ST ST	No No No No No No	Data I/O pin for Programming/Debugging Communication Channel 1. Clock input pin for Programming/Debugging Communication Channel 1. Data I/O pin for Programming/Debugging Communication Channel 2. Clock input pin for Programming/Debugging Communication Channel 2. Data I/O pin for Programming/Debugging Communication Channel 3. Clock input pin for Programming/Debugging Communication Channel 3. Clock input pin for Programming/Debugging Communication Channel 3. Master Clear (Reset) input. This pin is an active-low Reset to the device. Positive supply for analog modules. This pin must be connected at all
AVss	Р	Р	No	times. Ground reference for analog modules. This pin must be connected at all times.
Vdd	Р	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	Р	—	No	CPU logic filter capacitor connection.
Vss	Р	_	No	Ground reference for logic and I/O pins.
Legend: $CMOS = C$	MOS co	omnatible	input	or output Analog = Analog input P = Power

TABLE 1-1. **PINOUT I/O DESCRIPTIONS (CONTINUED)**

egend: CMOS : CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels O = Output PPS = Peripheral Pin Select

Analog = Analog Input TTL = TTL input buffer

```
= Power
I = Input
```

FIGURE 3-1: dsPIC33EPXXGS202 CPU BLOCK DIAGRAM









FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33EP16/32GS202 DEVICES

TABLE 4-20: PROGRAMMABLE GAIN AMPLIFIER REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PGA1CON	0504	PGAEN	_	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	_		-	_	_	GAIN2	GAIN1	GAIN0	0000
PGA1CAL	0506	_	_	_	_	_	_	_	_	_	_			PGACA	L<5:0>			0000
PGA2CON	0508	PGAEN	_	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	_	_	_	_	_	GAIN2	GAIN1	GAIN0	0000
PGA2CAL	050A	_	_	_	_	_	_	_	_	_	_			PGACA	L<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: ANALOG COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMP1CON	0540	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	_	INSEL1	INSEL0	_	HYSPOL	CMPSTAT	ALTINP	CMPPOL	—	0000
CMP1DAC	0542	_	_	_	_						CMREF	<11:0>						0000
CMP2CON	0544	CMPON	_	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL		INSEL1	INSEL0	_	HYSPOL	CMPSTAT	ALTINP	CMPPOL	_	0000
CMP2DAC	0546	_	_	_	_						CMREF	<11:0>						0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER (CONTINUED)

- bit 3-0 NVMOP<3:0>: NVM Operation Select bits^(1,3,4)
 - 1111 = Reserved
 - •
 - .
 - 0101 = Reserved
 - 0100 = Reserved
 - 0011 = Memory page erase operation
 - 0010 = Memory row program operation
 - 0001 = Memory double-word program operation⁽⁵⁾
 - 0000 = Reserved
- **Note 1:** These bits can only be reset on a POR.
 - 2: If this bit is set, power consumption will be further reduced (IIDLE), and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.
 - 3: All other combinations of NVMOP<3:0> are unimplemented.
 - 4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
 - **5:** Two adjacent words on a 4-word boundary are programmed during execution of this operation.

REGISTER 5-2: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAD	R<15:8>			
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAE)R<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 NVMADR<15:0>: Nonvolatile Memory Lower Write Address bits

Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 8-6: LFSR: LINEAR FEEDBACK SHIFT REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				LFSR<14:8>	•		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LFSI	R<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown

bit 15 Unimplemented: Read as '0'

bit 14-0 LFSR<14:0>: Pseudorandom Data bits

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<7:0>
External Interrupt 2	INT2	RPINR1	INT2R<7:0>
Timer1 External Clock	T1CK	RPINR2	T1CKR<7:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<7:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<7:0>
Input Capture 1	IC1	RPINR7	IC1R<7:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<7:0>
PWM Fault 1	FLT1	RPINR12	FLT1R<7:0>
PWM Fault 2	FLT2	RPINR12	FLT2R<7:0>
PWM Fault 3	FLT3	RPINR13	FLT3R<7:0>
PWM Fault 4	FLT4	RPINR13	FLT4R<7:0>
UART1 Receive	U1RX	RPINR18	U1RXR<7:0>
UART1 Clear-to-Send	U1CTS	RPINR18	U1CTSR<7:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<7:0>
SPI1 Clock Input	SCK1	RPINR20	SCK1R<7:0>
SPI1 Slave Select	SS1	RPINR21	SS1R<7:0>
PWM Synchronous Input 1	SYNCI1	RPINR37	SYNCI1R<7:0>
PWM Synchronous Input 2	SYNCI2	RPINR38	SYNCI2R<7:0>
PWM Fault 5	FLT5	RPINR42	FLT5R<7:0>
PWM Fault 6	FLT6	RPINR42	FLT6R<7:0>
PWM Fault 7	FLT7	RPINR43	FLT7R<7:0>
PWM Fault 8	FLT8	RPINR43	FLT8R<7:0>

TABLE 10-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

REGISTER 10-5: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—		—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			IC1R	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-8	Unimplemen	ted: Read as '	0'				
bit 7-0	IC1R<7:0>: A	ssign Input Ca	pture 1 (IC1)	to the Corresp	onding RPn Pin	bits	
	10110101 =	Input tied to RF	P181				
	10110100 =	Input tied to RF	P180				
	•						
	•						
	00000001 =	Input tied to RF	P1				
	00000000 =	Input tied to Vs	S				

REGISTER 10-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15					•		bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			OCFA	R<7:0>			
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
							
bit 15-8	Unimplemen	ted: Read as '	0'				
bit 7-0	OCFAR<7:0>	: Assign Outpu	ut Compare Fa	ault A (OCFA)	to the Correspor	nding RPn Pin	bits
	10110101 =	Input tied to RF	P181				
	10110100 =	Input tied to RF	P180				
	•						
	•						
	00000001 =	Input tied to RF	P1				

00000000 =Input tied to Vss

16.1 SPI Helpful Tips

- 1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPI1CON2<13>) = 1, use a pull-down resistor on SS1.
 - b) If FRMPOL = 0, use a pull-up resistor on $\overline{SS1}$.

Note:	This	ensures	s tha	at	the	first	fr	ame
	transr	nission	after	in	itializa	ation	is	not
	shifte	d or corre	upted.					

- 2. In Non-Framed 3-Wire mode (i.e., not using SS1 from a master):
 - a) If CKP (SPI1CON1<6>) = 1, always place a pull-up resistor on SS1.
 - b) If CKP = <u>0</u>, always place a pull-down resistor on SS1.
 - **Note:** This will ensure that during power-up and initialization, the master/slave will not lose synchronization due to an errant SCK1 transition that would cause the slave to accumulate data shift errors for both transmit and receive, appearing as corrupted data.
- FRMEN (SPI1CON2<15>) = 1 and SSEN (SPI1CON1<7>) = 1 are exclusive and invalid. In Frame mode, SCK1 is continuous and the frame sync pulse is active on the SS1 pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame						
	mode	timing.	Refer	to	the	SPI1	
	specifications in Section 25.0 "Electric						
	Charac	cteristics	" for det	ails.			

 In Master mode only, set the SMP bit (SPI1CON1<9>) to a '1' for the fastest SPI1 data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPI1CON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPI1BUF Transmit register in advance of the next master transaction cycle. SPI1BUF is transferred to the SPI1 Shift register and is empty once the data transmission begins.

16.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

16.2.1 KEY RESOURCES

- "Serial Peripheral Interface (SPI)" (DS70005185) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 18-2: U1STA: UART1 STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	 PERR: Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	<pre>FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected</pre>
bit 1	 OERR: Receive Buffer Overrun Error Status bit (clear/read-only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the U1RSR to the empty state
bit 0	 URXDA: UART1 Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data, at least one more character can be read 0 = Receive buffer is empty

Note 1: Refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UART1 module for transmit operation.

REGISTER 19-2: ADCON1H: ADC CONTROL REGISTER 1 HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_	—	—	—	_	_	—	
bit 15							bit 8	
R/W-0	R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	
FORM	SHRRES1	SHRRES0	_	—	—	—	—	
bit 7							bit 0	
Legend:								
R = Readable bit		W = Writable bit		U = Unimpleme	ented bit, read	as '0'		
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-8	Unimplemented: Read as '0'							
bit 7	FORM: Fractional Data Output Format bit							
	1 = Fractional 0 = Integer							
bit 6-5	SHRRES<1:0>: Shared ADC Core Resolution Selection bits							
	11 = 12-bit resolution 10 = 10-bit resolution 01 = 8-bit resolution 00 = 6-bit resolution							
bit 4-0	Unimplemen	ted: Read as '0'						

20.0 HIGH-SPEED ANALOG COMPARATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed Analog Comparator Module" (DS70005128) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 2: Some registers and associated bits
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The high-speed analog comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

20.1 Features Overview

The SMPS comparator module offers the following major features:

- Two Rail-to-Rail Analog Comparators
- Dedicated 12-Bit DAC for each Analog Comparator
- Up to Six Selectable Input Sources per Comparator:
 - Four external inputs
 - Two internal inputs from the PGAx module
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Voltage References for the DACx:
 - AVDD
- Interrupt Generation Capability
- Functional Support for PWM:
 - PWM duty cycle control
 - PWM period control
 - PWM Fault detected

21.0 PROGRAMMABLE GAIN AMPLIFIER (PGA)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Programmable Gain Amplifier (PGA)" (DS70005146) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 family devices have two Programmable Gain Amplifiers (PGA1, PGA2). The PGA is an op amp-based, non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold inputs of the Analog-to-Digital Converter and/or to the high-speed analog comparator module. The PGA has five selectable gains and may be used as a ground referenced amplifier (single-ended) or used with an independent ground reference point.

Key features of the PGA module include:

- Single-Ended or Independent Ground Reference
- Selectable Gains: 4x, 8x, 16x, 32x and 64x
- High Gain Bandwidth
- Rail-to-Rail Output Voltage
- Wide Input Voltage Range

FIGURE 21-1: PGAx MODULE BLOCK DIAGRAM



21.1 Module Description

The programmable gain amplifiers are used to amplify small voltages (e.g., voltages across burden/shunt resistors) to improve the signal-to-noise ratio of the measured signal. The PGAx output voltage can be read by the two dedicated Sample-and-Hold circuits on the ADC module. The output voltage can also be fed to the comparator module for overcurrent/voltage protection. Figure 21-2 shows a functional block diagram of the PGAx module. Refer to Section 19.0 "High-Speed, 12-Bit Analog-to-Digital Converter (ADC)" and Section 20.0 "High-Speed Analog Comparator" for more interconnection details. The gain of the PGAx module is selectable via the GAIN<2:0> bits in the PGAxCON register. There are five selectable gains, ranging from 4x to 64x. The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of three positive/negative inputs to the PGAx module. For single-ended applications, the SELNI<2:0> bits will select ground as the negative input source. To provide an independent ground reference, the PGAxN2 pin is available as the negative input source to the PGAx module.



FIGURE 21-2: PGAx FUNCTIONAL BLOCK DIAGRAM

The different device security segments are shown in Figure 22-3. Here, all three segments are shown but are not required. If only basic code protection is required, then the GS can be enabled independently or combined with the CS if desired.

FIGURE 22-3:

dsPIC33EPXXGS202 SECURITY SEGMENTS EXAMPLE



NOTES:

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			2.00
Center Pad Length	Y2			2.00
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.85
Contact Pad to Center Pad (X28)	G1		0.52	
Contact Pad to Pad (X24)	G2	0.20		
Contact Pad to Corner Pad (X8)	G3	0.20		
Corner Anchor Width (X4)	X3			0.78
Corner Anchor Length (X4)	Y3			0.78
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2333-M6 Rev B

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-124C Sheet 1 of 2