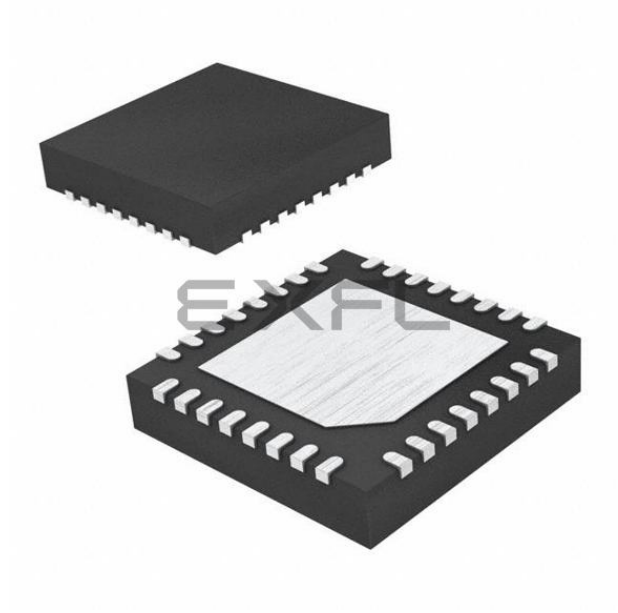
Microchip Technology - DSPIC33EP16GS202T-E/MM Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b, 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs202t-e-mm

Communication Interfaces

- One UART module (15 Mbps):
  - Supports LIN/J2602 protocols and IrDA®
- One 4-Wire SPI module (15 Mbps)
- One I^2C module (up to 1 Mbaud) with SMBus Support

Input/Output

- Sink/Source up to 12mA/15mA, respectively; Pin-Specific for Standard VOH/VOL
- 5V Tolerant Pins
- Selectable Open-Drain, Pull-ups and Pull-Downs
- External Interrupts on All I/O Pins
- Peripheral Pin Select (PPS) to allow Function Remap with Six Virtual I/Os

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- Class B Safety Library, IEC 60730
- 4x4x0.6 mm and 6x6x0.5 mm UQFN Packages are Designed and Optimized to ease IPC9592B 2nd Level Temperature Cycle Qualification

Debugger Development Support

- In-Circuit and In-Application Programming
- Three Program and One Complex Data Breakpoint
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

TABLE 1: dsPIC33EPXXGS202 FAMILY DEVICES

Device	Pins	Program Memory Bytes	RAM Bytes	Timers(1)	Remappable Peripherals					PWM	ADC Inputs	I^2C	ADC Cores	PGA	Analog Comparator	General Purpose I/O (GPIO)	Packages
					Input Capture	Output Compare	UART	SPI	External Interrupts(2)								
dsPIC33EP16GS202	28	16K	2K	3	1	1	1	1	3	3x2	12	1	3	2	2	21	SSOP, SOIC, QFN-S, UQFN (4x4 mm), UQFN (6x6 mm)
dsPIC33EP32GS202	28	32K	2K	3	1	1	1	1	3	3x2	12	1	3	2	2	21	

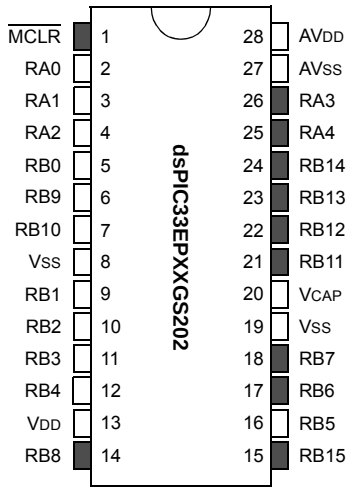
Note 1: The external clock for Timer1, Timer2 and Timer3 is remappable.

2: INT0 is not remappable; INT1 and INT2 are remappable.

Pin Diagrams

28-Pin SOIC,
28-Pin SSOP

■ = Pins are up to 5V tolerant



PIN FUNCTION DESCRIPTIONS

Pin	Pin Function	Pin	Pin Function
1	MCLR	15	PGEC3/**RP47**/RB15
2	AN0/PGA1P1/CMP1A/RA0	16	TDO/AN9/PGA2N2/**RP37**/RB5
3	AN1/PGA1P2/PGA2P1/CMP1B/RA1	17	PGED1/TDI/AN10/SCL1/**RP38**/RB6
4	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	18	PGEC1/AN11/SDA1/**RP39**/RB7
5	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0	19	VSS
6	AN4/CMP2C/**RP41**/RB9	20	VCAP
7	AN5/CMP2D/**RP42**/RB10	21	TMS/PWM3H/**RP43**/RB11
8	VSS	22	TCK/PWM3L/**RP44**/RB12
9	OSC1/CLKI/AN6/**RP33**/RB1	23	PWM2H/**RP45**/RB13
10	OSC2/CLKO/AN7/PGA1N2/**RP34**/RB2	24	PWM2L/**RP46**/RB14
11	PGED2/AN8/INT0/**RP35**/RB3	25	PWM1H/RA4
12	PGEC2/ADTRG31/**RP36**/RB4	26	PWM1L/RA3
13	VDD	27	AVSS
14	PGED3/**RP40**/RB8	28	AVDD

Legend: Shaded pins are up to 5 VDC tolerant.
Note: **RPn** represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN11	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
IC1	I	ST	Yes	Capture Input 1.
OCFA	I	ST	Yes	Compare Fault A input (for compare channels).
OC1	O	—	Yes	Compare Output 1.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
T1CK	I	ST	Yes	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	Yes	Timer3 external clock input.
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 Clear-to-Send.
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 Request-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
BCLK1	O	ST	Yes	UART1 IrDA® baud clock output.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
$\overline{\text{SS1}}$	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
FLT1-FLT8	I	ST	Yes	PWM Fault Inputs 1 through 8.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 through 3.
SYNCI1, SYNCI2	I	ST	Yes	PWM Synchronization Inputs 1 and 2.
SYNCO1, SYNCO2	O	—	Yes	PWM Synchronization Outputs 1 and 2.
CMP1A-CMP2A	I	Analog	No	Comparator Channels 1A through 2A inputs.
CMP1B-CMP2B	I	Analog	No	Comparator Channels 1B through 2B inputs.
CMP1C-CMP2C	I	Analog	No	Comparator Channels 1C through 2C inputs.
CMP1D-CMP2D	I	Analog	No	Comparator Channels 1D through 2D inputs.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

4.5 Special Function Register Maps

TABLE 4-2: CPU CORE REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																xxxx
W1	0002	W1																xxxx
W2	0004	W2																xxxx
W3	0006	W3																xxxx
W4	0008	W4																xxxx
W5	000A	W5																xxxx
W6	000C	W6																xxxx
W7	000E	W7																xxxx
W8	0010	W8																xxxx
W9	0012	W9																xxxx
W10	0014	W10																xxxx
W11	0016	W11																xxxx
W12	0018	W12																xxxx
W13	001A	W13																xxxx
W14	001C	W14																xxxx
W15	001E	W15																xxxx
SPLIM	0020	SPLIM																0000
ACCAL	0022	ACCAL																0000
ACCAH	0024	ACCAH																0000
ACCAU	0026	Sign Extension of ACCA<39>								ACCAU								0000
ACCBL	0028	ACCBL																0000
ACCBH	002A	ACCBH																0000
ACCBU	002C	Sign Extension of ACCB<39>								ACCBU								0000
PCL	002E	PCL<15:1>															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000
DSRPAG	0032	—	—	—	—	—	—	Extended Data Space (EDS) Read Page Register (DSRPAG<9:0>)										0001
DSWPAG(1)	0034	—	—	—	—	—	—	—	Extended Data Space (EDS) Write Page Register (DSWPAG8:0>)(1)									0001
RCOUNT	0036	RCOUNT<15:0>																0000
DCOUNT	0038	DO Loop Counter Register (DCOUNT<15:0>)																0000
DOSTARTL	003A	DO Loop Start Address Register Low (DOSTARTL<15:1>)															—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DO Loop Start Address Register High (DOSTARTH<5:0>)						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: The contents of this register should never be modified. The DSWPAG must always point to the first page.

TABLE 4-9: PWM GENERATOR 2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON2	0C40	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON2	0C42	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON2	0C44	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC2	0C46	PWM Generator 2 Duty Cycle Register (PDC2<15:0>)																0000
PHASE2	0C48	PWM Phase-Shift Value or Independent Time Base Period for the PWM Generator 2 Register (PHASE2<15:0>)																0000
DTR2	0C4A	—	—	DTR2<13:0>														0000
ALTDTR2	0C4C	—	—	ALTDTR2<13:0>														0000
SDC2	0C4E	SDC2<15:0>																0000
SPHASE2	0C50	SPHASE2<15:0>																0000
TRIG2	0C52	TRGCMP<12:0>													—	—	—	0000
TRGCON2	0C54	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG2	0C56	STRGCMP<12:0>													—	—	—	0000
PWMCAP2	0C58	PWMCAP<12:0>													—	—	—	0000
LEBCON2	0C5A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY2	0C5C	—	—	—	—	LEB<8:0>									—	—	—	0000
AUXCON2	0C5E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)

bit 3-0 **SEVTPS<3:0>:** PWM Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 Postscaler generates a Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 Postscaler generates a Special Event Trigger on every second compare match event
0000 = 1:1 Postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 15-2: PTCON2: PWM CLOCK DIVIDER SELECT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits(1)
111 = Reserved
110 = Divide-by-64, maximum PWM timing resolution
101 = Divide-by-32, maximum PWM timing resolution
100 = Divide-by-16, maximum PWM timing resolution
011 = Divide-by-8, maximum PWM timing resolution
010 = Divide-by-4, maximum PWM timing resolution
001 = Divide-by-2, maximum PWM timing resolution
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 15-3: PTPER: PWM PRIMARY MASTER TIME BASE PERIOD REGISTER(1,2)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTPER<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PTPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

Note 1: The PWM time base has a minimum value of 0x0010 and a maximum value of 0xFFF8.

2: Any period value that is less than 0x0028 must have the Least Significant 3 bits set to '0', thus yielding a period resolution at 8.32 ns (at fastest auxiliary clock rate).

REGISTER 15-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<12:5>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
SEVTCMP<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **SEVTCMP<12:0>:** Special Event Compare Count Value bits

bit 2-0 **Unimplemented:** Read as '0'

Note 1: One LSB = 1.04 ns (at fastest auxiliary clock rate); therefore, the minimum SEVTCMP resolution is 8.32 ns.

REGISTER 15-27: PWMCAPx: PWMx PRIMARY TIME BASE CAPTURE REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWMCAP<12:5>(1,2,3,4)							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	U-0	U-0	U-0
PWMCAP<4:0>(1,2,3,4)					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **PWMCAP<12:0>:** Captured PWMx Time Base Value bits(1,2,3,4)
The value in this register represents the captured PWMx time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: The capture feature is only available on a primary output (PWMxH).
2: This feature is active only after LEB processing on the current-limit input signal is complete.
3: The minimum capture resolution is 8.32 ns.
4: This feature can be used when the XPRES bit (PWMCONx<1>) is set to ‘0’.

REGISTER 17-1: I2C1CONL: I2C1 CONTROL REGISTER LOW (CONTINUED)

bit 6 **STREN:** SCL1 Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on the SDA1 and SCL1 pins and transmits the ACKDT data bit. Hardware clears it at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C. Hardware clears it at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on the SDA1 and SCL1 pins. Hardware clears it at the end of the master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on the SDA1 and SCL1 pins. Hardware clears it at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on the SDA1 and SCL1 pins. Hardware clears it at the end of the master Start sequence.
0 = Start condition is not in progress

REGISTER 19-8: ADCON4H: ADC CONTROL REGISTER 4 HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	C1CHS1	C1CHS0	C0CHS1	C0CHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-2 **C1CHS<1:0>:** Dedicated ADC Core 1 Input Channel Selection bits
11 = PGA2
10 = PGA1
01 = AN8
00 = AN1
AN8 is a negative input when DIFF1 (ADMOD0L<3>) = 1.

bit 1-0 **C0CHS<1:0>:** Dedicated ADC Core 0 Input Channel Selection bits
11 = PGA2
10 = PGA1
01 = AN7
00 = AN0
AN7 is a negative input when DIFF0 (ADMOD0L<1>) = 1.

REGISTER 19-22: ADCAL0L: ADC CALIBRATION REGISTER 0 LOW

R-0, HC, HS	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL1RDY	—	—	—	CAL1SKIP	CAL1DIFF	CAL1EN	CAL1RUN
bit 15							bit 8

R-0, HC, HS	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL0RDY	—	—	—	CAL0SKIP	CAL0DIFF	CAL0EN	CAL0RUN
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CAL1RDY:** Dedicated ADC Core 1 Calibration Status Flag bit
1 = Dedicated ADC Core 1 calibration is finished
0 = Dedicated ADC Core 1 calibration is in progress

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CAL1SKIP:** Dedicated ADC Core 1 Calibration Bypass bit
1 = After power-up, the dedicated ADC Core 1 will not be calibrated
0 = After power-up, the dedicated ADC Core 1 will be calibrated

bit 10 **CAL1DIFF:** Dedicated ADC Core 1 Pseudo-Differential Input Mode Calibration bit
1 = Dedicated ADC Core 1 will be calibrated in Pseudo-Differential Input mode
0 = Dedicated ADC Core 1 will be calibrated in Single-Ended Input mode

bit 9 **CAL1EN:** Dedicated ADC Core 1 Calibration Enable bit
1 = Dedicated ADC Core 1 calibration bits (CALxRDY, CALxSKIP, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 1 calibration bits are disabled

bit 8 **CAL1RUN:** Dedicated ADC Core 1 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 1 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

bit 7 **CAL0RDY:** Dedicated ADC Core 0 Calibration Status Flag bit
1 = Dedicated ADC Core 0 calibration is finished
0 = Dedicated ADC Core 0 calibration is in progress

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **CAL0SKIP:** Dedicated ADC Core 0 Calibration Bypass bit
1 = After power-up, the dedicated ADC Core 0 will not be calibrated
0 = After power-up, the dedicated ADC Core 0 will be calibrated

bit 2 **CAL0DIFF:** Dedicated ADC Core 0 Pseudo-Differential Input Mode Calibration bit
1 = Dedicated ADC Core 0 will be calibrated in Pseudo-Differential Input mode
0 = Dedicated ADC Core 0 will be calibrated in Single-Ended Input mode

bit 1 **CAL0EN:** Dedicated ADC Core 0 Calibration Enable bit
1 = Dedicated ADC Core 0 calibration bits (CALxRDY, CALxSKIP, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 0 calibration bits are disabled

bit 0 **CAL0RUN:** Dedicated ADC Core 0 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 0 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

REGISTER 19-26: ADFL0CON: ADC DIGITAL FILTER 0 CONTROL REGISTER (CONTINUED)

bit 4-0 **FLCHSEL<4:0>:** Oversampling Filter Input Channel Selection bits
01111-11111 = Reserved
01110 = AN14
•
•
•
00001 = AN1
00000 = AN0

22.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXGS202 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

22.1 Configuration Bits

In the dsPIC33EPXXGS202 family devices, the Configuration Words are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 22-1 with detailed descriptions in Table 22-2. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

NOTES:

25.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXGS202 family AC characteristics and timing parameters.

TABLE 25-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 25.1 "DC Characteristics"**.

FIGURE 25-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

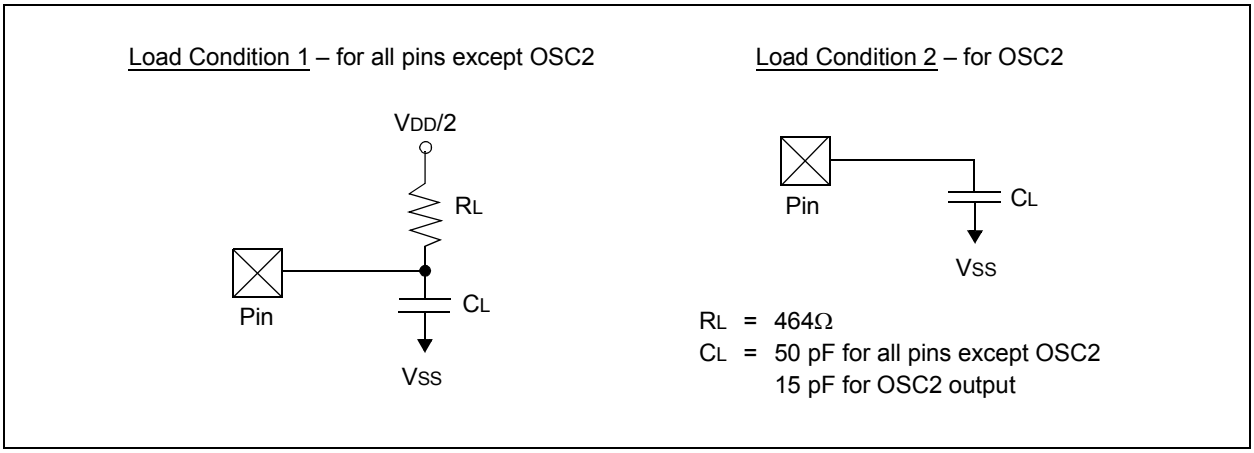


TABLE 25-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCL1, SDA1	—	—	400	pF	In I^2C mode

TABLE 25-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1,2)							
F20a	FRC	-2	0.5	+2	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-0.9	0.5	+0.9	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-2	1	+2	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

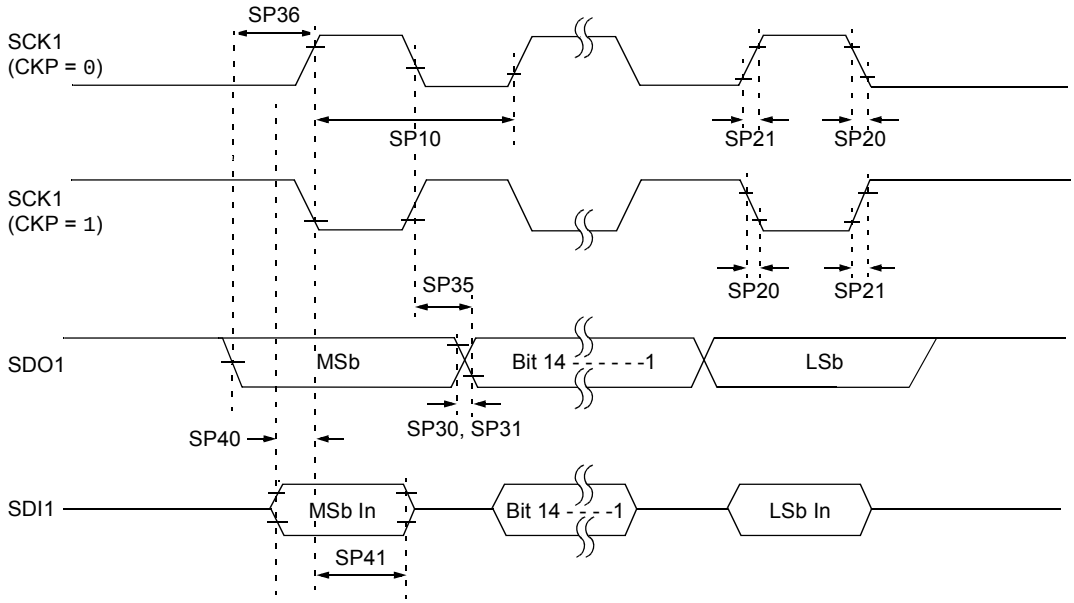
2: Over the lifetime of the 28-Lead 4x4 UQFN package device, the internal FRC accuracy could vary between ±4%.

TABLE 25-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
LPRC @ 32.768 kHz(1)							
F21a	LPRC	-30	—	+30	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-20	—	+20	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F21b	LPRC	-30	—	+30	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: This is the change of the LPRC frequency as VDD changes.

FIGURE 25-13: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 25-1 for load conditions.

TABLE 25-33: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	9	MHz	**(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid After SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

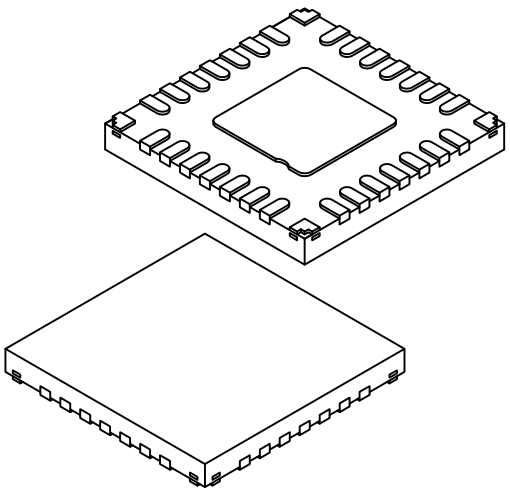
2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	-	-	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.80	1.90	2.00
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.80	1.90	2.00
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1	0.40	0.45	0.50
Corner Pad, Metal Free Zone	b2	0.18	0.23	0.28
Terminal Length	L	0.30	0.45	0.50
Terminal-to-Exposed-Pad	K	-	0.60	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

INDEX