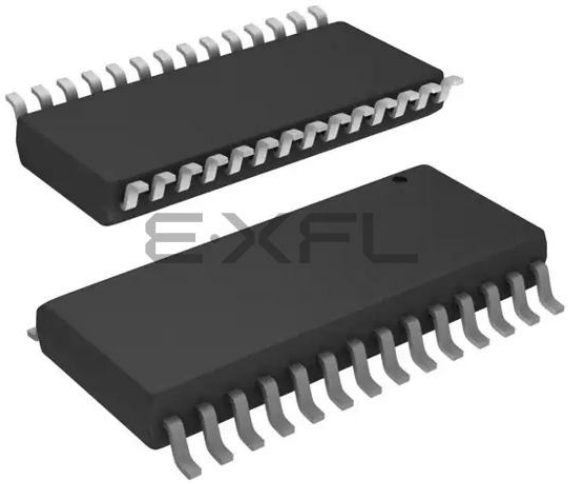
# Microchip Technology - DSPIC33EP16GS202T-E/SO Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 12x12b, 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs202t-e-so |

### 4.2.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-3).

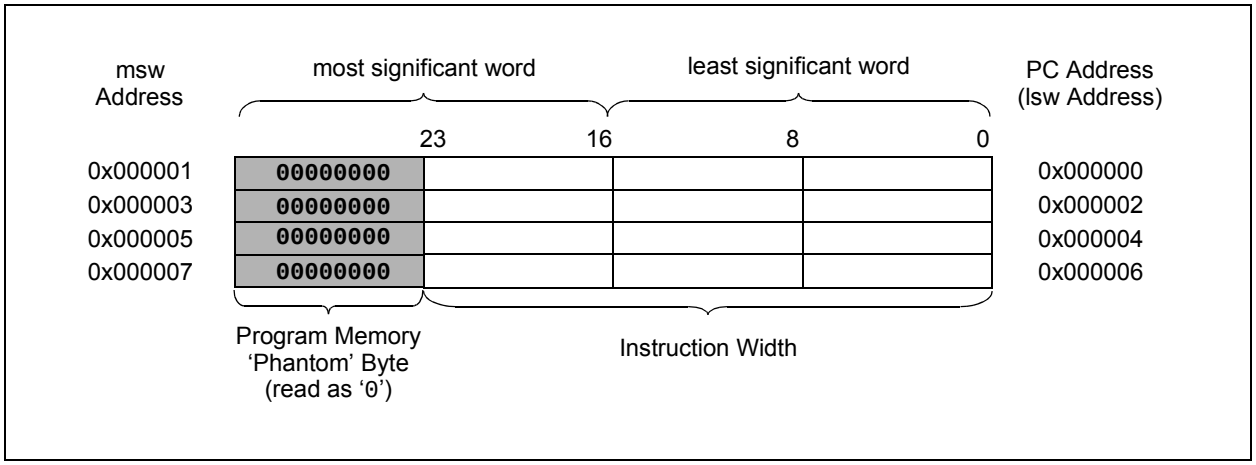
Program memory addresses are always word-aligned on the lower word, and addresses are incremented, or decremented, by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.2.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXGS202 family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1 "Interrupt Vector Table"**.

**FIGURE 4-3: PROGRAM MEMORY ORGANIZATION**



## 4.5 Special Function Register Maps

### TABLE 4-2: CPU CORE REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 |
| ACCAL | 0022 | ACCAL | | | | | | | | | | | | | | | | 0000 |
| ACCAH | 0024 | ACCAH | | | | | | | | | | | | | | | | 0000 |
| ACCAU | 0026 | Sign Extension of ACCA<39> | | | | | | | | ACCAU | | | | | | | | 0000 |
| ACCBL | 0028 | ACCBL | | | | | | | | | | | | | | | | 0000 |
| ACCBH | 002A | ACCBH | | | | | | | | | | | | | | | | 0000 |
| ACCBU | 002C | Sign Extension of ACCB<39> | | | | | | | | ACCBU | | | | | | | | 0000 |
| PCL | 002E | PCL<15:1> | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH<6:0> | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | Extended Data Space (EDS) Read Page Register (DSRPAG<9:0>) | | | | | | | | | | 0001 |
| DSWPAG(1) | 0034 | — | — | — | — | — | — | — | Extended Data Space (EDS) Write Page Register (DSWPAG8:0>)(1) | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| DCOUNT | 0038 | DO Loop Counter Register (DCOUNT<15:0>) | | | | | | | | | | | | | | | | 0000 |
| DOSTARTL | 003A | DO Loop Start Address Register Low (DOSTARTL<15:1>) | | | | | | | | | | | | | | | — | 0000 |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | — | DO Loop Start Address Register High (DOSTARTH<5:0>) | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note 1:** The contents of this register should never be modified. The DSWPAG must always point to the first page.

### 10.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than $V_{DD}$ by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum $V_{IH}$ specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 25-11 for the maximum $V_{IH}$ specification for each pin.

## 10.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UART, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level ($V_{OH}$ or $V_{OL}$) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin, defined as a digital input (including the ANx pins), can cause the input buffer to consume current that exceeds the device specifications.

### 10.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP, as shown in Example 10-1.

## 10.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the ICN functionality of each I/O port. The CNENx registers contain the ICN interrupt enable control bits for each of the input pins. Setting any of these bits enables an ICN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source, or sink source, connected to the pin, and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

| **Note:** | Pull-ups and pull-downs on Input Change Notification pins should always be disabled when the port pin is configured as a digital output. |
|---|---|

**EXAMPLE 10-1: PORT WRITE/READ**

```
MOV   0xFF00, W0   ; Configure PORTB<15:8>
                   ; as inputs
MOV   W0, TRISB    ; and PORTB<7:0>
                   ; as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```

## 10.7 Peripheral Pin Select Registers

**REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INT1R<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **INT1R<7:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as ‘0’

**REGISTER 10-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INT2R<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **INT2R<7:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits
10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

**REGISTER 10-24: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP177R5 | RP177R4 | RP177R3 | RP177R2 | RP177R1 | RP177R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP176R5 | RP176R4 | RP176R3 | RP176R2 | RP176R1 | RP176R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP177R<5:0>:** Peripheral Output Function is Assigned to RP177 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP176R<5:0>:** Peripheral Output Function is Assigned to RP176 Output Pin bits (see Table 10-2 for peripheral function numbers)

**REGISTER 10-25: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP179R5 | RP179R4 | RP179R3 | RP179R2 | RP179R1 | RP179R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP178R5 | RP178R4 | RP178R3 | RP178R2 | RP178R1 | RP178R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP179R<5:0>:** Peripheral Output Function is Assigned to RP179 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP178R<5:0>:** Peripheral Output Function is Assigned to RP178 Output Pin bits (see Table 10-2 for peripheral function numbers)

## 11.0 TIMER1

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode from an External Clock Source
- The External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

A block diagram of Timer1 is shown in Figure 11-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

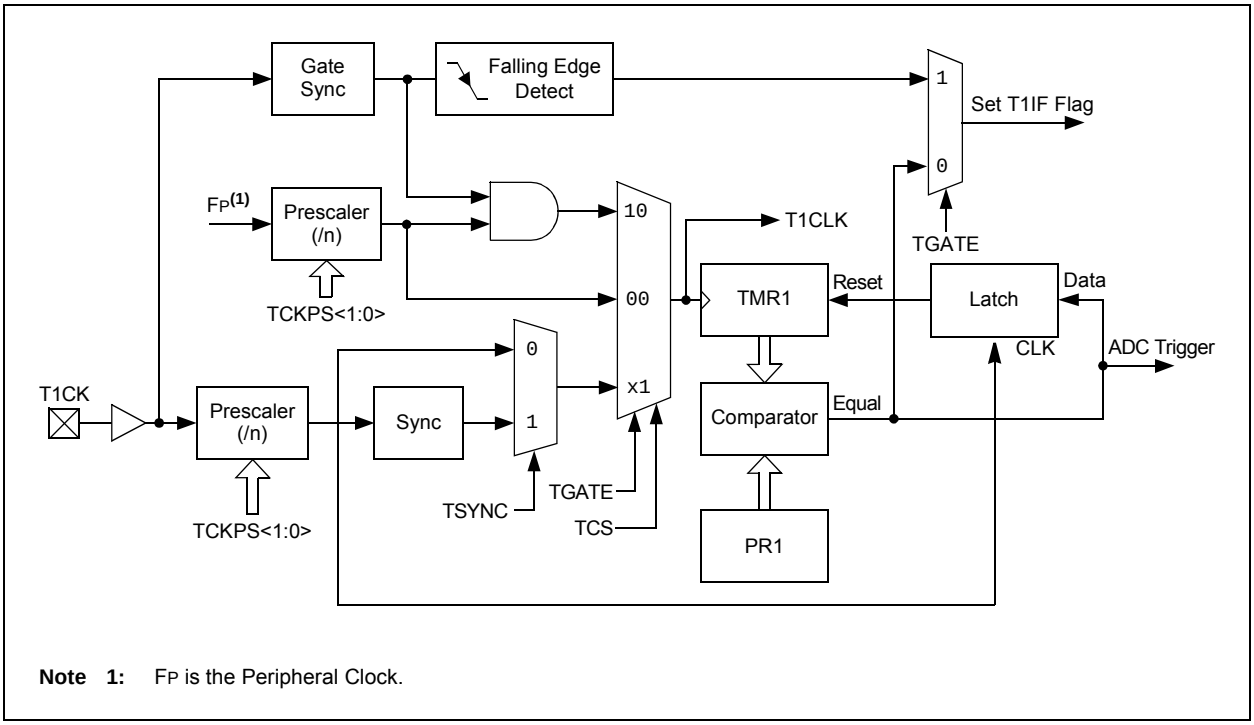
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit settings for different operating modes are provided in Table 11-1.

**TABLE 11-1: TIMER MODE SETTINGS**

| Mode | TCS | TGATE | TSYNC |
|---|---|---|---|
| Timer | 0 | 0 | x |
| Gated Timer | 0 | 1 | x |
| Synchronous Counter | 1 | x | 1 |
| Asynchronous Counter | 1 | x | 0 |

**FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**




**Note 1:** FP is the Peripheral Clock.

**REGISTER 12-2: T3CON: TIMER3 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL(2) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(1) | TCKPS1(1) | TCKPS0(1) | — | — | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timer3 On bit(1)
1 = Starts 16-bit Timer3
0 = Stops 16-bit Timer3

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer3 Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer3 Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer3 Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer3 Clock Source Select bit(1)
1 = External clock is from pin, T3CK (on the rising edge)
0 = Peripheral Clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timer3 operation; all timer functions are set through T2CON.

**2:** When 32-bit timer operation is enabled (T32 = 1) in the Timer2 Control register (T2CON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU(1) | SYNCPOL(1) | SYNCOEN(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SYNCEN(1) | SYNCSRC2(1) | SYNCSRC1(1) | SYNCSRC0(1) | SEVTPS3(1) | SEVTPS2(1) | SEVTPS1(1) | SEVTPS0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWM cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)
1 = SYNCIx/SYNCO1 polarity is inverted (active-low)
0 = SYNCIx/SYNCO1 is active-high

bit 8 **SYNCOEN:** Primary Time Base Synchronization Enable bit(1)
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits(1)
111 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved
010 = Reserved
001 = SYNCI2
000 = SYNCI1

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**REGISTER 15-12: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)**

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Reserved
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all Output modes

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWMx generator uses the secondary master time base for synchronization and the clock source for the PWMx generation logic (if secondary time base is available)
0 = PWMx generator uses the primary master time base for synchronization and the clock source for the PWMx generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,3,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWMx generator if it is in Independent Time Base mode
0 = External pins do not affect the PWMx time base

bit 0 **IUE:** Immediate Update Enable bit
1 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are immediate
0 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are synchronized to the local PWMx time base

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx register in the interrupt controller.
**2:** The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**3:** These bits should not be changed after the PWM is enabled by setting PTEN (PTCON<15>) = 1.
**4:** Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
**5:** Configure CLMOD (FCLCONx<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

**REGISTER 15-13: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER(1,2,3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PDCx<15:0>:** PWMx Generator Duty Cycle Value bits

**Note 1:** In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In the Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL.

**2:** The smallest pulse width that can be generated on the PWMx output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

**3:** As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from 1 to 3 LSBs.

**REGISTER 15-14: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER(1,2,3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SDCx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SDCx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **SDCx<15:0>:** Secondary Duty Cycle for PWMxL Output Pin bits

**Note 1:** The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.

**2:** The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

**3:** As the duty cycle gets closer to 0% or 100% of the PWM period (0 to 40 ns, depending on the mode of operation), PWM duty cycle resolution will increase from 1 to 3 LSBs.

**REGISTER 15-24: LEBCONx: PWMx LEADING-EDGE BLANKING (LEB) CONTROL REGISTER (CONTINUED)**

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
0 = No blanking when the PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
0 = No blanking when the PWMxL output is low

**Note 1:** The blanking signal is selected via the BLANKSEL<3:0> bits in the AUXCONx register.

**REGISTER 15-25: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LEB<8:5> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| LEB<4:0> | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-3 **LEB<8:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits
The value is in 8.32 ns increments.

bit 2-0 **Unimplemented:** Read as ‘0’

**REGISTER 17-2: I2C1CONH: I2C1 CONTROL REGISTER HIGH**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit ($I^2C$ Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit ($I^2C$ Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit ($I^2C$ Slave mode only)
1 = I2C1RCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if the RBF bit = 0
0 = I2C1RCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDA1 Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDA1 after the falling edge of SCL1
0 = Minimum of 100 ns hold time on SDA1 after the falling edge of SCL1

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit ($I^2C$ Slave mode only)
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled
If the rising edge of SCL1 and SDA1 is sampled low when the module is in a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

bit 1 **AHEN:** Address Hold Enable bit ($I^2C$ Slave mode only)
1 = Following the 8th falling edge of SCL1 for a matching received address byte, the SCLREL (I2C1CONL<12>) bit will be cleared and SCL1 will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit ($I^2C$ Slave mode only)
1 = Following the 8th falling edge of SCL1 for a received data byte, the slave hardware clears the SCLREL (I2C1CONL<12>) bit and SCL1 is held low
0 = Data holding is disabled

## 19.0 HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)**" (DS70005213) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS202 devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC, DC/DC power converters.

### 19.1 Features Overview

The 12-Bit High Speed Multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- 12-Bit Resolution
- Up to 3.25 Msps Conversion Rate per ADC Core @ 12-Bit Resolution
- Multiple Dedicated ADC Cores
- One Shared (common) ADC Core
- Up to 12 Analog Input Sources
- Conversion Result can be Formatted as Unsigned or Signed Data on a per Channel Basis for All Channels
- Separate 16-Bit Conversion Result Register for each Analog Input
- Simultaneous Sampling of up to 3 Analog Inputs
- Flexible Trigger Options
- Early Interrupt Generation to Enable Fast Processing of Converted Data
- Two Integrated Digital Comparators:
  - Multiple comparison options
  - Assignable to specific analog inputs
- Oversampling Filters:
  - Provides increased resolution
  - Assignable to a specific analog input
- Operation During CPU Sleep and Idle modes

Simplified block diagrams of the Multiple SARs 12-Bit ADC are shown in Figure 19-1, Figure 19-2 and Figure 19-3.

The module consists of two independent SAR ADC cores. The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S/H) circuit of each ADC core. The core uses the channel information (the output format, the measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC module can sample up to three inputs at a time (two inputs from the dedicated SAR ADC cores and one from the shared SAR ADC cores). If multiple ADC inputs request conversion, the ADC module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

**REGISTER 19-6: ADCON3H: ADC CONTROL REGISTER 3 HIGH**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CLKSEL1 | CLKSEL0 | CLKDIV5 | CLKDIV4 | CLKDIV3 | CLKDIV2 | CLKDIV1 | CLKDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SHREN | — | — | — | — | — | C1EN | C0EN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **CLKSEL<2:0>:** ADC Module Clock Source Selection bits

11 = APLL
10 = FRC
01 = FOSC (System Clock x 2)
00 = FSYS (System Clock)

bit 13-8 **CLKDIV<5:0>:** ADC Module Clock Source Divider bits

The divider forms a TCORESRC clock used by all ADC cores (shared and dedicated) from the TSRC ADC module clock source selected by the CLKSEL<2:0> bits. Then, each ADC core individually divides the TCORESRC clock to get a core-specific TADCORE clock using the ADCS<6:0> bits in the ADCOREXH register or the SHRADCS<6:0> bits in the ADCON2L register.

111111 = 64 Core Source Clock periods
•
•
•
000011 = 4 Core Source Clock periods
000010 = 3 Core Source Clock periods
000001 = 2 Core Source Clock periods
000000 = 1 Core Source Clock period

bit 7 **SHREN:** Shared ADC Core Enable bit

This bit does not disable the core clock and analog bias circuitry.
1 = Shared ADC core is enabled
0 = Shared ADC core is disabled

bit 6-2 **Unimplemented:** Read as ‘0’

bit 1-0 **C1EN:C0EN:** Dedicated ADC Core x Enable bits

This bit does not disable the core clock and analog bias circuitry.
1 = Dedicated ADC Core x is enabled
0 = Dedicated ADC Core x is disabled

**REGISTER 19-21: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 3)**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | TRGSRC(4x+3)<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | TRGSRC(4x+2)<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(4x+3)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Reserved
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = Reserved
10010 = Reserved
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = Reserved
01000 = Reserved
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

## 25.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the dsPIC33EPXXGS202 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXGS202 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to $V_{SS}$(3) ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 3.0V$(3) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} < 3.0V$(3) ..... -0.3V to +3.6V
Maximum current out of $V_{SS}$ pin ..... 300 mA
Maximum current into $V_{DD}$ pin(2) ..... 300 mA
Maximum current sunk/sourced by any 4x I/O pin ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin ..... 25 mA
Maximum current sunk by all ports(2) ..... 200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 25-2).

**3:** See the **“Pin Diagrams”** section for the 5V tolerant pins.

**TABLE 25-8: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **Power-Down Current ($I_{PD}$)(1)** | | | | | |
| DC60d | 10 | 30 | μA | -40°C | 3.3V |
| DC60a | 16 | 60 | μA | +25°C | |
| DC60b | 60 | 300 | μA | +85°C | |
| DC60c | 300 | 800 | μA | +125°C | |

**Note 1:** $I_{PD}$ (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as output and driving low.
- $\overline{MCLR}$ = $V_{DD}$, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

**TABLE 25-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT ($\Delta I_{WDT}$)(1)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| DC61d | 1 | 2 | μA | -40°C | 3.3V |
| DC61a | 1 | 2 | μA | +25°C | |
| DC61b | 1 | 3 | μA | +85°C | |
| DC61c | 2 | 5 | μA | +125°C | |

**Note 1:** The $\Delta I_{WDT}$ current is the additional current consumed when the module is enabled. This current should be added to the base $I_{PD}$ current. All parameters are characterized but not tested during manufacturing.

**TABLE 25-46: PGAx MODULE SPECIFICATIONS**

| AC/DC CHARACTERISTICS(1) | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| PA01 | VIN | Input Voltage Range | | AVSS – 0.3 | — | AVDD + 0.3 | V | |
| PA02 | VCM | Common-Mode Input Voltage Range | | AVSS | — | AVDD – 1.6 | V | |
| PA03 | VOS | Input Offset Voltage | | -20 | — | +20 | mV | |
| PA04 | VOS | Input Offset Voltage Drift with Temperature | | — | ±15 | — | µV/°C | |
| PA05 | RIN+ | Input Impedance of Positive Input | | — | >1M \|\| 7 pf | — | Ω\|\| pF | |
| PA06 | RIN- | Input Impedance of Negative Input | | — | 10K \|\| 7 pf | — | Ω\|\| pF | |
| PA07 | GERR | Gain Error | | -2 | — | +2 | % | Gain = 4x and 8x |
| | | | | -3 | — | +3 | % | Gain = 16x |
| | | | | -4 | — | +4 | % | Gain = 32x and 64x |
| PA08 | LERR | Gain Nonlinearity Error | | — | — | 0.5 | % | % of full scale, Gain = 16x |
| PA09 | IDD | Current Consumption | | — | 2.0 | — | mA | Module is enabled with a 2-volt P-P output voltage swing |
| PA10a | BW | Small Signal Bandwidth (-3 dB) | G = 4x | — | 10 | — | MHz | |
| PA10b | | | G = 8x | — | 5 | — | MHz | |
| PA10c | | | G = 16x | — | 2.5 | — | MHz | |
| PA10d | | | G = 32x | — | 1.25 | — | MHz | |
| PA10e | | | G = 64x | — | 0.625 | — | MHz | |
| PA11 | OST | Output Settling Time to 1% of Final Value | | — | 0.4 | — | µs | Gain = 16x, 100 mV input step change |
| PA12 | SR | Output Slew Rate | | — | 40 | — | V/µs | Gain = 16x |
| PA13 | TGSEL | Gain Selection Time | | — | 1 | — | µs | |
| PA14 | TON | Module Turn On/Setting Time | | — | — | 10 | µs | |

**Note 1:** The PGAx module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

## 26.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 26-1: VOH – 4x DRIVER PINS**

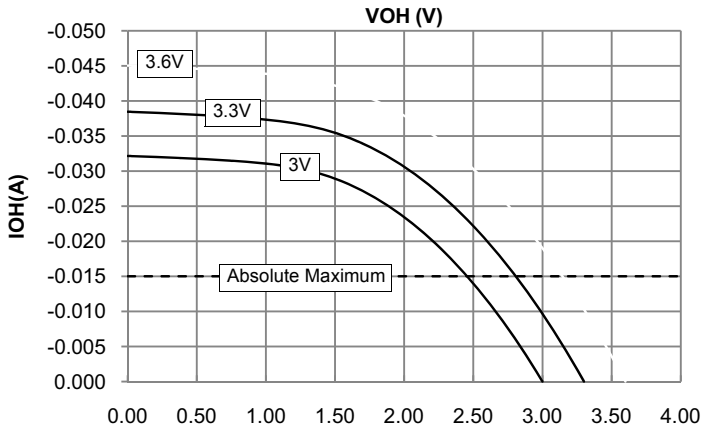



**FIGURE 26-2: VOH – 8x DRIVER PINS**

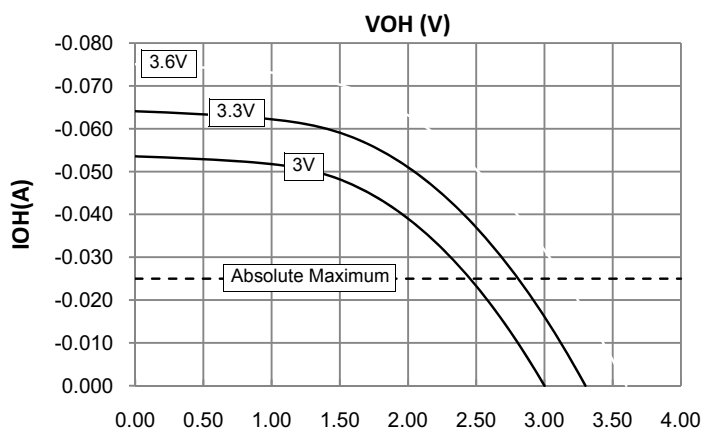



**FIGURE 26-3: VOL – 4x DRIVER PINS**

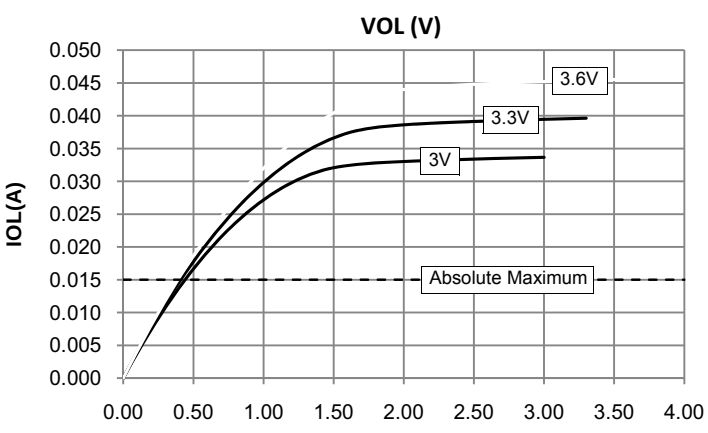
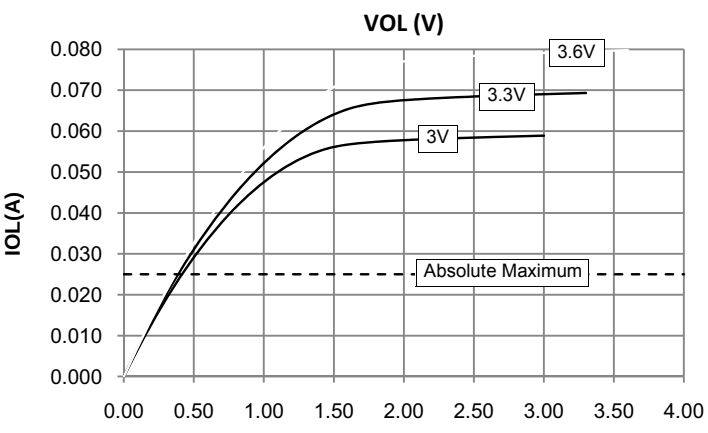



**FIGURE 26-4: VOL – 8x DRIVER PINS**



**NOTES:**