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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs202-i-ss

dsPIC33EPXXGS202 FAMILY

Communication Interfaces

- One UART module (15 Mbps):
 - Supports LIN/J2602 protocols and IrDA®
- One 4-Wire SPI module (15 Mbps)
- One I²C module (up to 1 Mbaud) with SMBus Support

Input/Output

- Sink/Source up to 12mA/15mA, respectively; Pin-Specific for Standard V_{OH}/V_{OL}
- 5V Tolerant Pins
- Selectable Open-Drain, Pull-ups and Pull-Downs
- External Interrupts on All I/O Pins
- Peripheral Pin Select (PPS) to allow Function Remap with Six Virtual I/Os

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- Class B Safety Library, IEC 60730
- 4x4x0.6 mm and 6x6x0.5 mm UQFN Packages are Designed and Optimized to ease IPC9592B 2nd Level Temperature Cycle Qualification

Debugger Development Support

- In-Circuit and In-Application Programming
- Three Program and One Complex Data Breakpoint
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

TABLE 1: dsPIC33EPXXGS202 FAMILY DEVICES

Device	Pins	Program Memory Bytes	RAM Bytes	Timers ⁽¹⁾	Remappable Peripherals					PWM	ADC Inputs	I ² C	ADC Cores	PGA	Analog Comparator	General Purpose I/O (GPIO)	Packages
					Input Capture	Output Compare	UART	SPI	External Interrupts ⁽²⁾								
dsPIC33EP16GS202	28	16K	2K	3	1	1	1	1	3	3x2	12	1	3	2	2	21	SSOP, SOIC, QFN-S, UQFN (4x4 mm), UQFN (6x6 mm)
dsPIC33EP32GS202	28	32K	2K	3	1	1	1	1	3	3x2	12	1	3	2	2	21	

Note 1: The external clock for Timer1, Timer2 and Timer3 is remappable.

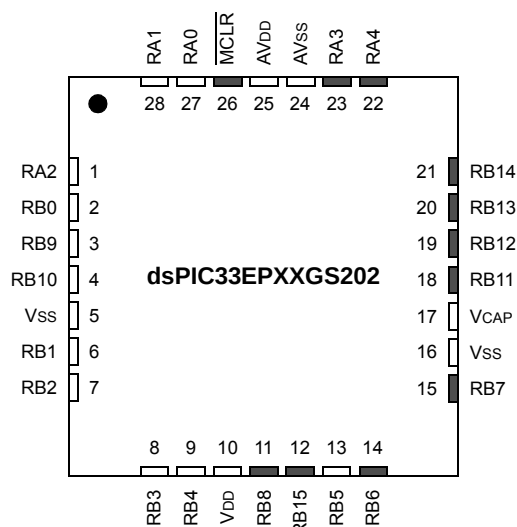
Note 2: INT0 is not remappable; INT1 and INT2 are remappable.

dsPIC33EPXXGS202 FAMILY

Pin Diagrams (Continued)

28-Pin UQFN 4x4 mm, 28-Pin UQFN 6x6 mm,
28-Pin QFN-S 6x6 mm

■ = Pins are up to 5V tolerant



PIN FUNCTION DESCRIPTIONS

Pin	Pin Function	Pin	Pin Function
1	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	15	PGEC1/AN11/SDA1/ RP39 /RB7
2	AN3/PGA2P3/CMP1D/ CMP28/ RP32 /RB0	16	Vss
3	AN4/CMP2C/ RP41 /RB9	17	VCAP
4	AN5/CMP2D/ RP42 /RB10	18	TMS/PWM3H/ RP43 /RB11
5	Vss	19	TCK/PWM3L/ RP44 /RB12
6	OSC1/CLKI/AN6/ RP33 /RB1	20	PWM2H/ RP45 /RB13
7	OSC2/CLKO/AN7/PGA1N2/ RP34 /RB2	21	PWM2L/ RP46 /RB14
8	PGED2/AN8/INT0/ RP35 /RB3	22	PWM1H/RA4
9	PGEC2/ADTRG31/ RP36 /RB4	23	PWM1L/RA3
10	Vdd	24	AVss
11	PGED3/ RP40 /RB8	25	AVdd
12	PGEC3/ RP47 /RB15	26	MCLR
13	TDO/AN9/PGA2N2/ RP37 /RB5	27	AN0/PGA1P1/CMP1A/RA0
14	PGED1/TDI/AN10/SCL1/ RP38 /RB6	28	AN1/PGA1P2/PGA2P1/CMP1B/RA1

Legend: Shaded pins are up to 5 VDC tolerant.

Note: **RPn** represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.6.1 KEY RESOURCES

- “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

dsPIC33EPXXGS202 FAMILY

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	SFA: Stack Frame Active Status bit 1 = Stack frame is active; W14 and W15 address of 0x0000 to 0xFFFF, regardless of DSRPAG 0 = Stack frame is not active; W14 and W15 address of Base Data Space
bit 1	RND: Rounding Mode Select bit 1 = Biased (conventional) rounding is enabled 0 = Unbiased (convergent) rounding is enabled
bit 0	IF: Integer or Fractional Multiplier Mode Select bit 1 = Integer mode is enabled for DSP multiply 0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	CCTXI2	CCTXI1	CCTXI0
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	MCTXI2	MCTXI1	MCTXI0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **CCTXI<2:0>:** Current (W Register) Context Identifier bits

111 = Reserved

•
•
•

011 = Reserved

010 = Alternate Working Register Set 2 is currently in use

001 = Alternate Working Register Set 1 is currently in use

000 = Default register set is currently in use

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **MCTXI<2:0>:** Manual (W Register) Context Identifier bits

111 = Reserved

•
•
•

011 = Reserved

010 = Alternate Working Register Set 2 was most recently manually selected

001 = Alternate Working Register Set 1 was most recently manually selected

000 = Default register set was most recently manually selected

TABLE 4-7: PWM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PWM Primary Master Time Base Period Register (PTPER<15:0>)																FFF8
SEVTCMP	0C06	PWM Special Event Compare Register (SEVTCMP12:0>)													—	—	—	0000
MDC	0C0A	MDC<15:0>																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	PWM Secondary Master Time Base Period Register (STPER<15:0>)																FFF8
SSEVTCMP	0C14	PWM Secondary Special Event Compare Register (SSEVTCMP<12:0>)													—	—	—	0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0	—	—	—	0000
PWMKEY	0C1E	PWM Protection Lock/Unlock Key Value Register (PWMKEY<15:0>)																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: PWM GENERATOR 1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEEN	CLIEEN	TRGIEEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON1	0C24	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC1	0C26	PWM Generator 1 Duty Cycle Register (PDC1<15:0>)																0000
PHASE1	0C28	PWM Phase-Shift Value or Independent Time Base Period for the PWM Generator 1 Register (PHASE1<15:0>)																0000
DTR1	0C2A	—	—	DTR1<13:0>														0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>														0000
SDC1	0C2E	SDC1<15:0>																0000
SPHASE1	0C30	SPHASE1<15:0>																0000
TRIG1	0C32	TRGCMP<12:0>													—	—	—	0000
TRGCON1	0C34	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG1	0C36	STRGCMP<12:0>													—	—	—	0000
PWMCAP1	0C38	PWMCAP<12:0>													—	—	—	0000
LEBON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB<8:0>									—	—	—	0000
AUXCON1	0C3E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXGS202 FAMILY

6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Reset” (DS70602) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
 - Illegal Opcode Reset
 - Uninitialized W Register Reset
 - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state, and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 “Memory Organization”** of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

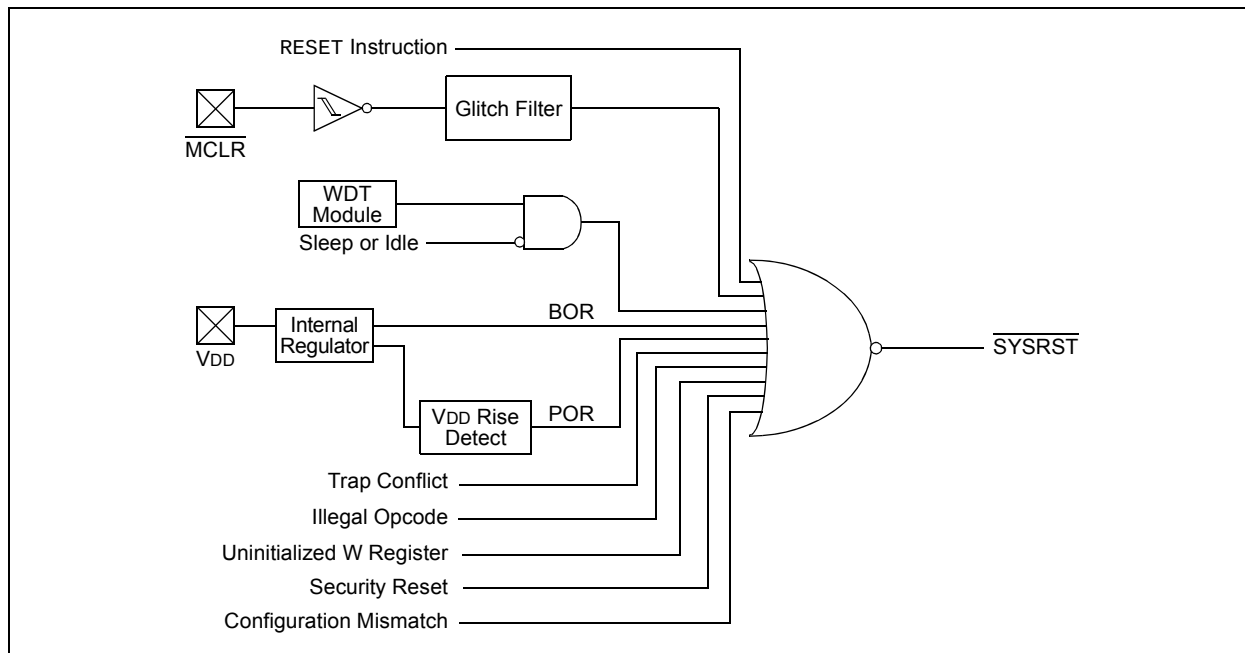
A POR clears all the bits, except for the BOR and POR bits (RCON<1:0>) that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSCx bits is loaded into the NOSC<2:0> (OSCCON<10:8>) bits on Reset, which in turn, initializes the system clock.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



dsPIC33EPXXGS202 FAMILY

FIGURE 7-1: dsPIC33EPXXGS202 FAMILY INTERRUPT VECTOR TABLE

Decreasing Natural Order Priority ↓ IVT ↑	Reset – GOTO Instruction	0x000000	See Table 7-1 for Interrupt Vector Details
	Reset – GOTO Address	0x000002	
	Oscillator Fail Trap Vector	0x000004	
	Address Error Trap Vector	0x000006	
	Generic Hard Trap Vector	0x000008	
	Stack Error Trap Vector	0x00000A	
	Math Error Trap Vector	0x00000C	
	Reserved	0x00000E	
	Generic Soft Trap Vector	0x000010	
	Reserved	0x000012	
	Interrupt Vector 0	0x000014	
	Interrupt Vector 1	0x000016	
	:	:	
	:	:	
	:	:	
	Interrupt Vector 52	0x00007C	
	Interrupt Vector 53	0x00007E	
	Interrupt Vector 54	0x000080	
	:	:	
	:	:	
	:	:	
	Interrupt Vector 116	0x0000FC	
	Interrupt Vector 117	0x0000FE	
	Interrupt Vector 118	0x000100	
	Interrupt Vector 119	0x000102	
	Interrupt Vector 120	0x000104	
	:	:	
	:	:	
	:	:	
	Interrupt Vector 244	0x0001FC	
	Interrupt Vector 245	0x0001FE	
	START OF CODE	0x000200	

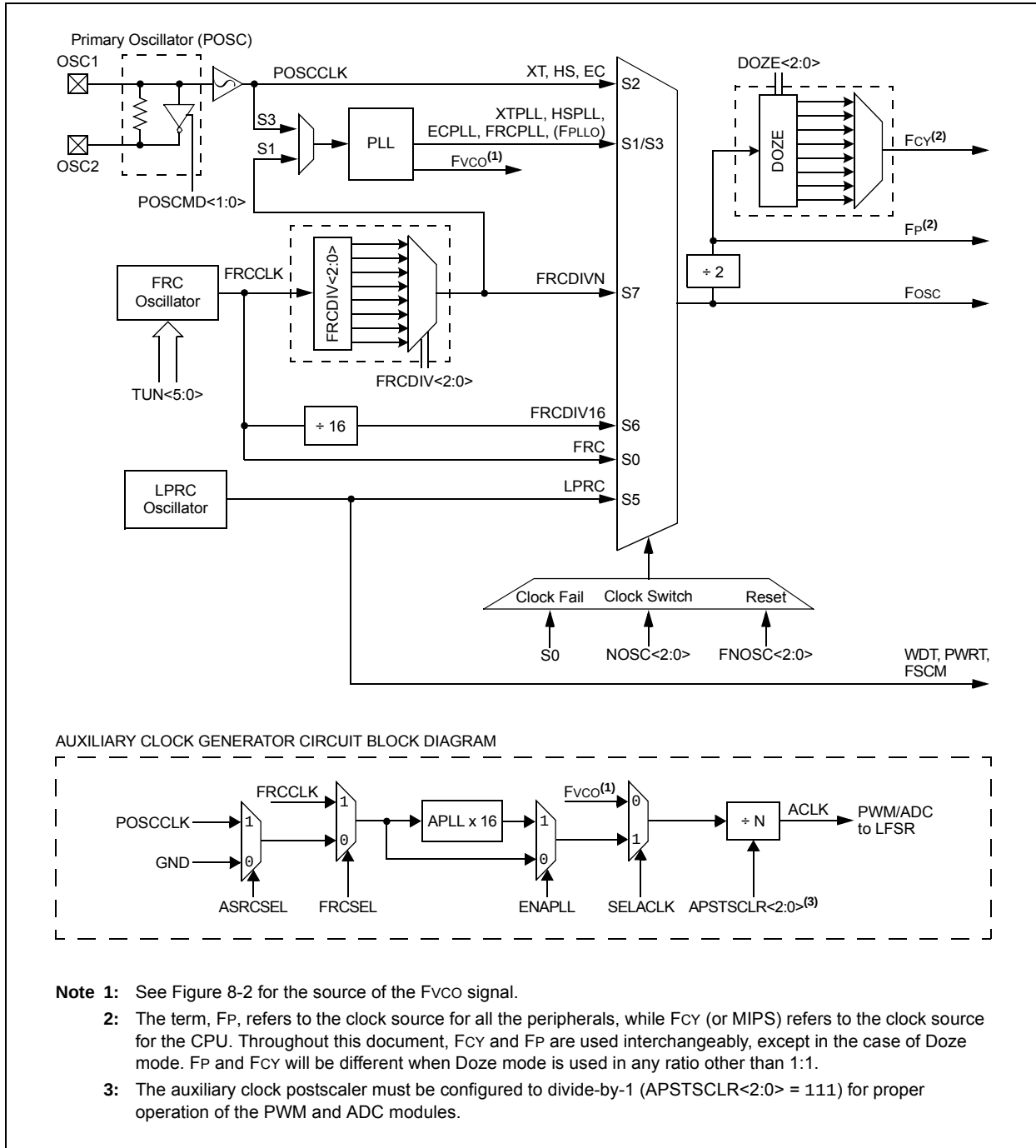
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TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Reserved	126-158	118-150	0x000100-0x000140	—	—	—
AN8 Conversion Done	159	151	0x000142	IFS9<7>	IEC9<7>	IPC37<14:12>
AN9 Conversion Done	160	152	0x000144	IFS9<8>	IEC9<8>	IPC38<2:0>
AN10 Conversion Done	161	153	0x000146	IFS9<9>	IEC9<9>	IPC38<6:4>
AN11 Conversion Done	162	154	0x000148	IFS9<10>	IEC9<10>	IPC38<10:8>
Reserved	163-164	155-156	0x00014A-0x00014C	—	—	—
AN14 Conversion Done	165	157	0x00014E	IFS9<13>	IEC9<13>	IPC39<6:4>
Reserved	163-180	155-172	0x00014A-0x00016C	—	—	—
I2C1 – I2C1 Bus Collision	181	173	0x00016E	IFS10<13>	IEC10<13>	IPC43<6:4>
Reserved	182-184	174-176	0x000170-0x000174	—	—	—
ADCMPO – ADC Digital Comparator 0	185	177	0x000176	IFS11<1>	IEC11<1>	IPC44<6:4>
ADCMPO – ADC Digital Comparator 1	186	178	0x000178	IFS11<2>	IEC11<2>	IPC44<10:8>
ADFL0 – ADC Filter 0	187	179	0x00017A	IFS11<3>	IEC11<3>	IPC44<14:12>
Reserved	188-253	180-245	0x00017C-0x0001FE	—	—	—

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FIGURE 8-1: OSCILLATOR SYSTEM DIAGRAM



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10.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-15). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

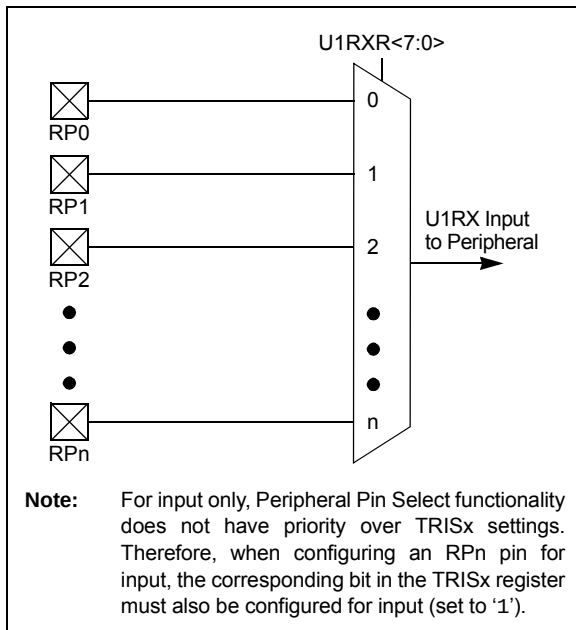
For example, Figure 10-2 illustrates remappable pin selection for the U1RX input.

10.4.4.1 Virtual Connections

The dsPIC33EPXXGS202 devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

FIGURE 10-2: REMAPPABLE INPUT FOR U1RX



dsPIC33EPXXGS202 FAMILY

6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:

- a) Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
- b) It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
- c) If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
- d) If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
- e) If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self-test.
- f) Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
- g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRISx setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRISx settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned.
- h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select (ANSELx) registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

10.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

10.6.1 KEY RESOURCES

- “I/O Ports” (DS70000598) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

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REGISTER 10-10: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK1INR7	SCK1INR6	SCK1INR5	SCK1INR4	SCK1INR3	SCK1INR2	SCK1INR1	SCK1INR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **SCK1INR<7:0>**: Assign SPI1 Clock Input (SCK1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•
•
•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **SDI1R<7:0>**: Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•
•
•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS202 FAMILY

REGISTER 12-2: T3CON: TIMER3 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL ⁽²⁾	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE ⁽¹⁾	TCKPS1 ⁽¹⁾	TCKPS0 ⁽¹⁾	—	—	TCS ⁽¹⁾	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TON:** Timer3 On bit⁽¹⁾
 1 = Starts 16-bit Timer3
 0 = Stops 16-bit Timer3
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timer3 Stop in Idle Mode bit⁽²⁾
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer3 Gated Time Accumulation Enable bit⁽¹⁾
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timer3 Input Clock Prescale Select bits⁽¹⁾
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer3 Clock Source Select bit⁽¹⁾
 1 = External clock is from pin, T3CK (on the rising edge)
 0 = Peripheral Clock (FP)
- bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timer3 operation; all timer functions are set through T2CON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timer2 Control register (T2CON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

dsPIC33EPXXGS202 FAMILY

14.2 Output Compare Control Registers

REGISTER 14-1: OC1CON1: OUTPUT COMPARE CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—
bit 15						bit 8	

R/W-0	U-0	U-0	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7						bit 0	

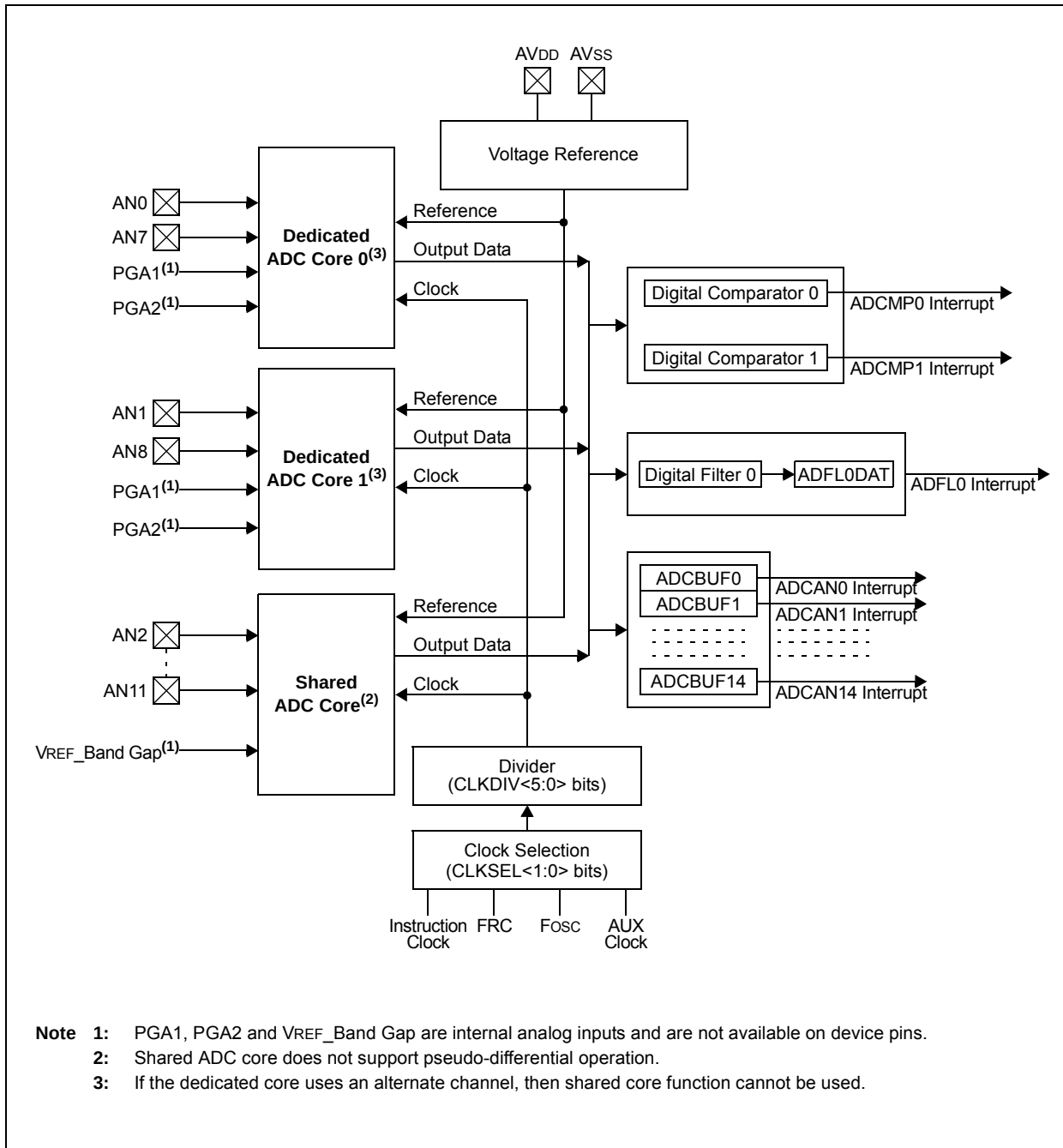
Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **OCSIDL:** Output Compare Stop in Idle Mode Control bit
 1 = Output compare halts in CPU Idle mode
 0 = Output compare continues to operate in CPU Idle mode
- bit 12-10 **OCTSEL<2:0>:** Output Compare Clock Select bits
 111 = Peripheral Clock (FP)
 110 = Reserved
 101 = Reserved
 100 = T1CLK is the clock source of the OC1 (only the synchronous clock is supported)
 011 = Reserved
 010 = Reserved
 001 = T3CLK is the clock source of the OC1
 000 = T2CLK is the clock source of the OC1
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **ENFLTA:** Fault A Input Enable bit
 1 = Output Compare Fault A input (OCFA) is enabled
 0 = Output Compare Fault A input (OCFA) is disabled
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **OCFLTA:** PWM Fault A Condition Status bit
 1 = PWM Fault A condition on the OCFA pin has occurred
 0 = No PWM Fault A condition on the OCFA pin has occurred
- bit 3 **TRIGMODE:** Trigger Status Mode Select bit
 1 = TRIGSTAT (OC1CON2<6>) is cleared when OC1RS = OC1TMR or in software
 0 = TRIGSTAT is cleared only by software

Note 1: OC1R and OC1RS are double-buffered in PWM mode only.

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FIGURE 19-1: ADC MODULE BLOCK DIAGRAM



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FIGURE 19-2: DEDICATED ADC CORE 0-1 BLOCK DIAGRAM

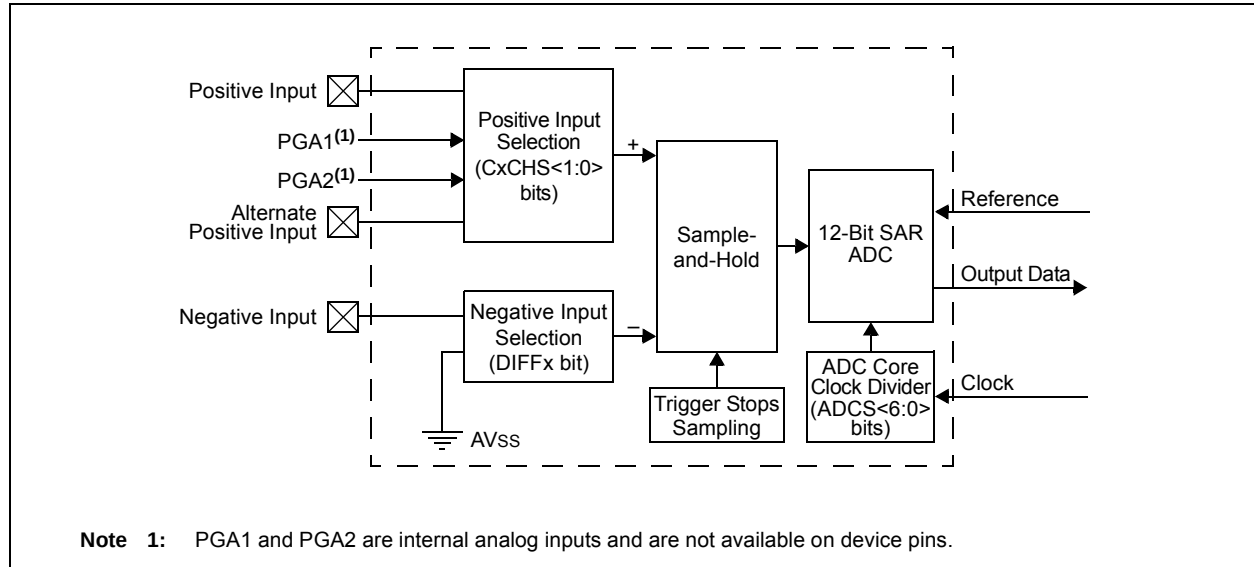
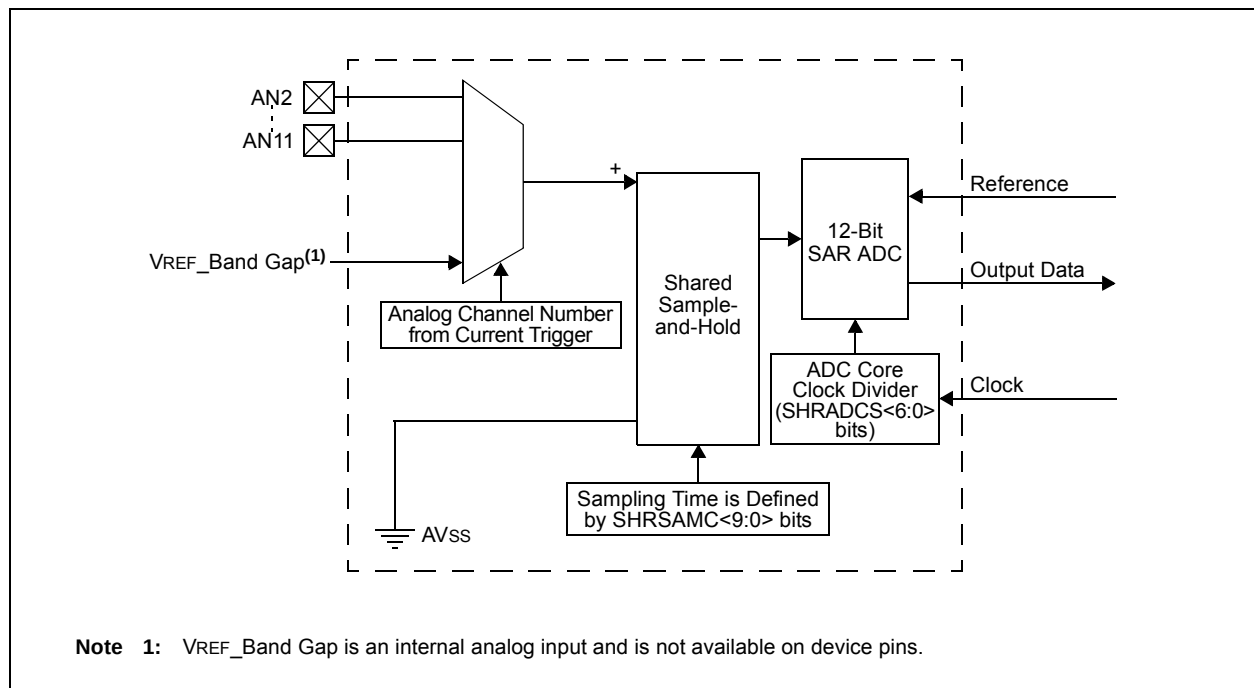


FIGURE 19-3: SHARED ADC CORE BLOCK DIAGRAM



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REGISTER 19-11: ADCORExL: DEDICATED ADC CORE x CONTROL REGISTER LOW (x = 0,1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SAMC<9:8>	
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMC<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SAMC<9:0>:** Dedicated ADC Core x Conversion Delay Selection bits

These bits determine the time between the trigger event and the start of conversion in the number of the ADC Core Clock (TADCORE) periods. During this time, the ADC Core x still continues sampling. This feature is enabled by the SAMCxEN bit in the ADCON4L register.

1111111111 = 1025 TADCORE

•

•

•

0000000001 = 3 TADCORE

0000000000 = 2 TADCORE

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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
47	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AwB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
48	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f, WREG	Move f to WREG	1	1	None
		MOV #lit16, Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8, Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV WREG, f	Move WREG to f	1	1	None
		MOV.D Wns, Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
49	MOVPAG	MOVPAG #lit10, DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit8, TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
50	MOVSAC	MOVSAC Acc, Wx, Wxd, Wy, Wyd, AwB	Prefetch and store accumulator	1	1	None
51	MPY	MPY Wm*Wn, Acc, Wx, Wxd, Wy, Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
52	MPY.N	MPY.N Wm*Wn, Acc, Wx, Wxd, Wy, Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
53	MSC	MSC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd, AwB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
54	MUL	MUL.SS Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb, Ws, Acc	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, Ws, Acc	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Acc	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb, Ws, Acc	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb, #lit5, Acc	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, Ws, Acc	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb, Ws, Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb, Ws, Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb, Ws, Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb, Ws, Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb, #lit5, Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

APPENDIX A: REVISION HISTORY

Revision A (January 2015)

This is the initial version of this document.

Revision B (May 2015)

Changes to Register 19-7 ADCON4L.

Changes to the hysteresis values in **Section 20.6 “Hysteresis”** and Register 20-1 CMPxCON.

A note has been added to Table 23-2 Instruction Set Overview.

Changes to **Section 25.0 “Electrical Characteristics”**.

New packaging diagrams have been added to **Section 27.0 “Packaging Information”**.

Minor text edits throughout document.

Revision C (November 2015)

Changes for this revision of the document have been effected in the following:

- Adds:
 - **Section 4.2 “Unique Device Identifier (UDID)”**
- Removes:
 - Table 4-21: JTAG Interface Register Map
- Updates and modifies:
 - Tables:
Table 4-3; Table 4-14; Table 4-17; Table 22-1;
Table 25-6; Table 25-8; Table 25-9; Table 25-13;
Table 25-42; Table 25-44; Table 25-45
 - Figures:
Figure 19-1; Figure 19-2; Figure 19-3
 - Registers:
Register 19-16; Register 19-22; Register 19-23
- Replaces:
 - Register 19-20
 - Three revised drawings of 28-Lead Ultra Thin Plastic Quad Flat (M6) 4x4x0.6 mm Body in **Section 27.0 “Packaging Information”**

Revision D (May 2016)

This revision of the document:

- Adds a new chapter **Section 26.0 “DC and AC Device Characteristics Graphs”**
- Updates Table 25-2 and Register 19-23
- Modifies the **“Qualification and Class B Support”** section
- Provides the family device number in **Section 4.2 “Unique Device Identifier (UDID)”**
- Wherever applicable, changes occurrences of PWMx to PWM

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