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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs202t-e-so

dsPIC33EPXXGS202 FAMILY

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT ⁽¹⁾	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency
0 = Fixed exception processing latency
- bit 14 **Unimplemented:** Read as '0'
- bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed
- bit 11 **EDT:** Early DO Loop Termination Control bit⁽¹⁾
1 = Terminates executing DO loop at the end of current loop iteration
0 = No effect
- bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active
- bit 7 **SATA:** ACCA Saturation Enable bit
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled
- bit 6 **SATB:** ACCB Saturation Enable bit
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled
- bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled
- bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)
- bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: This bit is always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-11: I2C1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1CONL	0200	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CONH	0202	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C1STAT	0204	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	0206	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	0208	—	—	—	—	—	—	I2C1 Address Mask Register										0000
I2C1BRG	020A	Baud Rate Generator Register																0000
I2C1TRN	020C	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1RCV	020E	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: UART1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler Register																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: SPI1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-15: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP33R5	RP33R4	RP33R3	RP33R2	RP33R1	RP33R0	—	—	RP32R5	RP32R4	RP32R3	RP32R2	RP32R1	RP32R0	0000
RPOR1	0672	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP34R5	RP34R4	RP34R3	RP34R2	RP34R1	RP34R0	0000
RPOR2	0674	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR3	0676	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR4	0678	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR5	067A	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR6	067C	—	—	RP45R5	RP45R4	RP45R3	RP45R2	RP45R1	RP45R0	—	—	RP44R5	RP44R4	RP44R3	RP44R2	RP44R1	RP44R0	0000
RPOR7	067E	—	—	RP47R5	RP47R4	RP47R3	RP47R2	RP47R1	RP47R0	—	—	RP46R5	RP46R4	RP46R3	RP46R2	RP46R1	RP46R0	0000
RPOR8	0680	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0	0000
RPOR9	0682	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	0000
RPOR10	0684	—	—	RP181R5	RP181R4	RP181R3	RP181R2	RP181R1	RP181R0	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-16: PERIPHERAL PIN SELECT INPUT REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	INT1R<7:0>									—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	INT2R<7:0>								0000
RPINR2	06A4	T1CKR<7:0>									—	—	—	—	—	—	—	0000
RPINR3	06A6	T3CKR7	T3CKR6	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0	T2CKR7	T2CKR6	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0	0000
RPINR7	06AE	—	—	—	—	—	—	—	—	IC1R<7:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	OCFAR<7:0>								0000
RPINR12	06B8	FLT2R7	FLT2R6	FLT2R5	FLT2R4	FLT2R3	FLT2R2	FLT2R1	FLT2R0	FLT1R7	FLT1R6	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0	0000
RPINR13	06BA	FLT4R7	FLT4R6	FLT4R5	FLT4R4	FLT4R3	FLT4R2	FLT4R1	FLT4R0	FLT3R7	FLT3R6	FLT3R5	FLT3R4	FLT3R3	FLT3R2	FLT3R1	FLT3R0	0000
RPINR18	06C4	U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTS0	U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0	0000
RPINR20	06C8	SCK1INR7	SCK1INR6	SCK1INR5	SCK1INR4	SCK1INR3	SCK1INR2	SCK1INR1	SCK1INR0	SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0	0000
RPINR21	06CA	—	—	—	—	—	—	—	—	SS1R<7:0>								0000
RPINR37	06EA	SYNCl1R<7:0>									—	—	—	—	—	—	—	0000
RPINR38	06EC	—	—	—	—	—	—	—	—	SYNCl2R<7:0>								0000
RPINR42	06F4	FLT6R7	FLT6R6	FLT6R5	FLT6R4	FLT6R3	FLT6R2	FLT6R1	FLT6R0	FLT5R7	FLT5R6	FLT5R5	FLT5R4	FLT5R3	FLT5R2	FLT5R1	FLT5R0	0000
RPINR43	06F6	FLT8R7	FLT8R6	FLT8R5	FLT8R4	FLT8R3	FLT8R2	FLT8R1	FLT8R0	FLT7R7	FLT7R6	FLT7R5	FLT7R4	FLT7R3	FLT7R2	FLT7R1	FLT7R0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 4	Unimplemented: Read as '0'
bit 3	CF: Clock Fail Detect bit ⁽³⁾ 1 = FSCM has detected a clock failure 0 = FSCM has not detected a clock failure
bit 2-1	Unimplemented: Read as '0'
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence.
- 2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
- 3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

10.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “I/O Ports” (DS70000598) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally, a Parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral’s output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port

has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through”, in which a port’s digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

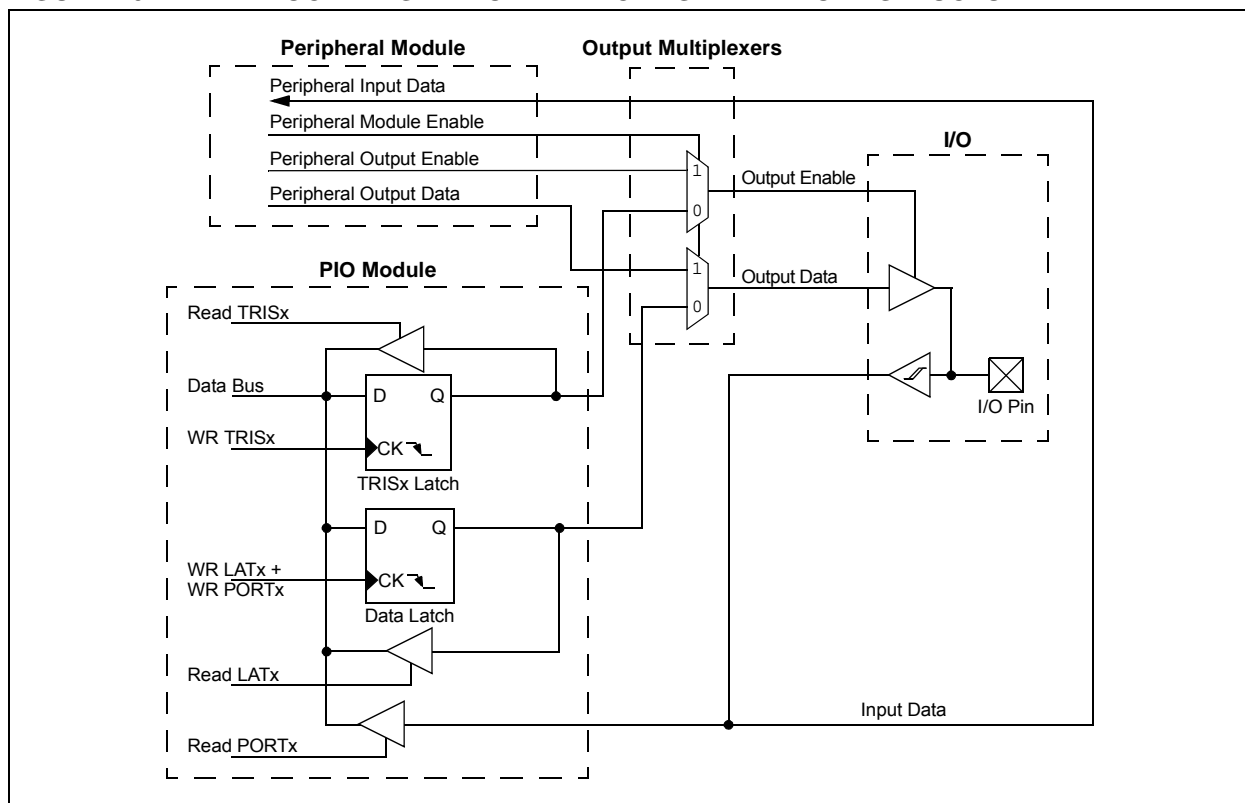
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means the corresponding LATx and TRISx registers, and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



10.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 25-11 under “Injection Current”, have internal protection diodes to VDD and VSS. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘0’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a ‘0’.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to $\sim(VDD - 0.8)$, not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristics specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the Absolute Maximum Ratings in **Section 25.0 “Electrical Characteristics”** of this data sheet. For example:

$$VOH = 2.4V @ IOH = -8 mA \text{ and } VDD = 3.3V$$

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted.

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REGISTER 10-4: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T3CKR7	T3CKR6	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2CKR7	T2CKR6	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **T3CKR<7:0>**: Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

0000001 = Input tied to RP1

0000000 = Input tied to Vss

bit 7-0 **T2CKR<7:0>**: Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS202 FAMILY

REGISTER 10-20: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits
(see Table 10-2 for peripheral function numbers)
bit 7-6 **Unimplemented:** Read as '0'
bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits
(see Table 10-2 for peripheral function numbers)

REGISTER 10-21: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits
(see Table 10-2 for peripheral function numbers)
bit 7-6 **Unimplemented:** Read as '0'
bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits
(see Table 10-2 for peripheral function numbers)

14.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **“Output Compare with Dedicated Timer”** (DS70005159) in the *“dsPIC33/PIC24 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of four available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a

single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

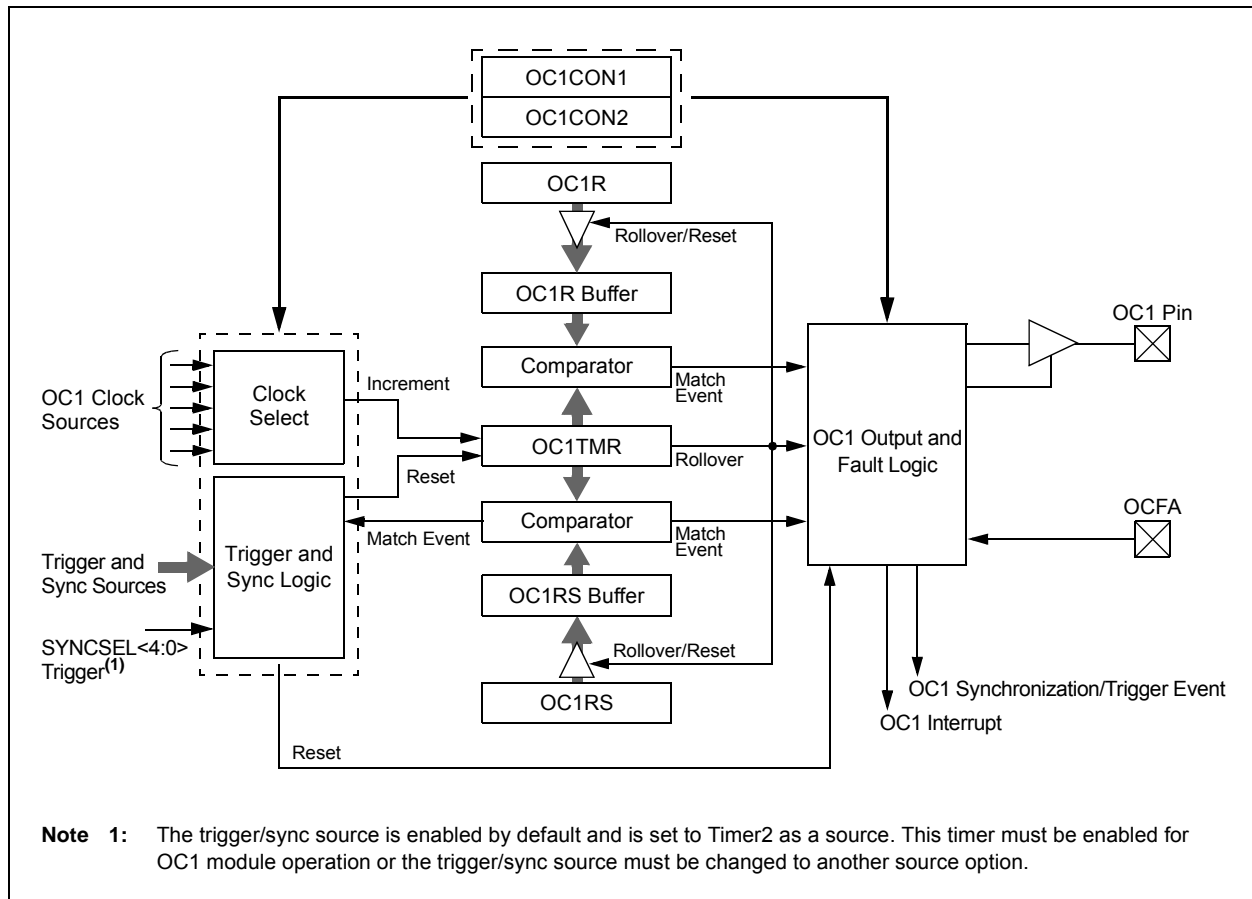
14.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

14.1.1 KEY RESOURCES

- **“Output Compare with Dedicated Timer”** (DS70005159) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

FIGURE 14-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



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REGISTER 14-2: OC1CON2: OUTPUT COMPARE CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	—
bit 15				bit 8			

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7				bit 0			

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **FLTMD:** Fault Mode Select bit
1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTA bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts
- bit 14 **FLTOUT:** Fault Out bit
1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault
- bit 13 **FLTTRIEN:** Fault Output State Select bit
1 = OC1 pin is tri-stated on a Fault condition
0 = OC1 pin I/O state is defined by the FLTOUT bit on a Fault condition
- bit 12 **OCINV:** Output Compare Invert bit
1 = OC1 output is inverted
0 = OC1 output is not inverted
- bit 11-8 **Unimplemented:** Read as '0'
- bit 7 **OCTRIG:** Output Compare Trigger/Sync Select bit
1 = Triggers OC1 from the source designated by the SYNCSEL<4:0> bits
0 = Synchronizes OC1 with the source designated by the SYNCSEL<4:0> bits
- bit 6 **TRIGSTAT:** Timer Trigger Status bit
1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear
- bit 5 **OCTRIS:** Output Compare Output Pin Direction Select bit
1 = Output compare is tri-stated
0 = Output compare module drives the OCx pin

Note 1: This option should only be selected as a trigger source and not as a synchronization source.

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REGISTER 19-11: ADCORExL: DEDICATED ADC CORE x CONTROL REGISTER LOW (x = 0,1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SAMC<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMC<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SAMC<9:0>:** Dedicated ADC Core x Conversion Delay Selection bits

These bits determine the time between the trigger event and the start of conversion in the number of the ADC Core Clock (TADCORE) periods. During this time, the ADC Core x still continues sampling. This feature is enabled by the SAMCxEN bit in the ADCON4L register.

1111111111 = 1025 TADCORE

•
•
•

0000000001 = 3 TADCORE

0000000000 = 2 TADCORE

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REGISTER 19-13: ADLVLTRGL: ADC LEVEL-SENSITIVE TRIGGER CONTROL REGISTER LOW

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	LVLEN14	—	—	LVLEN<11:8>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LVLEN<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **LVLEN14:** Level Trigger 14 Enable bit
1 = Input Channel 14 trigger is level-sensitive
0 = Input Channel 14 trigger is edge-sensitive

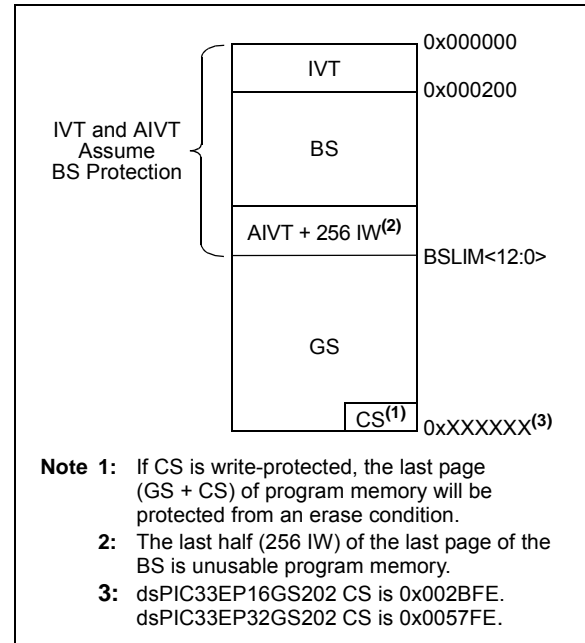
bit 13-12 **Unimplemented:** Read as '0'

bit 11-0 **LVLEN<11:0>:** Level Trigger x Enable bits
1 = Input Channel x trigger is level-sensitive
0 = Input Channel x trigger is edge-sensitive

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The different device security segments are shown in Figure 22-3. Here, all three segments are shown but are not required. If only basic code protection is required, then the GS can be enabled independently or combined with the CS if desired.

FIGURE 22-3: dsPIC33EPXXGS202 SECURITY SEGMENTS EXAMPLE



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TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
47	MAC	MAC $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd, AWB$	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd$	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
48	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV $f, WREG$	Move f to WREG	1	1	None
		MOV $\#lit16, Wn$	Move 16-bit literal to Wn	1	1	None
		MOV.b $\#lit8, Wn$	Move 8-bit literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV $WREG, f$	Move WREG to f	1	1	None
		MOV.D Wns, Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
49	MOVPAG	MOVPAG $\#lit10, DSRPAG$	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG $\#lit8, TBLPAG$	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW $Ws, DSRPAG$	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW $Ws, TBLPAG$	Move Ws<7:0> to TBLPAG	1	1	None
50	MOVSAC	MOVSAC $Acc, Wx, Wxd, Wy, Wyd, AWB$	Prefetch and store accumulator	1	1	None
51	MPY	MPY $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd$	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd$	Square Wm to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
52	MPY.N	MPY.N $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd$	-(Multiply Wm by Wn) to Accumulator	1	1	None
53	MSC	MSC $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd, AWB$	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
54	MUL	MUL.SS Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{signed}(Wb) * \text{signed}(Ws)$	1	1	None
		MUL.SS Wb, Ws, Acc	Accumulator = $\text{signed}(Wb) * \text{signed}(Ws)$	1	1	None
		MUL.SU Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{signed}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MUL.SU Wb, Ws, Acc	Accumulator = $\text{signed}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MUL.SU $Wb, \#lit5, Acc$	Accumulator = $\text{signed}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL.US Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{unsigned}(Wb) * \text{signed}(Ws)$	1	1	None
		MUL.US Wb, Ws, Acc	Accumulator = $\text{unsigned}(Wb) * \text{signed}(Ws)$	1	1	None
		MUL.UU Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{unsigned}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MUL.UU $Wb, \#lit5, Acc$	Accumulator = $\text{unsigned}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL.UU Wb, Ws, Acc	Accumulator = $\text{unsigned}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MULW.SS Wb, Ws, Wnd	$Wnd = \text{signed}(Wb) * \text{signed}(Ws)$	1	1	None
		MULW.SU Wb, Ws, Wnd	$Wnd = \text{signed}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MULW.US Wb, Ws, Wnd	$Wnd = \text{unsigned}(Wb) * \text{signed}(Ws)$	1	1	None
		MULW.UU Wb, Ws, Wnd	$Wnd = \text{unsigned}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MUL.SU $Wb, \#lit5, Wnd$	$\{Wnd + 1, Wnd\} = \text{signed}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL.SU $Wb, \#lit5, Wnd$	$Wnd = \text{signed}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL.UU $Wb, \#lit5, Wnd$	$\{Wnd + 1, Wnd\} = \text{unsigned}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL.UU $Wb, \#lit5, Wnd$	$Wnd = \text{unsigned}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL f	$W3:W2 = f * WREG$	1	1	None

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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24.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

24.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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TABLE 25-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DI10	V _{IL}	Input Low Voltage Any I/O Pin and MCLR	V _{SS}	—	0.2 V _{DD}	V	
DI18		I/O Pins with SDA1, SCL1	V _{SS}	—	0.3 V _{DD}	V	SMBus disabled
DI19		I/O Pins with SDA1, SCL1	V _{SS}	—	0.8	V	SMBus enabled
DI20	V _{IH}	Input High Voltage I/O Pins Not 5V Tolerant ⁽⁴⁾	0.8 V _{DD}	—	V _{DD}	V	
		I/O Pins 5V Tolerant and MCLR ⁽⁴⁾	0.8 V _{DD}	—	5.5	V	
		5V Tolerant I/O Pins with SDA1, SCL1 ⁽⁴⁾	0.8 V _{DD}	—	5.5	V	SMBus disabled
		5V I/O Pins with SDA1, SCL1 ⁽⁴⁾	2.1	—	5.5	V	SMBus enabled
		I/O Pins with SDA1, SCL1 Not 5V Tolerant ⁽⁴⁾	0.8 V _{DD}	—	V _{DD}	V	SMBus disabled
		I/O Pins with SDA1, SCL1 Not 5V Tolerant ⁽⁴⁾	2.1	—	V _{DD}	V	SMBus enabled
DI30	ICNPU	Input Change Notification Pull-up Current	50	250	600	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS}
DI31	ICNPD	Input Change Notification Pull-Down Current⁽⁵⁾	—	50	—	μA	V _{DD} = 3.3V, V _{PIN} = V _{DD}

- Note 1:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 5:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- 6:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 7:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 8:** |Injection Currents| > 0 can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

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FIGURE 25-2: EXTERNAL CLOCK TIMING

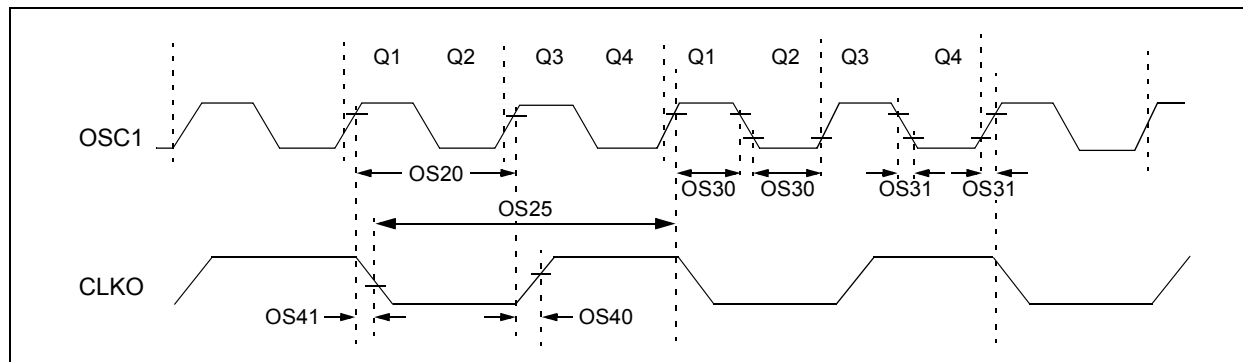


TABLE 25-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 40	MHz MHz	XT HS
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C
OS25	Tcy	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

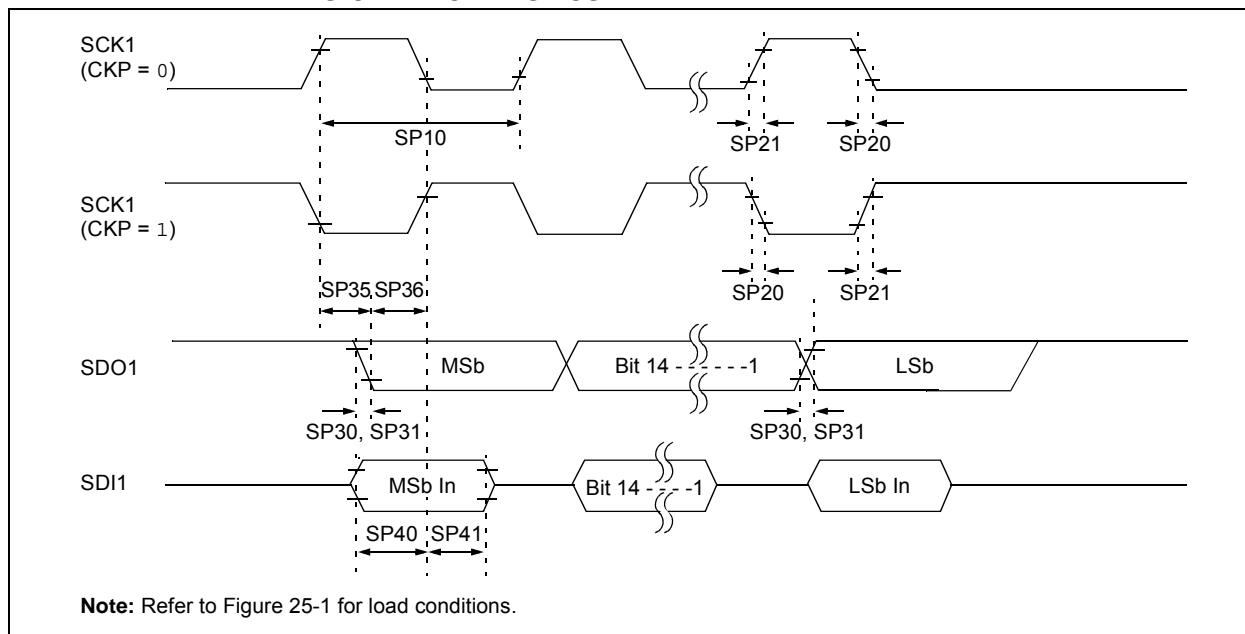
2: Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: Parameters are for design guidance only and are not tested in manufacturing.

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**FIGURE 25-14: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING CHARACTERISTICS**



**TABLE 25-34: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid After SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 25-21: I2C1 BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

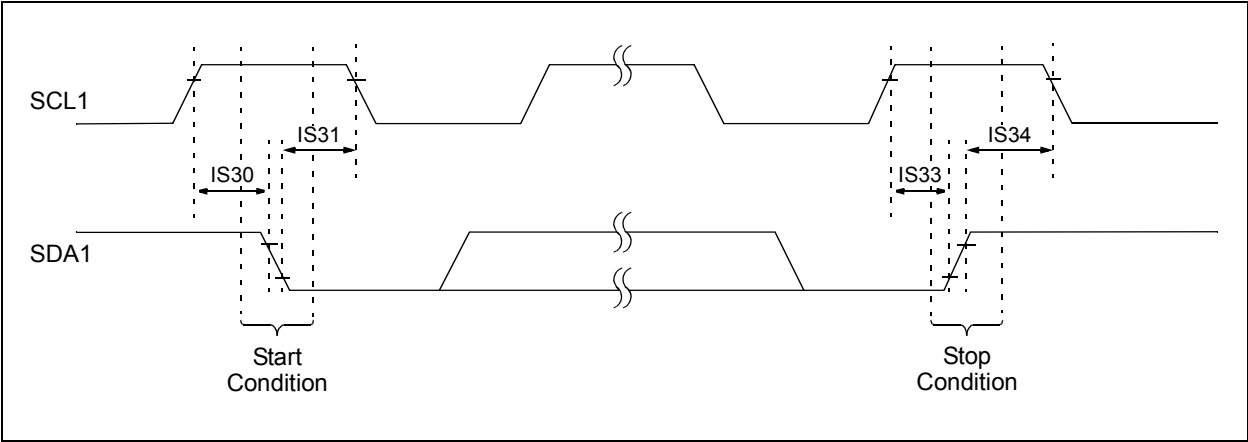
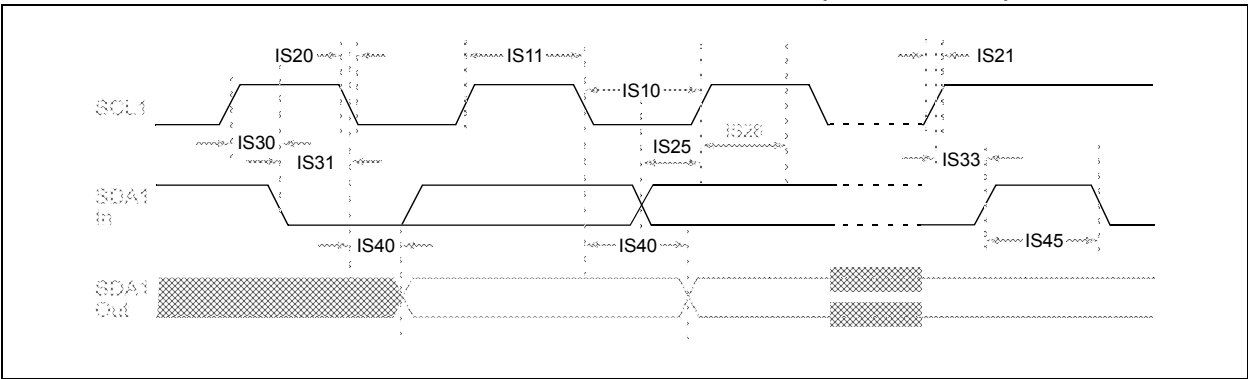


FIGURE 25-22: I2C1 BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



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