Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs202t-e-ss

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXGS202 family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins
  regardless if ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins
  used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins
  when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.6.1 KEY RESOURCES

- **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

4.5 Special Function Register Maps

TABLE 4-2: CPU CORE REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																xxxx
W1	0002	W1																xxxx
W2	0004	W2																xxxx
W3	0006	W3																xxxx
W4	0008	W4																xxxx
W5	000A	W5																xxxx
W6	000C	W6																xxxx
W7	000E	W7																xxxx
W8	0010	W8																xxxx
W9	0012	W9																xxxx
W10	0014	W10																xxxx
W11	0016	W11																xxxx
W12	0018	W12																xxxx
W13	001A	W13																xxxx
W14	001C	W14																xxxx
W15	001E	W15																xxxx
SPLIM	0020	SPLIM																0000
ACCAL	0022	ACCAL																0000
ACCAH	0024	ACCAH																0000
ACCAU	0026	Sign Extension of ACCA<39>								ACCAU								0000
ACCBL	0028	ACCBL																0000
ACCBH	002A	ACCBH																0000
ACCBU	002C	Sign Extension of ACCB<39>								ACCBU								0000
PCL	002E	PCL<15:1>															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000
DSRPAG	0032	—	—	—	—	—	—	Extended Data Space (EDS) Read Page Register (DSRPAG<9:0>)										0001
DSWPAG(1)	0034	—	—	—	—	—	—	—	Extended Data Space (EDS) Write Page Register (DSWPAG8:0>)(1)									0001
RCOUNT	0036	RCOUNT<15:0>																0000
DCOUNT	0038	DO Loop Counter Register (DCOUNT<15:0>)																0000
DOSTARTL	003A	DO Loop Start Address Register Low (DOSTARTL<15:1>)															—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DO Loop Start Address Register High (DOSTARTH<5:0>)						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: The contents of this register should never be modified. The DSWPAG must always point to the first page.

REGISTER 9-5: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CMP2MD	CMP1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PGA1MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **CMP2MD:** Comparator Channel 2 (CMP2) Module Disable bit
1 = CMP2 module is disabled
0 = CMP2 module is enabled

bit 8 **CMP1MD:** Comparator Channel 1 (CMP1) Module Disable bit
1 = CMP1 module is disabled
0 = CMP1 module is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **PGA1MD:** PGA1 Module Disable bit
1 = PGA1 module is disabled
0 = PGA1 module is enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 9-6: PMD8: PERIPHERAL MODULE DISABLE CONTROL REGISTER 8

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	PGA2MD	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PGA2MD:** PGA2 Module Disable bit
1 = PGA2 module is disabled
0 = PGA2 module is enabled

bit 9-0 **Unimplemented:** Read as '0'

REGISTER 10-11: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SS1R<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **SS1R<7:0>:** Assign SPI1 Slave Select ($\overline{SS1}$) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

REGISTER 10-12: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCI1R<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **SYNCI1R<7:0>:** Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as ‘0’

11.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

11.1.1 KEY RESOURCES

- **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)

bit 3-0 **SEVTPS<3:0>:** PWM Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 Postscaler generates a Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 Postscaler generates a Special Event Trigger on every second compare match event
0000 = 1:1 Postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 15-2: PTCON2: PWM CLOCK DIVIDER SELECT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits(1)
111 = Reserved
110 = Divide-by-64, maximum PWM timing resolution
101 = Divide-by-32, maximum PWM timing resolution
100 = Divide-by-16, maximum PWM timing resolution
011 = Divide-by-8, maximum PWM timing resolution
010 = Divide-by-4, maximum PWM timing resolution
001 = Divide-by-2, maximum PWM timing resolution
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 19-3: ADCON2L: ADC CONTROL REGISTER 2 LOW

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
REFCIE	REFERCIE(2)	—	EIEN	—	SHREISEL2(1)	SHREISEL1(1)	SHREISEL0(1)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SHRADCS6	SHRADCS5	SHRADCS4	SHRADCS3	SHRADCS2	SHRADCS1	SHRADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **REFCIE:** Band Gap and Reference Voltage Ready Common Interrupt Enable bit
1 = Common interrupt will be generated when the band gap will become ready
0 = Common interrupt is disabled for the band gap ready event

bit 14 **REFERCIE:** Band Gap or Reference Voltage Error Common Interrupt Enable bit(2)
1 = Common interrupt will be generated when the band gap or reference voltage error is detected
0 = Common interrupt is disabled for the band gap and reference voltage error event

bit 13 **Unimplemented:** Read as '0'

bit 12 **EIEN:** Early Interrupts Enable bit
1 = The early interrupt feature is enabled for the input channels interrupts (when EISTATx flag is set)
0 = The individual interrupts are generated when conversion is done (when ANxRDY flag is set)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SHREISEL<2:0>:** Shared Core Early Interrupt Time Selection bits(1)
111 = Early interrupt is set and interrupt is generated 8 TADCORE clocks prior to when the data is ready
110 = Early interrupt is set and interrupt is generated 7 TADCORE clocks prior to when the data is ready
101 = Early interrupt is set and interrupt is generated 6 TADCORE clocks prior to when the data is ready
100 = Early interrupt is set and interrupt is generated 5 TADCORE clocks prior to when the data is ready
011 = Early interrupt is set and interrupt is generated 4 TADCORE clocks prior to when the data is ready
010 = Early interrupt is set and interrupt is generated 3 TADCORE clocks prior to when the data is ready
001 = Early interrupt is set and interrupt is generated 2 TADCORE clocks prior to when the data is ready
000 = Early interrupt is set and interrupt is generated 1 TADCORE clock prior to when the data is ready

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SHRADCS<6:0>:** Shared ADC Core Input Clock Divider bits
These bits determine the number of TCORESRC (Core Source Clock) periods for one shared TADCORE (ADC Core Clock) period.
1111111 = 254 Core Source Clock periods
•
•
•
0000011 = 6 Core Source Clock periods
0000010 = 4 Core Source Clock periods
0000001 = 2 Core Source Clock periods
0000000 = 2 Core Source Clock periods

Note 1: For the 6-bit shared ADC core resolution (SHRRES<1:0> = 00), the SHREISEL<2:0> settings, from '100' to '111', are not valid and should not be used. For the 8-bit shared ADC core resolution (SHRRES<1:0> = 01), the SHREISEL<2:0> settings, '110' and '111', are not valid and should not be used.

2: To avoid false interrupts, the REFERCIE bit must be set only after the module is enabled (ADON = 1).

REGISTER 19-20: ADTRIGxL: ADC CHANNEL TRIGGER x SELECTION REGISTER LOW (x = 0 to 3)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(4x+1)<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(4x)<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(4x+1)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Reserved
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = Reserved
10010 = Reserved
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = Reserved
01000 = Reserved
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

NOTES:

TABLE 25-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(1) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	3.0	—	3.6	V	
DC12	VDR	**RAM Data Retention Voltage(2)**	1.8	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0V-3V in 3 ms

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, PGAs and comparators) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 25-13 for the minimum and maximum BOR values.

2: This is the limit to which VDD may be lowered without losing RAM data.

TABLE 25-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
	CEFC	External Filter Capacitor Value(1)	4.7	10	—	μF	Capacitor must have a low series resistance (<1 Ohm)

Note 1: Typical VCAP Voltage = 1.8V when VDD ≥ VDDMIN.

TABLE 25-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins(3)	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	**Output High Voltage** 4x Source Driver Pins(2)	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins(3)	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	**Output High Voltage** 4x Source Driver Pins(2)	1.5	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -12 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins(3)	1.5	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -18 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Includes RB<14:11> pins.

3: Includes all I/O pins that are not 4x driver pins (see **Note 2**).

TABLE 25-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.(2)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD **(Notes 2, 3)**

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, PGAs and comparators) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

FIGURE 25-18: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

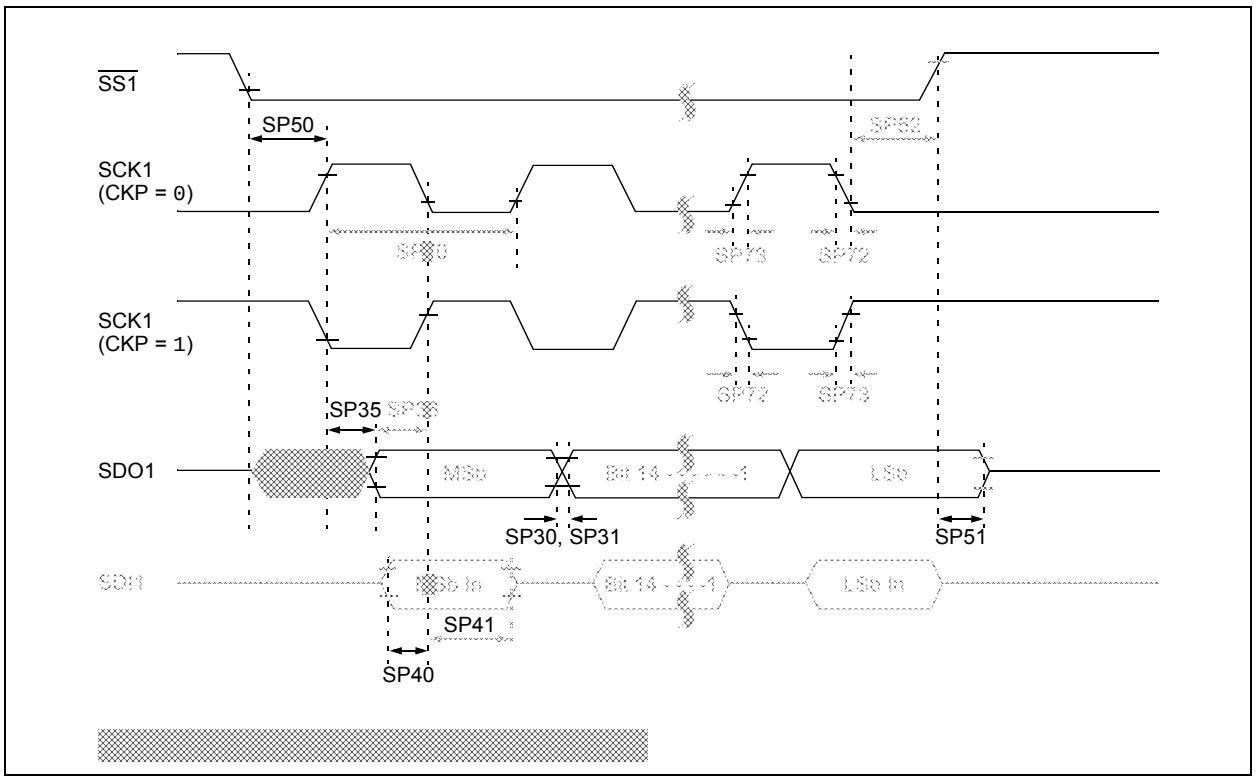


TABLE 25-38: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	11	MHz	**(Note 3)**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid After SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ After SCK1 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 25-42: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[4] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics[3]**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy: Single-Ended Input							
AD20b	Nr	Resolution	12			bits	
AD21b	INL	Integral Nonlinearity	> -4	—	< 4	LSb	AVSS = 0V, AVDD = 3.3V
AD22b	DNL	Pseudo-Differential Nonlinearity	> -1	—	< 1.5	LSb	AVSS = 0V, AVDD = 3.3V **(Note 5)**
AD23b	GERR	Gain Error (Dedicated Core)	> -5	—	< 5	LSb	AVSS = 0V, AVDD = 3.3V
		Gain Error (Shared Core)	> -5	—	< 5	LSb	AVSS = 0V, AVDD = 3.3V, -40°C < TA ≤ +85°C
			> -6	—	< 6	LSb	AVSS = 0V, AVDD = 3.3V, -85°C < TA ≤ +125°C
AD24b	EOFF	Offset Error (Dedicated Core)	0	7	< 12	LSb	AVSS = 0V, AVDD = 3.3V
		Offset Error (Shared Core)	0	7	< 12	LSb	
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal-to-Noise and Distortion	63	—	> 65	dB	**(Notes 2, 3)**
AD34b	ENOB	Effective Number of bits	10.3	—	—	bits	**(Notes 2, 3)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

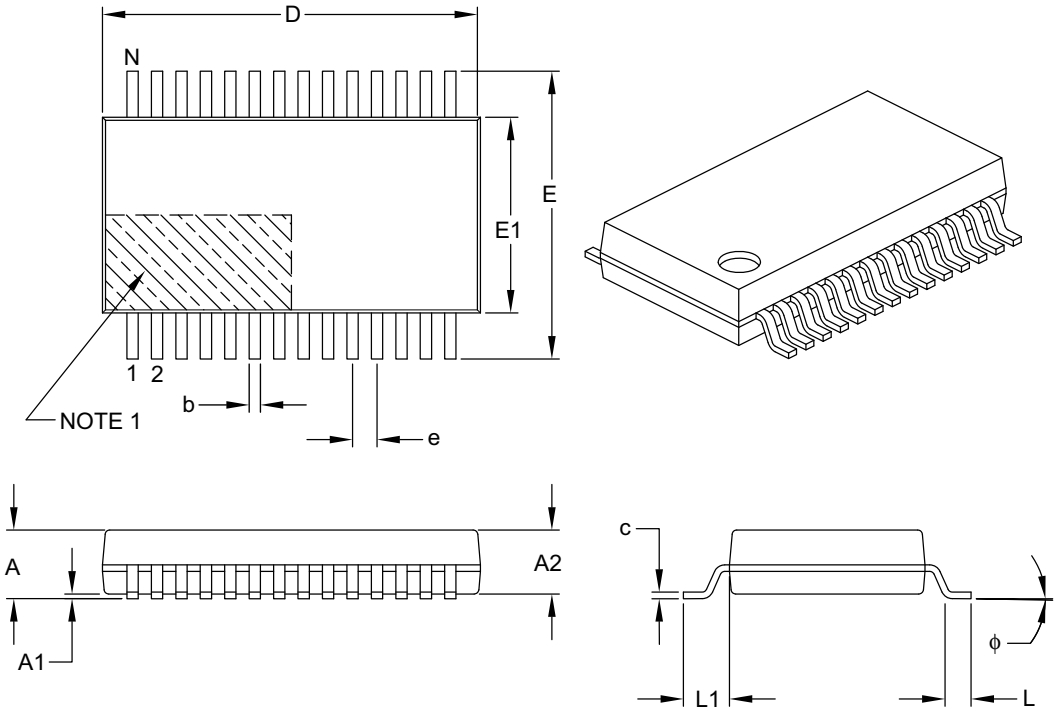
4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

5: No missing codes, limits are based on the characterization results.

27.2 Package Details

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

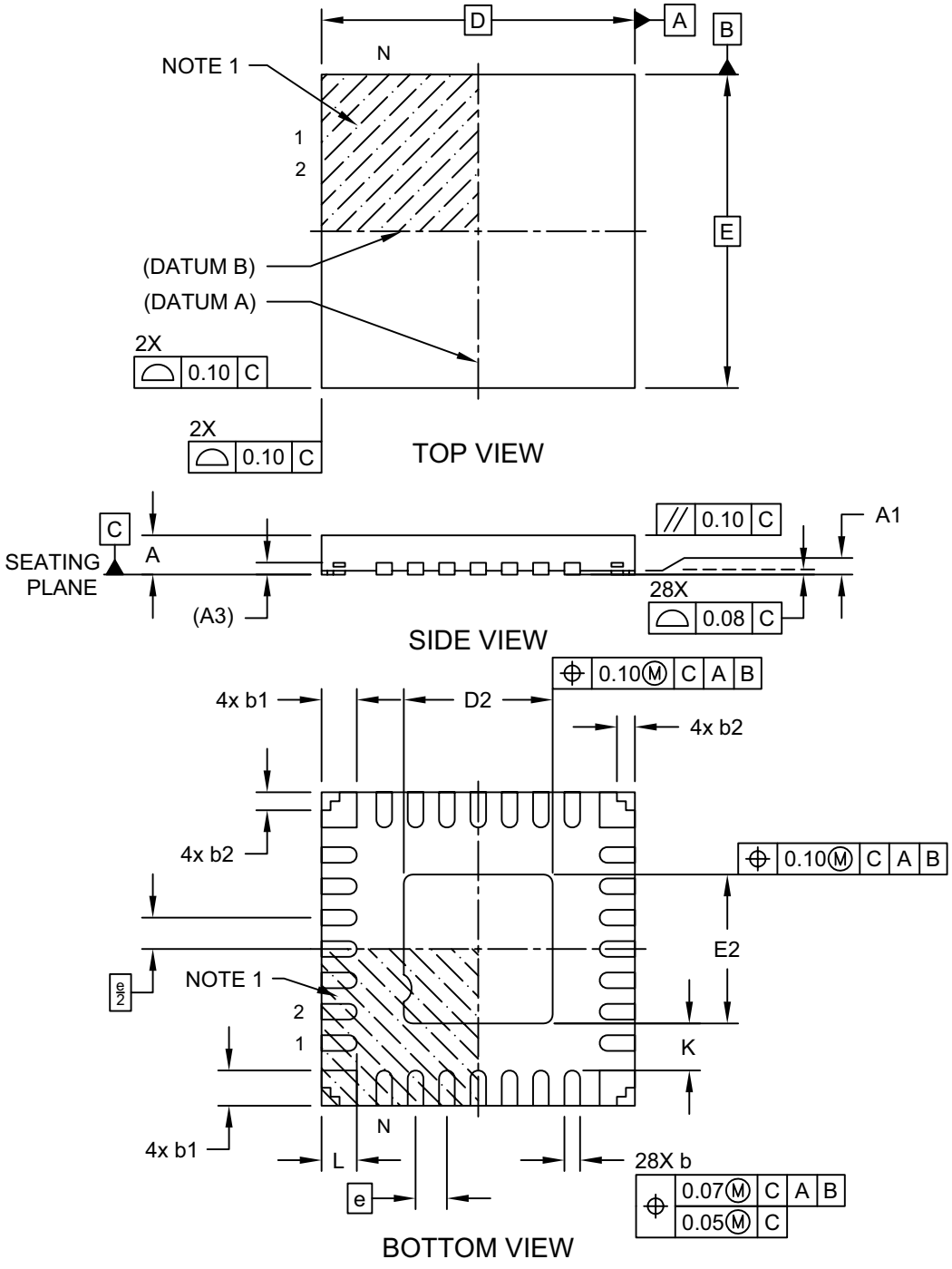
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

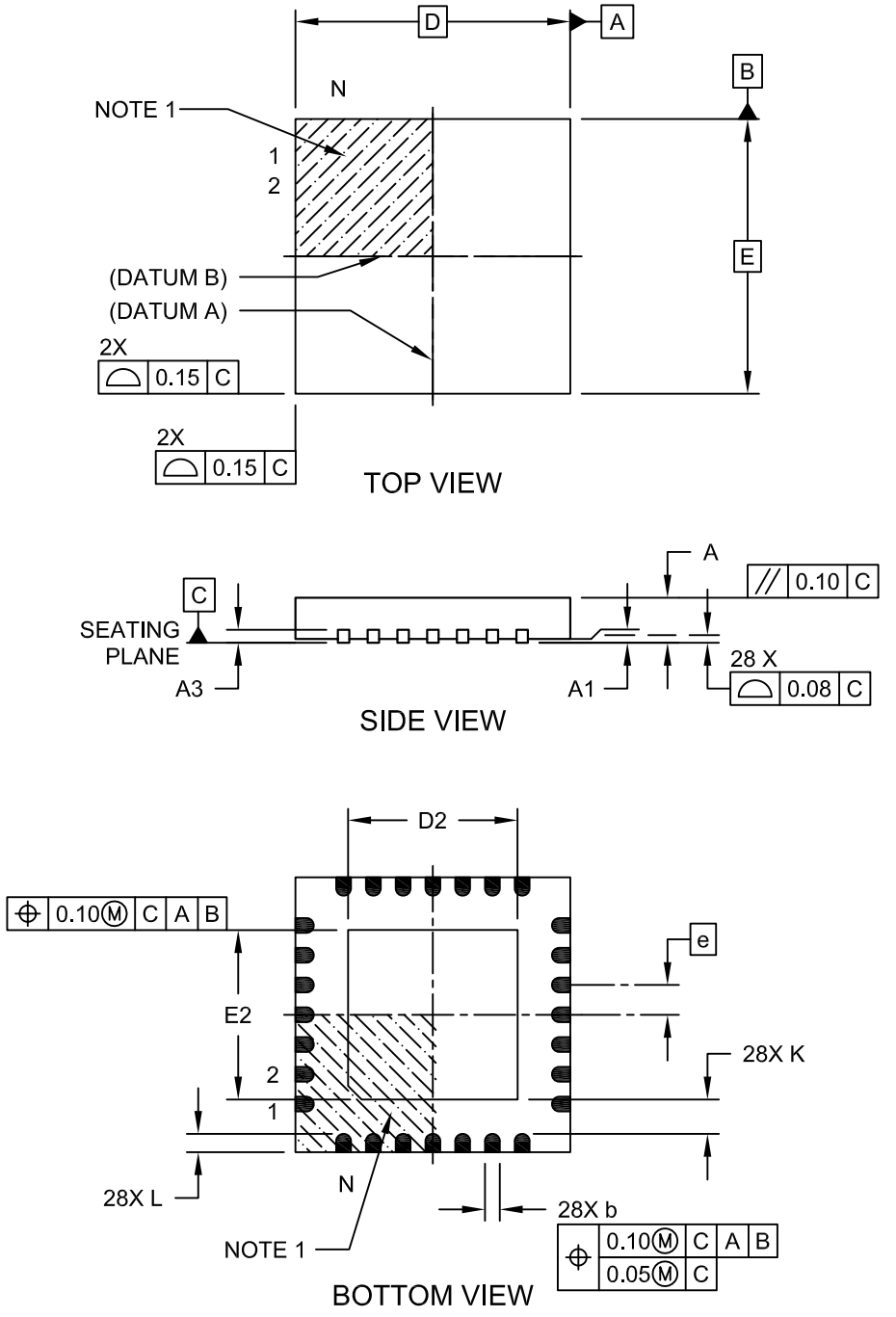
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S]
With 0.40 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-124C Sheet 1 of 2

SR (CPU STATUS) 22, 79
SSEVTCMP (PWM Secondary Special Event Compare) 160
STCON (PWM Secondary Master Time Base Control) 158
STCON2 (PWM Secondary Clock Divider Select 2) 159
STPER (PWM Secondary Master Time Base Period) 159
STRIGx (PWMx Secondary Trigger Compare Value) 172
T1CON (Timer1 Control) 135
T2CON (Timer2 Control) 139
T3CON (Timer3 Control) 140
TRGCONx (PWMx Trigger Control) 168
TRIGx (PWMx Primary Trigger Compare Value) 170
U1MODE (UART1 Mode) 195
U1STA (UART1 Status and Control) 197
Resets 69
Brown-out Reset (BOR) 69
Configuration Mismatch Reset (CM) 69
Illegal Condition Reset (IOPUWR) 69
Illegal Opcode 69
Security 69
Uninitialized W Register 69
Master Clear ($\overline{MCLR}$) Pin Reset 69
Power-on Reset (POR) 69
RESET Instruction (SWR) 69
Resources 70
Trap Conflict Reset (TRAPR) 69
Watchdog Timer Time-out Reset (WDTO) 69
Revision History 331

S

Serial Peripheral Interface (SPI) 177
Serial Peripheral Interface. *See* SPI.
Software Simulator (MPLAB X SIM) 263
Special Features of the CPU 239
SPI
Control Registers 179
Helpful Tips 178
Resources 178

T

Thermal Operating Conditions 266
Thermal Packaging Characteristics 266
Third-Party Development Tools 264
Timer1 133
Control Register 135
Resources 134
Timer2/3 137
Control Registers 139
Resources 137
Timing Diagrams
BOR and Master Clear Reset Characteristics 281
External Clock 278
High-Speed PWMx Fault Characteristics 287
High-Speed PWMx Module Characteristics 287
I/O Characteristics 281
I2C1 Bus Data (Master Mode) 300
I2C1 Bus Data (Slave Mode) 302
I2C1 Bus Start/Stop Bits (Master Mode) 300
I2C1 Bus Start/Stop Bits (Slave Mode) 302
Input Capture 1 (IC1) Characteristics 285
OC1/PWMx Characteristics 286
Output Compare 1 (OC1) Characteristics 286
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) 291
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) 290
SPI1 Master Mode (Half-Duplex, Transmit Only, CKE = 0) 288
SPI1 Master Mode (Half-Duplex, Transmit Only, CKE = 1) 289
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) 298
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) 296
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) 292
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) 294
Timer1-Timer3 External Clock Characteristics 283
UART1 I/O Characteristics 304

U

Unique Device Identifier (UDID) 27
Universal Asynchronous Receiver Transmitter (UART) 193
Control Registers 195
Helpful Tips 194
Resources 194
Universal Asynchronous Receiver Transmitter. *See* UART.

V

Voltage Regulator (On-Chip) 246

W

Watchdog Timer (WDT) 239, 247
Programming Considerations 247
WWW Address 338
WWW, On-Line Support 6

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support