



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs202t-i-so

dsPIC33EPXXGS202 FAMILY

FIGURE 2-6: OFF-LINE UPS

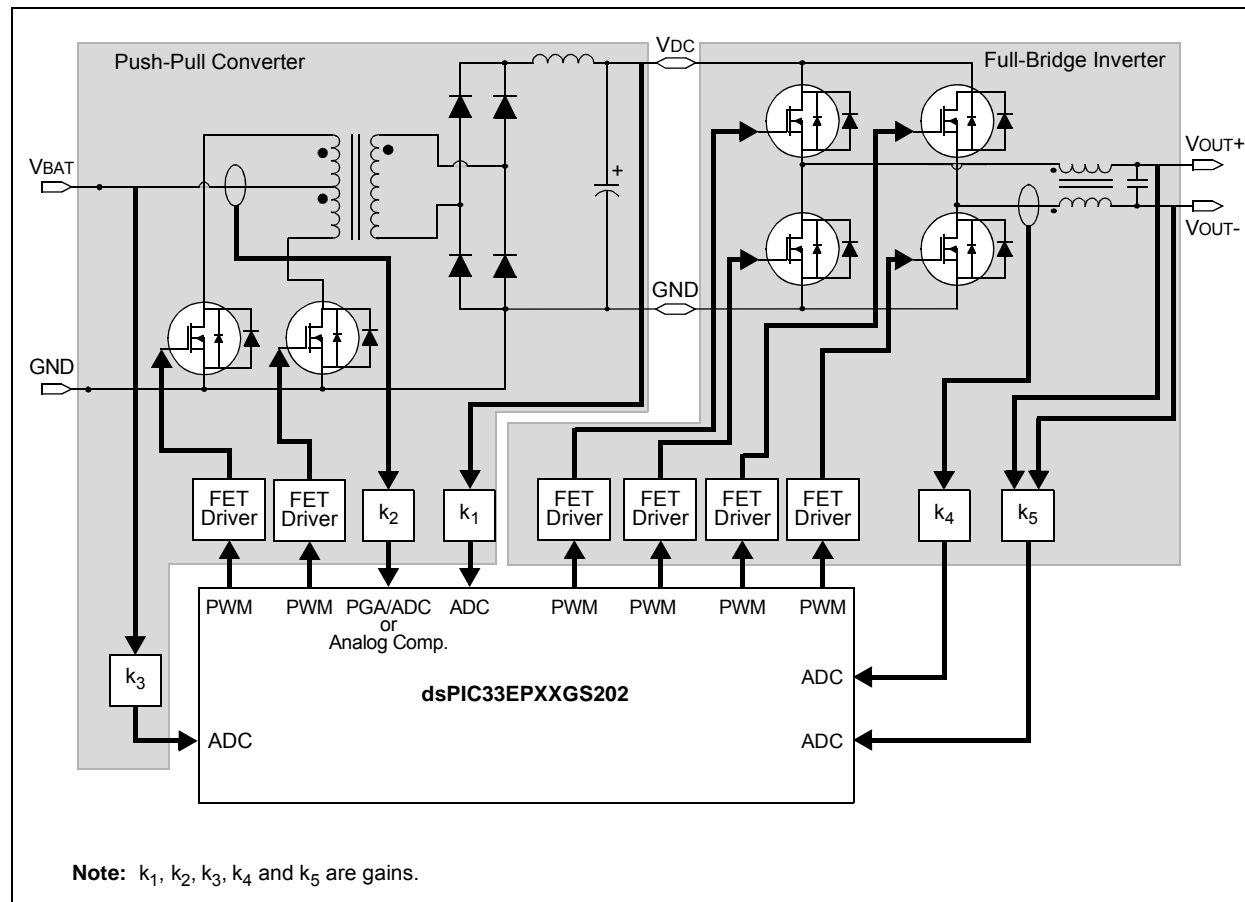


TABLE 4-22: PORTA REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					001F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA<2:0>			0007

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: PORTB REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																FFFF
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	ANSB<10:9>		—	ANSB<7:0>								06FF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.9.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

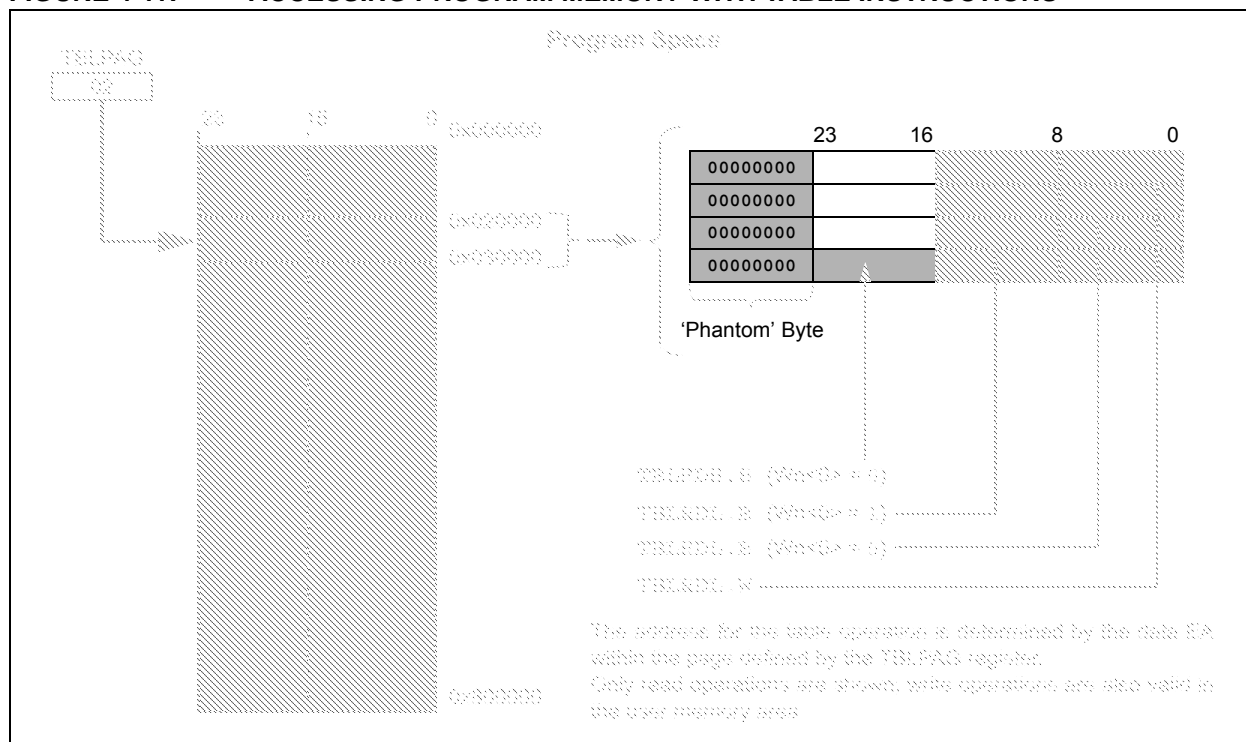
- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location ($P<15:0>$) to a data address ($D<15:0>$)
 - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. The 'phantom' byte ($D<15:8>$) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-11: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



dsPIC33EPXXGS202 FAMILY

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVATE	COVTE
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFail	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled
- bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A
- bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B
- bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A
- bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B
- bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled
- bit 9 **OVATE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled
- bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled
- bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift
- bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

dsPIC33EPXXGS202 FAMILY

6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:

- a) Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
- b) It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
- c) If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
- d) If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
- e) If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self-test.
- f) Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
- g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRISx setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRISx settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned.
- h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select (ANSELx) registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

10.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

10.6.1 KEY RESOURCES

- “**I/O Ports**” (DS70000598) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

dsPIC33EPXXGS202 FAMILY

REGISTER 13-2: IC1CON2: INPUT CAPTURE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0, HS	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG ⁽¹⁾	TRIGSTAT ⁽²⁾	—	SYNCSEL4 ⁽³⁾	SYNCSEL3 ⁽³⁾	SYNCSEL2 ⁽³⁾	SYNCSEL1 ⁽³⁾	SYNCSEL0 ⁽³⁾
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ICTRIG:** Input Capture Trigger Operation Select bit⁽¹⁾

1 = Input source used to trigger the input capture timer (Trigger mode)

0 = Input source used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit⁽²⁾

1 = IC1TMR has been triggered and is running

0 = IC1TMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The input source is selected by the SYNCSEL<4:0> bits of the IC1CON2 register.

2: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.

3: Do not use the IC1 module as its own sync or trigger source.

4: This option should only be selected as a trigger source and not as a synchronization source.

dsPIC33EPXXGS202 FAMILY

REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)

bit 3-0 **SEVTPS<3:0>**: PWM Special Event Trigger Output Postscaler Select bits⁽¹⁾

1111 = 1:16 Postscaler generates a Special Event Trigger on every sixteenth compare match event

•

•

0001 = 1:2 Postscaler generates a Special Event Trigger on every second compare match event

0000 = 1:1 Postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIX feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 15-2: PTCON2: PWM CLOCK DIVIDER SELECT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0> ⁽¹⁾		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>**: PWM Input Clock Prescaler (Divider) Select bits⁽¹⁾

111 = Reserved

110 = Divide-by-64, maximum PWM timing resolution

101 = Divide-by-32, maximum PWM timing resolution

100 = Divide-by-16, maximum PWM timing resolution

011 = Divide-by-8, maximum PWM timing resolution

010 = Divide-by-4, maximum PWM timing resolution

001 = Divide-by-2, maximum PWM timing resolution

000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

dsPIC33EPXXGS202 FAMILY

REGISTER 15-19: TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTM ⁽¹⁾	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
 1110 = Trigger output for every 15th trigger event
 1101 = Trigger output for every 14th trigger event
 1100 = Trigger output for every 13th trigger event
 1011 = Trigger output for every 12th trigger event
 1010 = Trigger output for every 11th trigger event
 1001 = Trigger output for every 10th trigger event
 1000 = Trigger output for every 9th trigger event
 0111 = Trigger output for every 8th trigger event
 0110 = Trigger output for every 7th trigger event
 0101 = Trigger output for every 6th trigger event
 0100 = Trigger output for every 5th trigger event
 0011 = Trigger output for every 4th trigger event
 0010 = Trigger output for every 3rd trigger event
 0001 = Trigger output for every 2nd trigger event
 0000 = Trigger output for every trigger event

bit 11-8 **Unimplemented**: Read as '0'

bit 7 **DTM**: Dual Trigger Mode bit⁽¹⁾

1 = Secondary trigger event is combined with the primary trigger event to create a PWM trigger
 0 = Secondary trigger event is not combined with the primary trigger event to create a PWM trigger;
 two separate PWM triggers are generated

bit 6 **Unimplemented**: Read as '0'

bit 5-0 **TRGSTRT<5:0>**: Trigger Postscaler Start Enable Select bits

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
 •
 •
 •
 000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled
 000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled
 000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWMx generator cannot generate PWM trigger interrupts.

dsPIC33EPXXGS202 FAMILY

REGISTER 17-4: I2C1MSK: I2C1 SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10

Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2C1MSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

dsPIC33EPXXGS202 FAMILY

REGISTER 19-3: ADCON2L: ADC CONTROL REGISTER 2 LOW

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
REFCIE	REFERCIE ⁽²⁾	—	EIEN	—	SHREISEL2 ⁽¹⁾	SHREISEL1 ⁽¹⁾	SHREISEL0 ⁽¹⁾
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SHRADCS6	SHRADCS5	SHRADCS4	SHRADCS3	SHRADCS2	SHRADCS1	SHRADCS0
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **REFCIE:** Band Gap and Reference Voltage Ready Common Interrupt Enable bit
 1 = Common interrupt will be generated when the band gap will become ready
 0 = Common interrupt is disabled for the band gap ready event
- bit 14 **REFERCIE:** Band Gap or Reference Voltage Error Common Interrupt Enable bit⁽²⁾
 1 = Common interrupt will be generated when the band gap or reference voltage error is detected
 0 = Common interrupt is disabled for the band gap and reference voltage error event
- bit 13 **Unimplemented:** Read as '0'
- bit 12 **EIEN:** Early Interrupts Enable bit
 1 = The early interrupt feature is enabled for the input channels interrupts (when E1STATx flag is set)
 0 = The individual interrupts are generated when conversion is done (when ANxRDY flag is set)
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **SHREISEL<2:0>:** Shared Core Early Interrupt Time Selection bits⁽¹⁾
 111 = Early interrupt is set and interrupt is generated 8 TADCORE clocks prior to when the data is ready
 110 = Early interrupt is set and interrupt is generated 7 TADCORE clocks prior to when the data is ready
 101 = Early interrupt is set and interrupt is generated 6 TADCORE clocks prior to when the data is ready
 100 = Early interrupt is set and interrupt is generated 5 TADCORE clocks prior to when the data is ready
 011 = Early interrupt is set and interrupt is generated 4 TADCORE clocks prior to when the data is ready
 010 = Early interrupt is set and interrupt is generated 3 TADCORE clocks prior to when the data is ready
 001 = Early interrupt is set and interrupt is generated 2 TADCORE clocks prior to when the data is ready
 000 = Early interrupt is set and interrupt is generated 1 TADCORE clock prior to when the data is ready
- bit 7 **Unimplemented:** Read as '0'
- bit 6-0 **SHRADCS<6:0>:** Shared ADC Core Input Clock Divider bits
 These bits determine the number of TCORESRC (Core Source Clock) periods for one shared TADCORE (ADC Core Clock) period.
 1111111 = 254 Core Source Clock periods
 •
 •
 •
 0000011 = 6 Core Source Clock periods
 0000010 = 4 Core Source Clock periods
 0000001 = 2 Core Source Clock periods
 0000000 = 2 Core Source Clock periods

- Note 1:** For the 6-bit shared ADC core resolution (SHRRES<1:0> = 00), the SHREISEL<2:0> settings, from '100' to '111', are not valid and should not be used. For the 8-bit shared ADC core resolution (SHRRES<1:0> = 01), the SHREISEL<2:0> settings, '110' and '111', are not valid and should not be used.
- 2:** To avoid false interrupts, the REPERCIE bit must be set only after the module is enabled (ADON = 1).

22.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXGS202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXGS202 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

22.1 Configuration Bits

In the dsPIC33EPXXGS202 family devices, the Configuration Words are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 22-1 with detailed descriptions in Table 22-2. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

dsPIC33EPXXGS202 FAMILY

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSBs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these

cases, the execution takes multiple instruction cycles, with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

TABLE 23-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
$a \in \{b, c, d\}$	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write-back destination address register $\in \{W13, [W13]+ = 2\}$
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{0...15\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address $\in \{0x0000...0x1FFF\}$
lit1	1-bit unsigned literal $\in \{0, 1\}$
lit4	4-bit unsigned literal $\in \{0...15\}$
lit5	5-bit unsigned literal $\in \{0...31\}$
lit8	8-bit unsigned literal $\in \{0...255\}$
lit10	10-bit unsigned literal $\in \{0...255\}$ for Byte mode, $\{0:1023\}$ for Word mode
lit14	14-bit unsigned literal $\in \{0...16384\}$
lit16	16-bit unsigned literal $\in \{0...65535\}$
lit23	23-bit unsigned literal $\in \{0...8388608\}$; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal $\in \{-512...511\}$
Slit16	16-bit signed literal $\in \{-32768...32767\}$
Slit6	6-bit signed literal $\in \{-16...16\}$
Wb	Base W register $\in \{W0...W15\}$
Wd	Destination W register $\in \{Wd, [Wd], [Wd++] , [Wd--], [++Wd], [--Wd] \}$
Wdo	Destination W register $\in \{Wnd, [Wnd], [Wnd++] , [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] \}$
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

dsPIC33EPXXGS202 FAMILY

TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
74	SL	SL f	f = Left Shift f	1	1	C,N,OV,Z
		SL f , WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL Ws, Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL Wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL $Wb, \#lit5, Wnd$	Wnd = Left Shift Wb by $lit5$	1	1	N,Z
75	SUB	SUB Acc	Subtract Accumulators	1	1	OA,OB,OAB,SA,SB,SAB
		SUB f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB f , WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB $\#lit10, Wn$	Wn = Wn – $lit10$	1	1	C,DC,N,OV,Z
		SUB Wb, Ws, Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB $Wb, \#lit5, Wd$	Wd = Wb – $lit5$	1	1	C,DC,N,OV,Z
76	SUBB	SUBB f	f = f – WREG – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB f , WREG	WREG = f – WREG – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB $\#lit10, Wn$	Wn = Wn – $lit10$ – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB Wb, Ws, Wd	Wd = Wb – Ws – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB $Wb, \#lit5, Wd$	Wd = Wb – $lit5$ – (\overline{C})	1	1	C,DC,N,OV,Z
77	SUBR	SUBR f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR f , WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR Wb, Ws, Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR $Wb, \#lit5, Wd$	Wd = $lit5$ – Wb	1	1	C,DC,N,OV,Z
78	SUBBR	SUBBR f	f = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR f , WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR Wb, Ws, Wd	Wd = Ws – Wb – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR $Wb, \#lit5, Wd$	Wd = $lit5$ – Wb – (\overline{C})	1	1	C,DC,N,OV,Z
79	SWAP	SWAP.b Wn	Wn = nibble swap Wn	1	1	None
		SWAP Wn	Wn = byte swap Wn	1	1	None
80	TBLRDH	TBLRDH Ws, Wd	Read Prog<23:16> to Wd <7:0>	1	5	None
81	TBLRDL	TBLRDL Ws, Wd	Read Prog<15:0> to Wd	1	5	None
82	TBLWTH	TBLWTH Ws, Wd	Write Ws <7:0> to Prog<23:16>	1	2	None
83	TBLWTL	TBLWTL Ws, Wd	Write Ws to Prog<15:0>	1	2	None
84	ULNK	ULNK	Unlink Frame Pointer	1	1	SFA
85	XOR	XOR f	f = f .XOR. WREG	1	1	N,Z
		XOR f , WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR $\#lit10, Wn$	Wd = $lit10$.XOR. Wd	1	1	N,Z
		XOR Wb, Ws, Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR $Wb, \#lit5, Wd$	Wd = Wb .XOR. $lit5$	1	1	N,Z
86	ZE	ZE Ws, Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

dsPIC33EPXXGS202 FAMILY

NOTES:

dsPIC33EPXXGS202 FAMILY

TABLE 25-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typ.	Max.	Units	Conditions		
Operating Current (IDD) ⁽¹⁾						
DC20d	5	10	mA	-40°C	3.3V	10 MIPS
DC20a	5	10	mA	+25°C		
DC20b	5	10	mA	+85°C		
DC20c	5	10	mA	+125°C		
DC22d	10	15	mA	-40°C	3.3V	20 MIPS
DC22a	10	15	mA	+25°C		
DC22b	10	15	mA	+85°C		
DC22c	10	15	mA	+125°C		
DC24d	15	20	mA	-40°C	3.3V	40 MIPS
DC24a	15	20	mA	+25°C		
DC24b	15	20	mA	+85°C		
DC24c	15	20	mA	+125°C		
DC25d	20	28	mA	-40°C	3.3V	60 MIPS
DC25a	20	28	mA	+25°C		
DC25b	20	28	mA	+85°C		
DC25c	20	28	mA	+125°C		
DC26d	30	35	mA	-40°C	3.3V	70 MIPS
DC26a	30	35	mA	+25°C		
DC26b	30	35	mA	+85°C		

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing:

```
while(1)
{
    NOP();
}
```
- JTAG is disabled

dsPIC33EPXXGS202 FAMILY

TABLE 25-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DI10	V _{IL}	Input Low Voltage Any I/O Pin and MCLR	V _{SS}	—	0.2 V _{DD}	V	
DI18		I/O Pins with SDA1, SCL1	V _{SS}	—	0.3 V _{DD}	V	SMBus disabled
DI19		I/O Pins with SDA1, SCL1	V _{SS}	—	0.8	V	SMBus enabled
DI20	V _{IH}	Input High Voltage I/O Pins Not 5V Tolerant ⁽⁴⁾	0.8 V _{DD}	—	V _{DD}	V	
		I/O Pins 5V Tolerant and MCLR ⁽⁴⁾	0.8 V _{DD}	—	5.5	V	
		5V Tolerant I/O Pins with SDA1, SCL1 ⁽⁴⁾	0.8 V _{DD}	—	5.5	V	SMBus disabled
		5V I/O Pins with SDA1, SCL1 ⁽⁴⁾	2.1	—	5.5	V	SMBus enabled
		I/O Pins with SDA1, SCL1 Not 5V Tolerant ⁽⁴⁾	0.8 V _{DD}	—	V _{DD}	V	SMBus disabled
		I/O Pins with SDA1, SCL1 Not 5V Tolerant ⁽⁴⁾	2.1	—	V _{DD}	V	SMBus enabled
DI30	ICNPU	Input Change Notification Pull-up Current	50	250	600	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS}
DI31	ICNPD	Input Change Notification Pull-Down Current⁽⁵⁾	—	50	—	μA	V _{DD} = 3.3V, V _{PIN} = V _{DD}

- Note 1:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 5:** V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.
- 6:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 7:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 8:** |Injection Currents| > 0 can affect the ADC results by approximately 4-6 counts.
- 9:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

dsPIC33EPXXGS202 FAMILY

TABLE 25-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min.	Typ.	Max.	Units	Conditions	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz ^(1,2)							
F20a	FRC	-2	0.5	+2	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-0.9	0.5	+0.9	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-2	1	+2	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

Note 2: Over the lifetime of the 28-Lead 4x4 UQFN package device, the internal FRC accuracy could vary between ±4%.

TABLE 25-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Characteristic	Min.	Typ.	Max.	Units	Conditions	
LPRC @ 32.768 kHz ⁽¹⁾							
F21a	LPRC	-30	—	+30	%	$-40^{\circ}\text{C} \leq T_A \leq -10^{\circ}\text{C}$	VDD = 3.0-3.6V
		-20	—	+20	%	$-10^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	VDD = 3.0-3.6V
F21b	LPRC	-30	—	+30	%	$+85^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	VDD = 3.0-3.6V

Note 1: This is the change of the LPRC frequency as VDD changes.

dsPIC33EPXXGS202 FAMILY

TABLE 25-23: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period	—	400	600	μs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 Period
SY12	TWDT	Watchdog Timer Time-out Period	0.81	—	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21a/F21b (see Table 25-21) at +85°C
			3.25	—	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21a/F21b (see Table 25-21) at +85°C
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	30	μs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	—	—	29	μs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μs	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

dsPIC33EPXXGS202 FAMILY

INDEX

A

Absolute Maximum Ratings	265
AC Characteristics	277
ADC Specifications	305
Analog-to-Digital Conversion Requirements	307
Auxiliary PLL Clock	279
Capacitive Loading Requirements on Output Pins	277
External Clock Requirements	278
High-Speed PWMx Requirements	287
I/O Requirements	281
I2C1 Bus Data Requirements (Master Mode)	301
I2C1 Bus Data Requirements (Slave Mode)	303
Input Capture 1 Requirements	285
Internal FRC Accuracy	280
Internal LPRC Accuracy	280
Load Conditions	277
OC1/PWMx Mode Requirements	286
Output Compare 1 Requirements	286
PLL Clock	279
Reset, WDT, OST, PWRT Requirements	282
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	291
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	290
SPI1 Master Mode (Half-Duplex, Transmit Only) Requirements	289
SPI1 Maximum Data/Clock Rate Summary	288
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	299
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	297
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	293
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	295
Temperature and Voltage Specifications	277
Timer1 External Clock Requirements	283
Timer2 External Clock Requirements	284
Timer3 External Clock Requirements	284
UART1 I/O Requirements	304
AC/DC Characteristics	
DACx Specifications	308
High-Speed Analog Comparator Specifications	307
PGAx Specifications	309
Arithmetic Logic Unit (ALU)	26
Assembler	
MPASM Assembler	262

B

Bit-Reversed Addressing	56
Example	57
Implementation	56
Sequence Table (16-Entry)	57

Block Diagrams

16-Bit Timer1 Module	133
ADC Module	200
Addressing for Table Registers	61
CALL Stack Frame	52
Connections for On-Chip Voltage Regulator	246
CPU Core	18
Data Access from Program Space Address Generation	58
Dedicated ADC Core 0-1	201
dsPIC33EPXXGS202 Family	7
High-Speed Analog Comparator x	230
High-Speed PWM Architecture	153
Hysteresis Control	232
I2C1 Module	186
Input Capture Module	141
Interleaved PFC	14
MCLR Pin Connections	12
Multiplexing Remappable Outputs for RPN	112
Off-Line UPS	16
Oscillator System	88
PGAx Functions	236
PGAx Module	235
Phase-Shifted Full-Bridge Converter	15
PLL Module	89
Programmer's Model	20
PSV Read Address Generation	49
Recommended Minimum Connection	12
Remappable Input for U1RX	110
Reset System	69
Security Segments Example	249
Shared ADC Core	201
Shared Port Structure	107
Simplified Conceptual of High-Speed PWM	154
SPI1 Module	177
Suggested Oscillator Circuit Placement	13
Timerx Module (x = 2,3)	138
Type B/Type C Timer Pair (32-Bit Timer)	138
UART1 Module	193
Watchdog Timer (WDT)	247
Brown-out Reset (BOR)	239, 246

C

C Compilers	
MPLAB XC	262
Code Examples	
Port Write/Read	108
PWM Write-Protected Register Unlock Sequence	152
PWRSV Instruction Syntax	99
Code Protection	239, 248
CodeGuard Security	239, 248
Configuration Bits	239
Description	241
Configuration Register Map	240