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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	FlexIO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl13z64vlh4

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3.1 Low-power modes

The ultra-low-power STM32L100C6 and STM32L100R8/RB devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 2.0-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 16* for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to *Table 16* for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 16* for consumption.

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  Sleep mode power consumption: refer to *Table 18*.

- **Low-power Run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (less than 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In the low-power Run mode, the clock frequency and the number of enabled peripherals are both limited.

  Low-power Run mode consumption: refer to *Table 19*.

- **Low-power Sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In the low-power Sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

  Low-power Sleep mode consumption: refer to *Table 20*.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI

Table 3. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See the application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

The HSI oscillator is to be calibrated to +/-1% before using of the bootloader.

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L100C6 and STM32L100R8/RB devices with up to 20 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode see *Table 15: Embedded internal reference voltage*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion

Eight DAC trigger inputs are used in the STM32L100C6 and STM32L100R8/RB devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L100C6 and STM32L100R8/RB devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

3.14 Timers and watchdogs

The ultra-low-power STM32L100C6 and STM32L100R8/RB devices include six general-purpose timers, two basic timers and two watchdog timers.

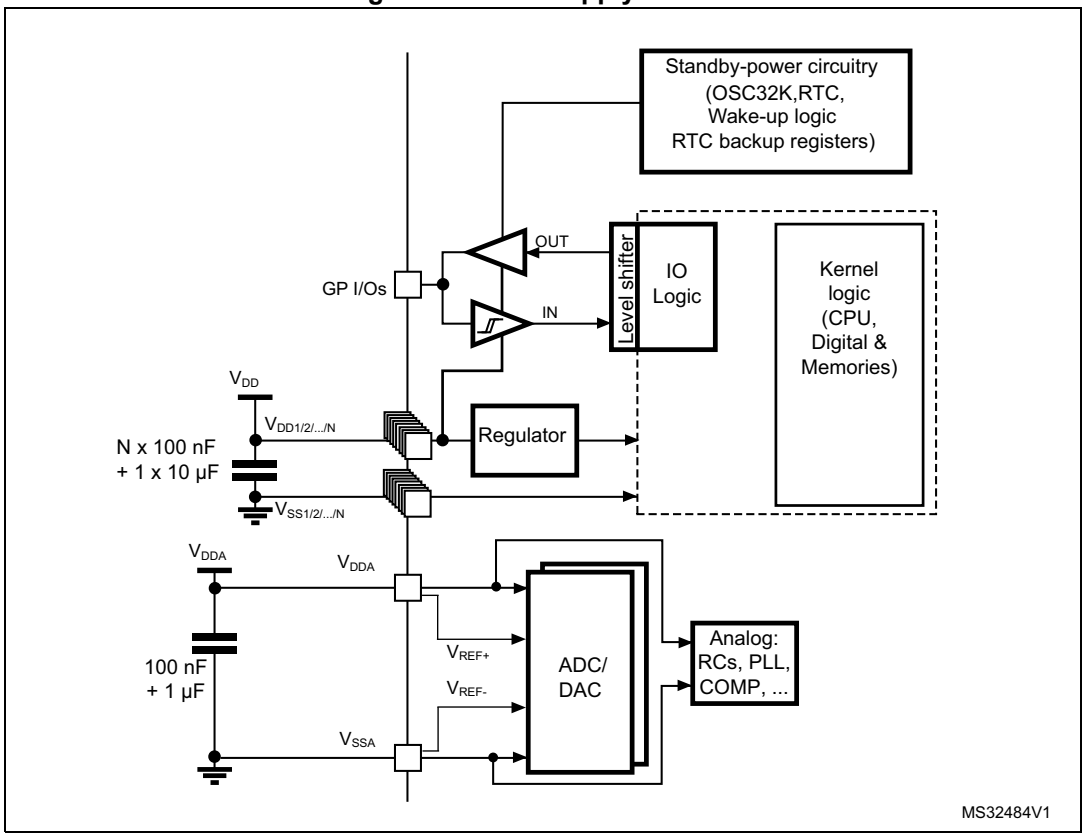
Table 5 compares the features of the general-purpose and basic timers.

Table 5. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

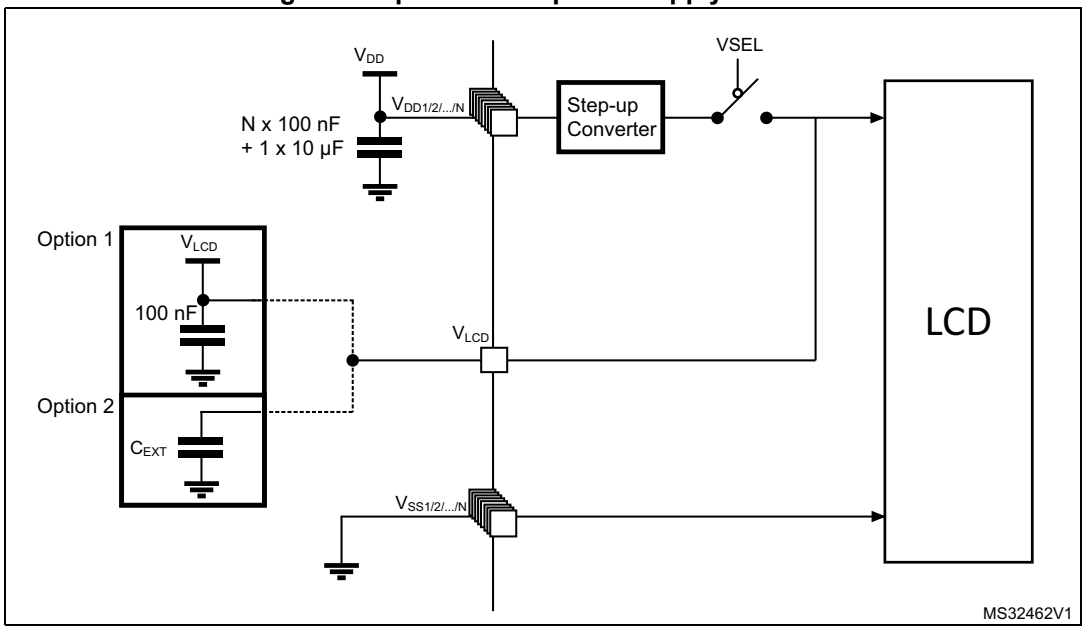
6.1.6 Power supply scheme

Figure 8. Power supply scheme



6.1.7 Optional LCD power supply scheme

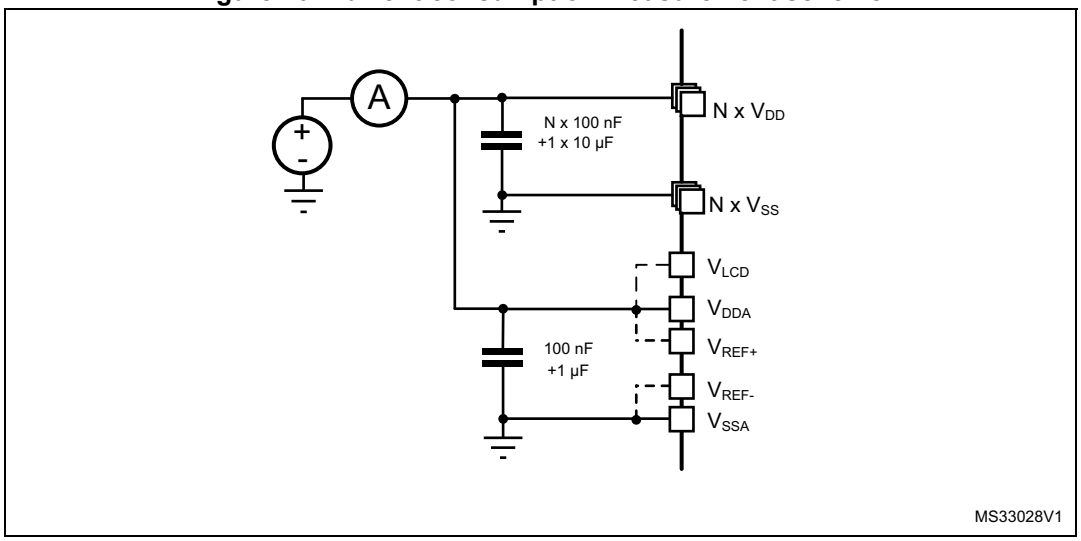
Figure 9. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

Figure 10. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 9: Voltage characteristics*, *Table 10: Current characteristics*, and *Table 11: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 10* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 10. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	80	mA
ΣI_{VSS}	Total current out of V_{SS}ground lines (sink)(1)	80	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3) RST and B pins	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.17*.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 9* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 9: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code, unless otherwise specified.

The current consumption values are derived from the tests performed under ambient temperature T_A=25°C and V_{DD} supply voltage conditions summarized in *Table 12: General operating conditions*, unless otherwise specified.

Maximum current consumption

The MCU is placed under the following conditions:

- V_{DD} = 3.6 V
- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted depending on f_{HCLK} frequency and voltage range.
- Prefetch and 64-bit access are enabled in configurations with 1 wait state.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$.
- When fHCLK > 8 MHz, PLL is ON and PLL inputs are equal to HSI = 8 MHz (if internal clock is used) or HSE = 8 MHz (if HSE bypass mode is used).

Table 17. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1) 105 °C	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	200	300	µA
				2 MHz	380	500	
				4 MHz	720	860	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.9	1	mA
				8 MHz	1.65	2	
				16 MHz	3.2	3.7	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2	2.5	
				16 MHz	4	4.5	
				32 MHz	7.7	8.5	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.3	3.8	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.8	9.2	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	40	80	µA
		MSI clock, 524 kHz		524 kHz	110	160	
		MSI clock, 4.2 MHz		4.2 MHz	700	820	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 12*.

Table 24. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.36	-	µs
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	32	-	
		f_{HCLK} = 262 kHz Flash switched OFF	34	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	8.2	-	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Ranges 1 and 2	8.2	9.3	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 3	7.8	11.2	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	10	12	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	15.5	20	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	29	35	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	53	63	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	105	118	
		f_{HCLK} = MSI = 65 kHz	210	237	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	50	103	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.5	3.2	ms

1. Guaranteed by characterization results, unless otherwise specified

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

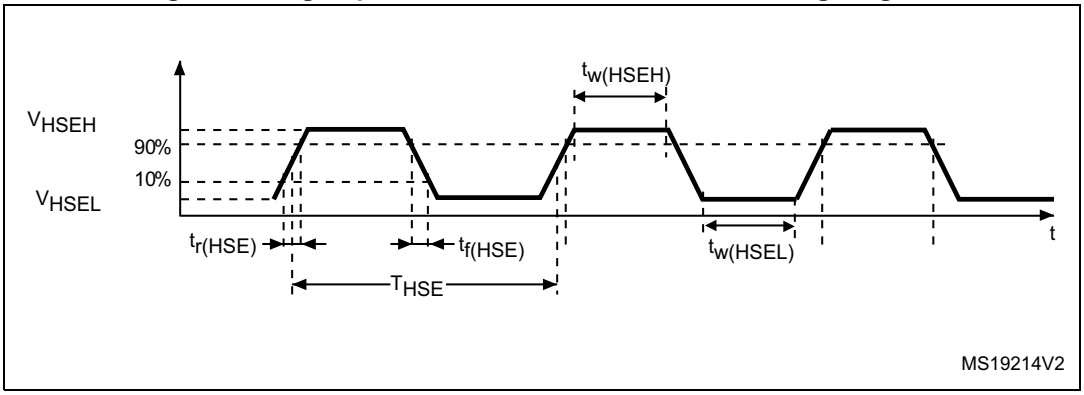
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 11*.

Table 25. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	2.6	-	pF

1. Guaranteed by design.

Figure 11. High-speed external clock source AC timing diagram



Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 39. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence, oscillator frequency deviation, LCD levels).

The test results are given in *Table 40*.

Table 40. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all 5 V tolerant (FT) pins	-5	NA	mA
	Injected current on BOOT0	-0	NA	
	Injected current on any other pin	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Figure 18. SPI timing diagram - slave mode and CPHA = 0

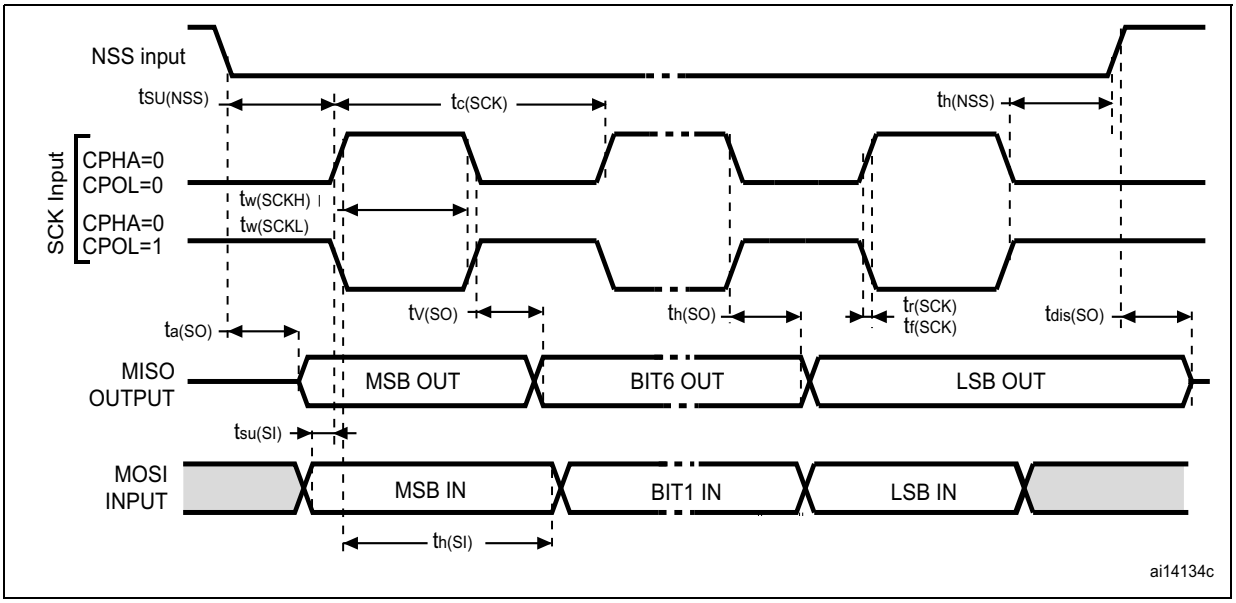
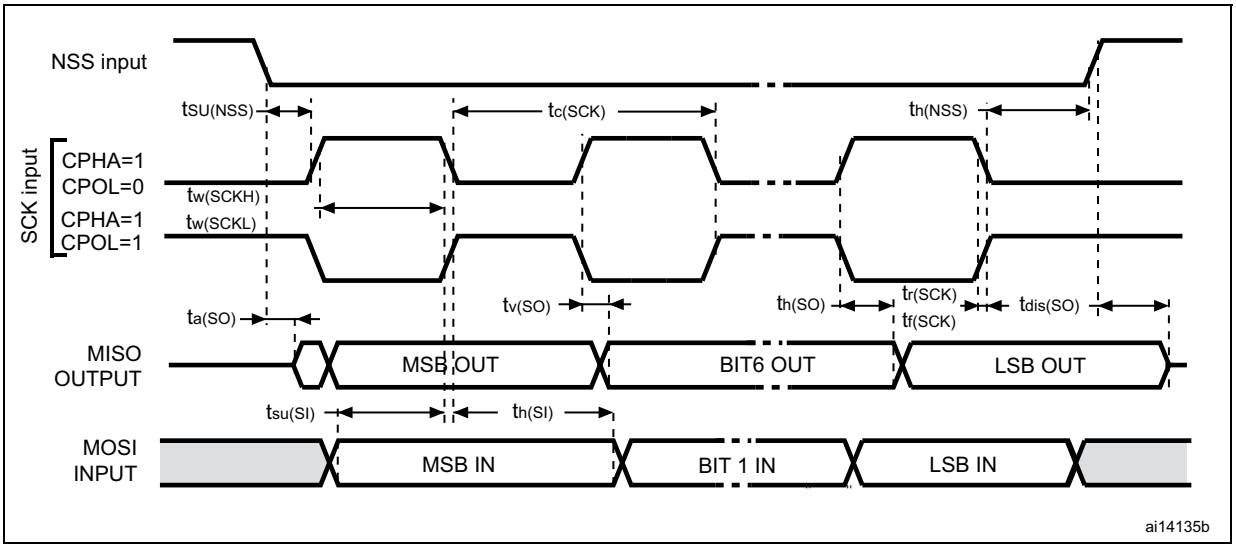


Figure 19. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 53. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}	Signal source impedance(3)	-	-	-	50	κΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. The current consumption through VDDA is composed of two parameters:

   - one constant (max 1300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.

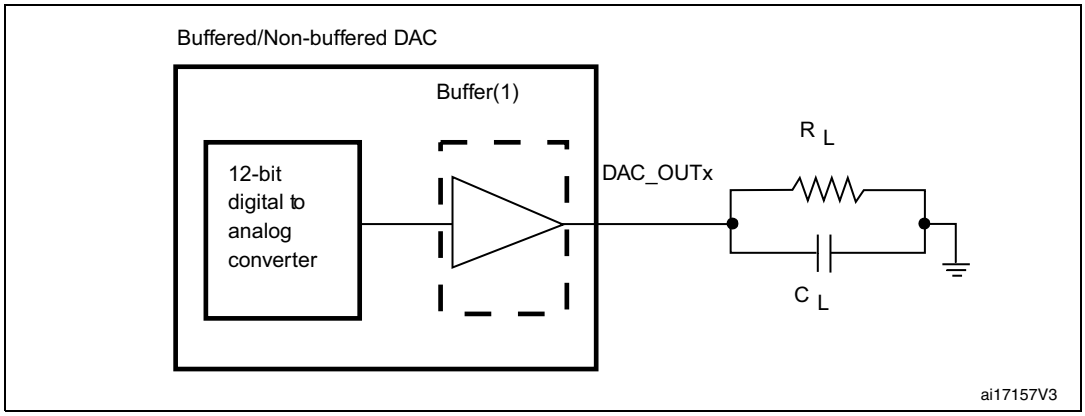
   So, peak consumption is 1300+400 = 1700 µA and average consumption is 1300 + [(4 sampling + 2) /16] x 400 = 1450 µA at 1Msps

2. V_{SSA} must be tied to ground.
3. See *Table 55: Maximum source impedance RAIN max* for R_{AIN} limitations

Table 54. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Min(3)	Typ	Max(3)	Unit
ET	Total unadjusted error	2.4 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 8 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C	-	2.5	4	LSB
EO	Offset error		-	1	2	
EG	Gain error		-	1.5	3.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	2	3	
ENOB	Effective number of bits	2.4 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 16 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C F_{input} =10 kHz	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio		59	62	-	dB
SNR	Signal-to-noise ratio		60	62	-	
THD	Total harmonic distortion		-	-72	-69	
ENOB	Effective number of bits	1.8 V ≤ V_{DDA} ≤ 2.4 V f_{ADC} = 8 MHz or 4 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C F_{input} =10 kHz	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio		59	62	-	dB
SNR	Signal-to-noise ratio		60	62	-	
THD	Total harmonic distortion		-	-72	-69	

Figure 25. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Comparator

Table 57. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.8		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 64. Document revision history (continued)

Date	Revision	Changes
31-Mar-2014 (continued)	2	Deleted second footnote in *Figure 30*. Updated *Section 6.3.11: Electrical sensitivity characteristics* title. Updated section link in second paragraph of *Section 6.3.15: TIM timer characteristics*. Removed all occurrences of “when 8 pins are sourced at same time” in *Table 42: Output voltage characteristics*. Modified first sentence in *Section 6.3.14: NRST pin characteristics*. Updated text and removed figure *Power supply and reference decoupling* in *General PCB design guidelines*. Updated sub-section *TIM10, TIM11 and TIM9*. In *Table 58: Comparator 2 characteristics*, parameter dThreshold/dt, replaced all occurrences of “V_{REF}+” with “V_{REFINT}”. Updated: – *Table 4: Working mode-dependent functionalities (from Run/active down to standby)* – *Table 5: Timer feature comparison* – *Table 7: STM32L100C6 and STM32L100R8/RB pin definitions* – *Table 9: Voltage characteristics* – *Table 12: General operating conditions* – *Table 15: Embedded internal reference voltage* – *Table 25: High-speed external user clock characteristics* – *Table 28: LSE oscillator characteristics (fLSE = 32.768 kHz)* – *Table 29: HSI oscillator characteristics* – *Table 38: ESD absolute maximum ratings* – *Table 40: I/O current injection susceptibility* – *Table 41: I/O static characteristics* – *Table 42: Output voltage characteristics* – *Table 44: NRST pin characteristics* – *Table 61: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data* – *Table 62: Thermal characteristics*, *Table 53: ADC characteristics* Updated: – *Figure 6: Pin loading conditions* – *Figure 7: Pin input voltage* – *Figure 8: Power supply scheme* – *Figure 10: Current consumption measurement scheme* – *Figure 17: I2C bus AC waveforms and measurement circuit* – *Figure 23: Typical connection diagram using the ADC* – *Figure 32: Thermal resistance* Added: – *Figure 28: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example* – *Figure 31: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example* – *Table 6: Legend/abbreviations used in the pinout table*
10-Apr-2014	3	Updated 10 KB RAM in Cover & description.