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### Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

### Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

#### Details

Product Status	Obsolete
Type	Fixed Point
Interface	I <sup>2</sup> C, SAI, SPI
Clock Rate	50MHz
Non-Volatile Memory	-
On-Chip RAM	15kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	-
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/tda7502">https://www.e-xfl.com/product-detail/stmicroelectronics/tda7502</a>

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Table 1. Pin description

N.	Name	Type	Reset status	Function
1	VDD1	P	–	3.3V core supply.
2	GND1	G	–	Core ground.
3	INT	I/O	–	External interrupt line (Input/Output). When this line is asserted low, the DSP may be interrupted. Acts as IRQA line of DSP core.
4	SCANEN	I	–	SCAN enable when active with TESTEN also active, controls the shifting of the internal scan chains.
5	TESTEN	I	–	Test enable when active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When SCANEN is also active, the scan chain shifting
6	DBRQN	I	–	Debug port request Input. A means of entering the Debug mode of operation.
7	DBOUT/GPIO2	I/O	I	The serial data output for the Debug port. Can also be used as a GPIO.
8	VDD2	I	–	3.3V core supply.
9	GND2	I	–	Core ground.
10	DBCK/GPIO0	I/O	I	Debug port Bit Clock/Chip status 1. The serial clock for the Debug Port is provided when an input. When an output, provides information about the chip status. Can also be used as GPIO
11	DBIN/GPIO1	I/O	I	Debug port Serial Input/Chip status 0. The serial data input for the Debug Port is provided when an input. When an output, provides information about the chip status. Can also be used as GPIO.
12	CLKOUT	O	–	Output clock.
13	PGND	G	–	PLL clock ground Input. Ground connection for oscillator circuit.
14	PVCC	P	–	PLL clock power supply. Positive supply for PLL clock oscillator.
15	XTO <sup>(1)</sup>	O	High	Crystal oscillator output. Crystal oscillator output drive.
16	XTI <sup>(1)</sup>	I	–	Crystal oscillator input. External clock input or crystal connection.
17	RESET	I/O	I	System reset. A logic low level applied to RESET input initializes DSPs. During debug mode if this pin is pulled low in while the DBRQN line is pulled low then the DSP pointed to by the DBSEL pin will be reset.
18	VDD3	P	–	3.3V supply.
19	GND3	G	–	Ground.
20	SDI0	I	–	SDI0 is a stereo digital audio data input pin channel 0.
21	SDI1	I	–	SDI1 is a stereo digital audio data input pin channel 1.
22	SDI2	I	–	SDI2 is a stereo digital audio data input pin channel 2.

**Table 1. Pin description** (continued)

N.	Name	Type	Reset status	Function
23	LRCKR	I/O	–	Left-right clock for SAI Receiver. Master or slave.
24	SCKR	I/O	–	SAI receive bit clock. Master or slave.
25	VDD4	P	–	3.3V supply.
26	GND4	G	–	Ground.
27	SDO0	O	High	SDO0 is a stereo digital audio data output pin channel 0.
28	SDO1	O	High	SDO1 is a stereo digital audio data output pin channel 1.
29	SDO2	O	High	SDO2 is a stereo digital audio data pin channel 2.
30	VDD5	P	–	3.3V supply.
31	GND5	G	–	Ground.
32	LRCKT	I/O	–	SAI transmit left/right clock. Master or slave.
33	SCKT	I/O	–	SAI transmit bit clock. Master or slave.
34	SCL	I/O	–	Clock line for I <sup>2</sup> C bus. Schmitt trigger input.
35	SDA	I/O	–	Data line for I <sup>2</sup> C bus. Schmitt trigger input.
36	SCK	I	–	Bit clock for SPI control interface.
37	SS	I	–	Slave select input pin for SPI control interface.
38	MOSI	I/O	–	Serial data output for SPI type serial port when in SPI master mode and serial data input when in SPI slave mode.
39	MISO	I/O	–	Serial data input for SPI style serial port when in SPI master mode and serial data output when in SPI slave mode.
40	VDD6	P	–	3.3V supply.
41	GND6	G	–	Ground.
42	GPIO3	I/O	–	This pin is dedicated as general I/O.
43	GPIO4	I/O	–	This pin is dedicated as general I/O.
44	GPIO5	I/O	–	This pin is dedicated as general I/O.

1. XTI and XTO are not 5V tolerant

## 2 Electrical specifications

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{dd}$	DC supply voltage	-0.5 to 4.6	V
$V_{in}$	Digital input voltage (XTI and XTO only)	-0.5 to ( $V_{DD} + 0.5$ )	V
$V_{in}$	Digital input voltage <sup>(1)</sup>	6.5	V
$T_j$	Operating junction temperature range	-40 to 125	°C
$T_{stg}$	Storage temperature	-55 to 150	°C

1. When the IC is powered.

**Warning:** Operation at or beyond these limit may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{th\ j-amb}$ <sup>(1)</sup>	Thermal resistance junction to ambient	68	°C/W

1. In still air.

**Table 4. Recommended DC operating conditions**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{dd}$	3.3V power supply voltage		3.15	3.3	3.45	V

**Table 5. Current consumption**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{dd}$	Maximum current	@3.3V and $T_j = 125^\circ\text{C}$			250	mA

Note: 50MHz internal DSP clock

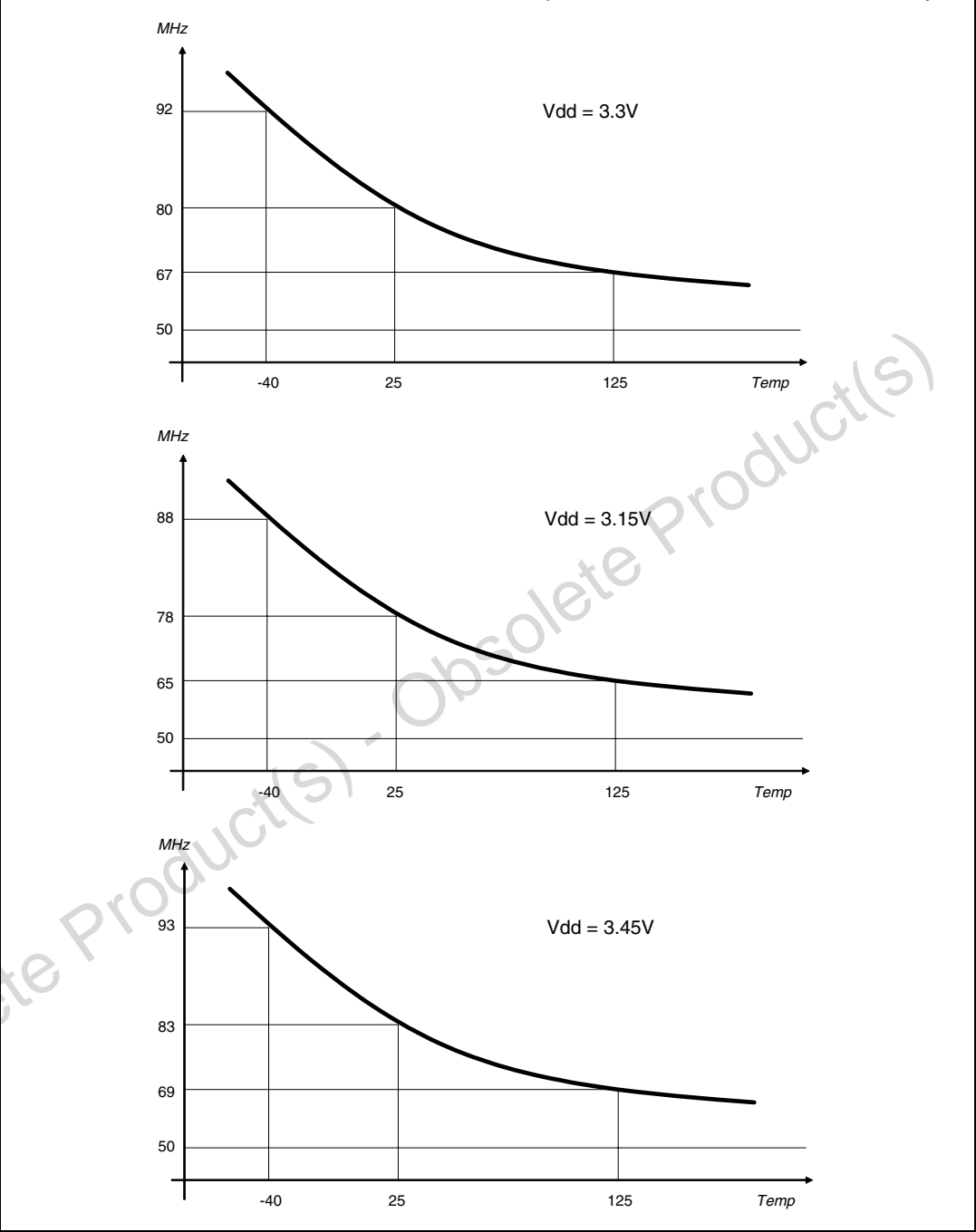
**Table 6. PLL characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	Lock time <sup>(1)</sup>	@3.3V and $T_j = 125^\circ\text{C}$			3	ms
$F_{vco}$	VCO frequency <sup>(2)</sup>		70		140	MHz

1. Depending on VCO output frequency.

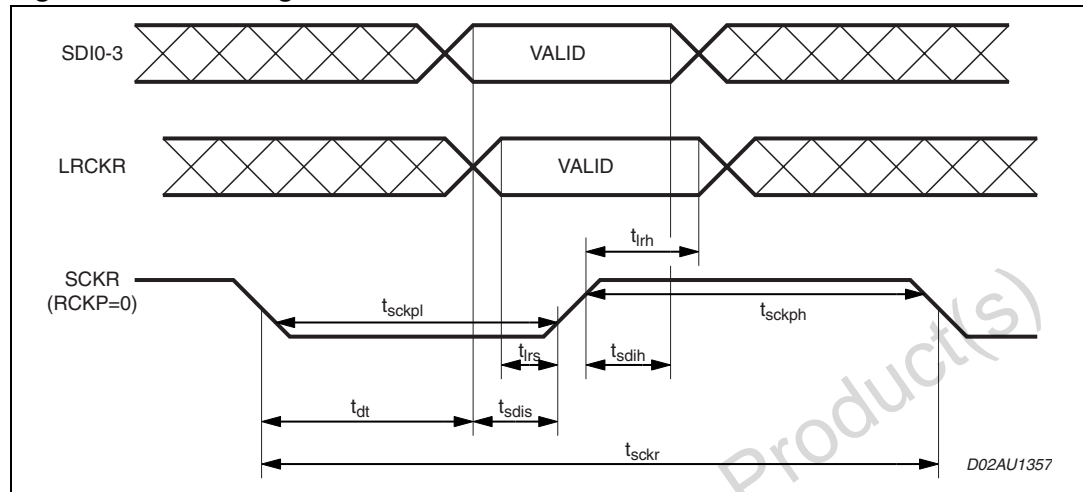
2.  $F_{dsp} = F_{vco}/2$  when PLL is running

Figure 3. Maximum DSP clock frequency ( $F_{dsp}$ ) versus junction temperature ( $T_j$ )



### 3 SAI interface

**Figure 4. SAI timings**

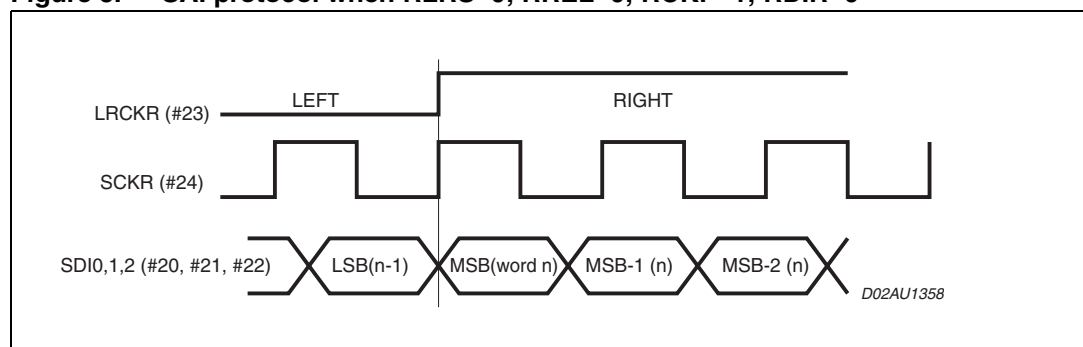


**Table 11. Cycles**

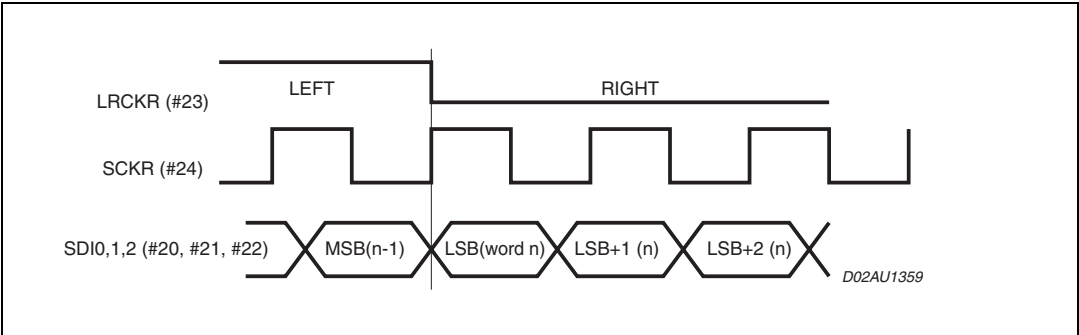
Timing	Description	Value	Unit
$t_{sckr}$	Minimum Clock Cycle	$4T_{DSP}$	ns
$t_{dt}$	SCKR active edge to data out valid	10	ns
$t_{lrs}$	LRCK setup time	5	ns
$t_{lrh}$	LRCK hold time	5	ns
$t_{sdi}$	SDI setup time	15	ns
$t_{sdi}$	SDI hold time	15	ns
$t_{sckph}$	Minimum SCK high time	$0.35 t_{sckr}$	ns
$t_{sckpl}$	Minimum SCK low time	$0.35 t_{sckr}$	ns

Note:  $T_{DSP}$  = dsp master clock cycle time =  $1/F_{DSP}$

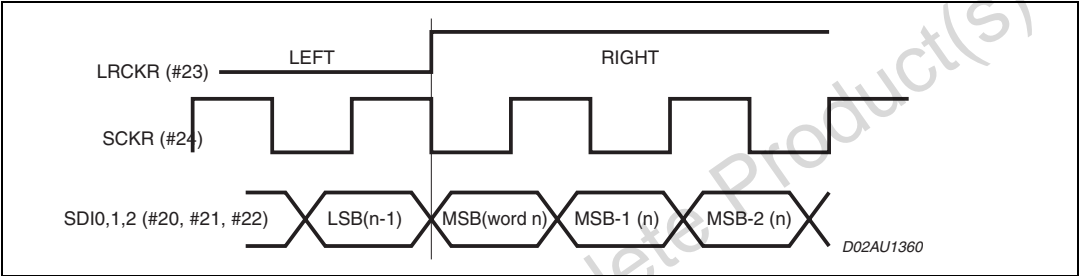
**Figure 5. SAI protocol when RLRS=0; RREL=0; RCKP=1; RDIR=0**



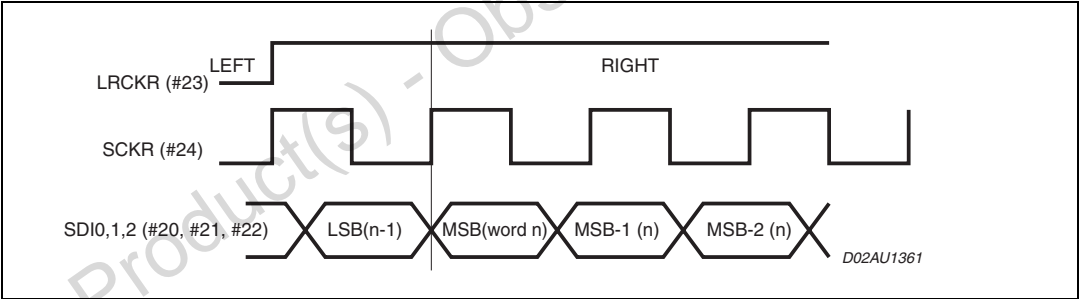
**Figure 6. SAI protocol when RLRS=1; RREL=0; RCKP=1; RDIR=1.**



**Figure 7. SAI protocol when RLRS=0; RREL=0; RCKP=0; RDIR=0.**



**Figure 8. SAI protocol when RLRS=0; RREL=1; RCKP=1; RDIR=0.**



## 4 SPI interfaces

**Table 12. SPI interfaces**

Symbol	Description	Min Value	Unit
<b>Master</b>			
$t_{\text{sclk}}$	Clock cycle	$12T_{\text{DSP}}$	ns
$t_{\text{dtr}}$	Sclk edge to MOSI valid	40	ns
$t_{\text{misosetup}}$	MISO setup time	16	ns
$t_{\text{misohold}}$	MISO hold time	4	ns
$t_{\text{sclkh}}$	SCK high time	$0.5t_{\text{sclk}}$	ns
$t_{\text{sckl}}$	SCK high low	$0.5t_{\text{sclk}}$	ns
<b>Slave</b>			
$t_{\text{sclk}}$	Clock cycle	$12T_{\text{DSP}}$	ns
$t_{\text{dtr}}$	Sclk edge to MOSI valid	40	ns
$t_{\text{mosisetup}}$	MOSI setup time	16	ns
$t_{\text{mosihold}}$	MOSI hold time	4	ns
$t_{\text{sclkh}}$	SCK high time	$0.5t_{\text{sclk}}$	ns
$t_{\text{sckl}}$	SCK high low	$0.5t_{\text{sclk}}$	ns

**Figure 9. SPI clocking scheme.**

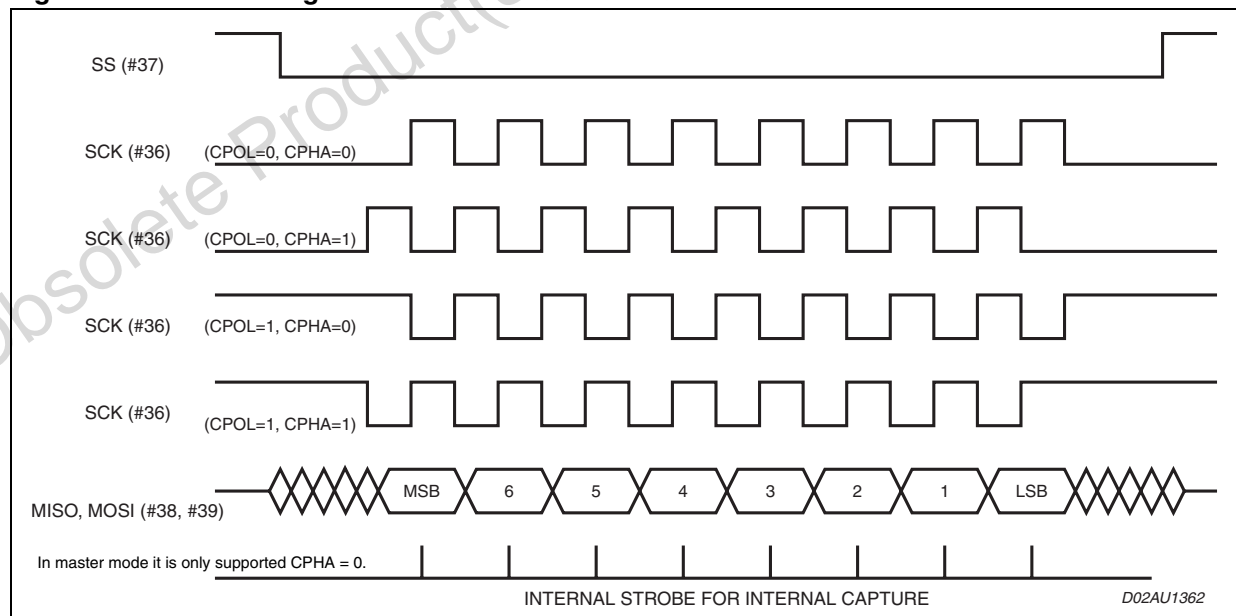


Figure 12. Debug port data I/O to status timing.

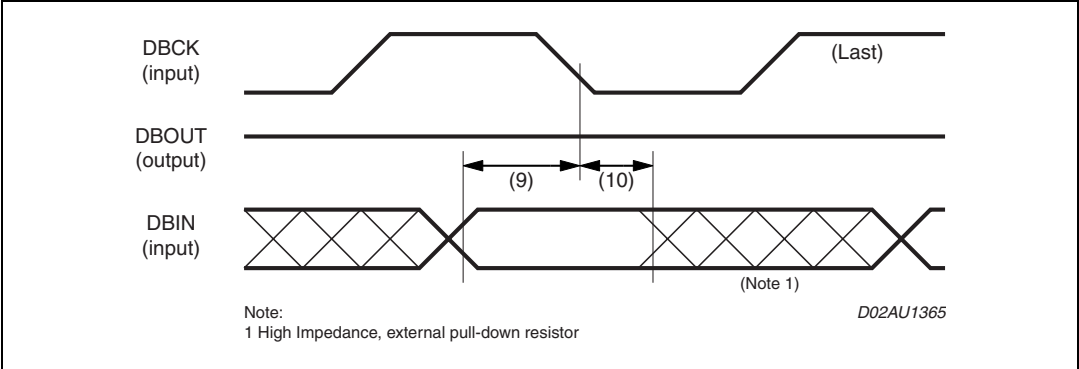


Figure 13. Debug port read timing.

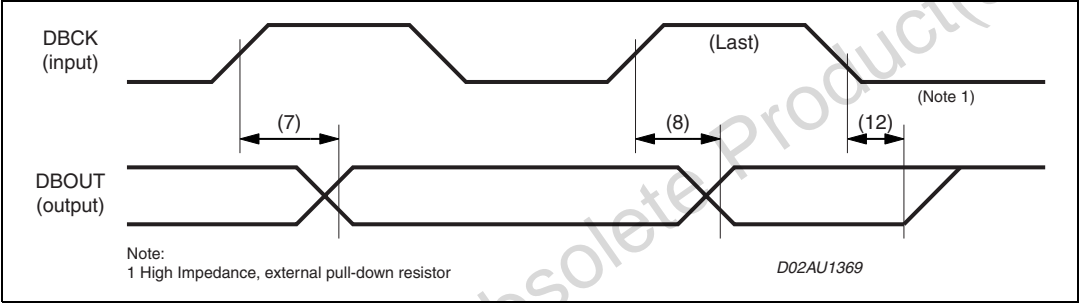
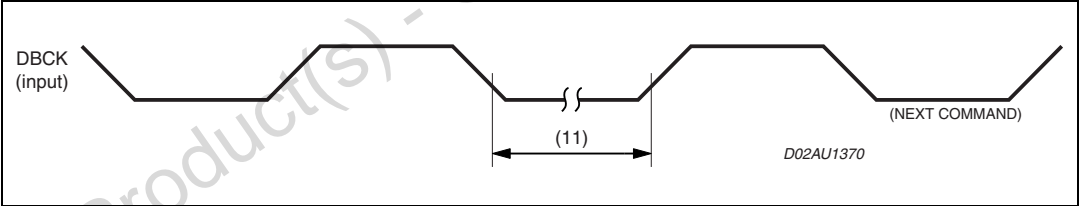


Figure 14. Debug port DBCK next command after read register timing.



## 5 I<sup>2</sup>C timing

Figure 15. Definition of timing for the I<sup>2</sup>C bus.

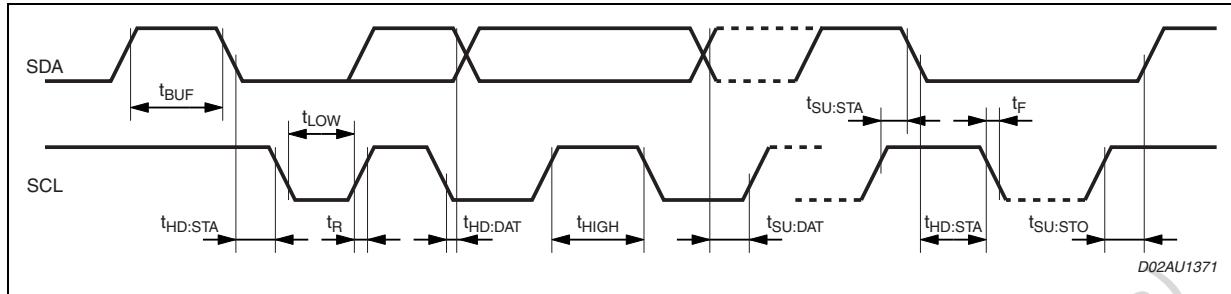


Table 14. Definitions

Symbol	Parameter	Test condition	Standard mode I <sup>2</sup> C bus		Fast mode I <sup>2</sup> C bus		Unit
			Min.	Max.	Min.	Max.	
$F_{SCL}$	SCL clock frequency		0	100	0	400	kHz
$t_{BUF}$	Bus free between a STOP and Start Condition		4.7	–	1.3	–	$\mu$ s
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	$\mu$ s
$t_{LOW}$	LOW period of the SCL clock		4.7	–	1.3	–	$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock		4.0	–	0.6	–	$\mu$ s
$t_{SU:STA}$	Set-up time for a repeated start condition		4.7	–	0.6	–	$\mu$ s
$t_{HD:DAT}$	DATA hold time		0	–	0	0.9	$\mu$ s
$t_R$	Rise time of both SDA and SCL signals	Cb in pF	–	1000	$20+0.1C_b$	300	ns
$t_F$	Fall time of both SDA and SCL signals	Cb in pF	–	300	$20+0.1C_b$	300	ns
$t_{SU:STO}$	Set-up time for STOP condition		4	–	0.6	–	$\mu$ s
$t_{SU:DAT}$	Data set-up time		250	–	–	100	ns
$C_b$	Capacitive load for each bus line		–	400	–	400	pF

## 6 Functional description

The TDA7502 contains one DSP core and associated peripherals.

### 6.1 24-BIT DSP core.

The DSP core is used to process the converted analog audio data coming from the CODEC chip via the SAI and return it for analog conversion. Functions such as volume, tone, balance, and fader control, as well as spatial enhancement and general purpose signal processing may be performed by the DSP.

Some capabilities of the DSPs are listed below:

Single cycle multiply and accumulate with convergent rounding and condition code generation

- 2 x 56-bit accumulators.
- Double precision multiply.
- Scaling and saturation arithmetic.
- 48-bit or 2 x 24-bit parallel moves.
- 64 interrupt vector locations.
- Fast or long interrupts possible.
- Programmable interrupt priorities and masking.
- 8 each of address registers, address offset registers and address modulo registers.
- linear, reverse carry, multiple buffer modulo, multiple wrap-around modulo address arithmetic.
- Post-increment or decrement by 1 or by offset, index by offset, predecrement address.
- Repeat instruction and zero overhead DO loops.
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts/subroutines.
- Bit manipulation instructions possible on all registers and memory locations. Also jump on bit test..
- 4 pin serial debug interface.
- Debug access to all internal registers, buses and memory locations.
- 5 word deep program address history FIFO.
- Hardware and software breakpoints for both program and data memory accesses.
- Debug single stepping, Instruction injection and disassembly of program memory.

## 6.2 DSP peripherals

There are a number of peripherals that are tightly coupled to the DSP Core. Each of the peripherals are listed below and described in the following sections.

- 1024 x 24-Bit X-RAM.
- 1024 x 24-Bit Y-RAM.
- 3072 x 24-Bit program RAM.
- 512 x 24-Bit Boot ROM.
- Serial audio interface (SAI).
- Programmable control interface (SPI/I<sup>2</sup>C).
- GPIO.
- PLL clock oscillator.

## 6.3 Data and program memory

Each of the memories are described below.

### 6.3.1 1024 x 24-Bit X-RAM (XRAM)

This is a 1024 x 24-Bit single port SRAM used for storing coefficients. The 16-Bit XRAM address, XABx(15:0) is generated by the address generation unit of the DSP core. The 24-Bit XRAM Data, XDBx(23:0), may be written to and read from the data ALU of the DSP core. The XDBx Bus is also connected to the internal bus switch so that it can be routed to and from all peripheral blocks.

### 6.3.2 1024 x 24 Bit Y-RAM (YRAM)

This is a 1024 x 24-Bit single port SRAM used for storing coefficients. The 16-Bit address, YABx(15:0) is generated by the address generation unit of the DSP core. The 24-Bit Data, YDBx(23:0), is written to and read from the Data ALU of the DSP core. The YDBx Bus is also connected to the internal bus switch so that it can be routed to and from other blocks.

### 6.3.3 3072 X 24-Bit Program RAM

This is a 3072 x 24-Bit single port SRAM used for storing and executing program code. The 16-Bit PRAM Address, PABx(15:0) is generated by the program address generator of the DSP core for instruction fetching, and by the AGU in the case of the move program memory (MOVEM) instruction. The 24-Bit PRAM Data (program code), PDBx(23:0), can only be written to using the MOVEM instruction.

During instruction fetching the PDBx bus is routed to the program decode controller of the DSP core for instruction decoding.

Spare space in the program area may be used as data memory to implement delay lines for example.

### 6.3.4 512 x 24-Bit Bootstrap ROM (Boot ROM)

This is a 512 x 24-Bit factory programmed Boot ROM used for storing the program sequence for initializing the DSP.

Every component hooked up to the I<sup>2</sup>C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and /or transmitter on its functionality.

### 6.3.8 General purpose input/output

The DSP requires a set of external general purpose input/output lines, and a reset line. These signals are used by external devices to signal events to the DSP. The GPIO lines are implemented as DSP's peripherals.

### 6.3.9 PLL clock oscillator

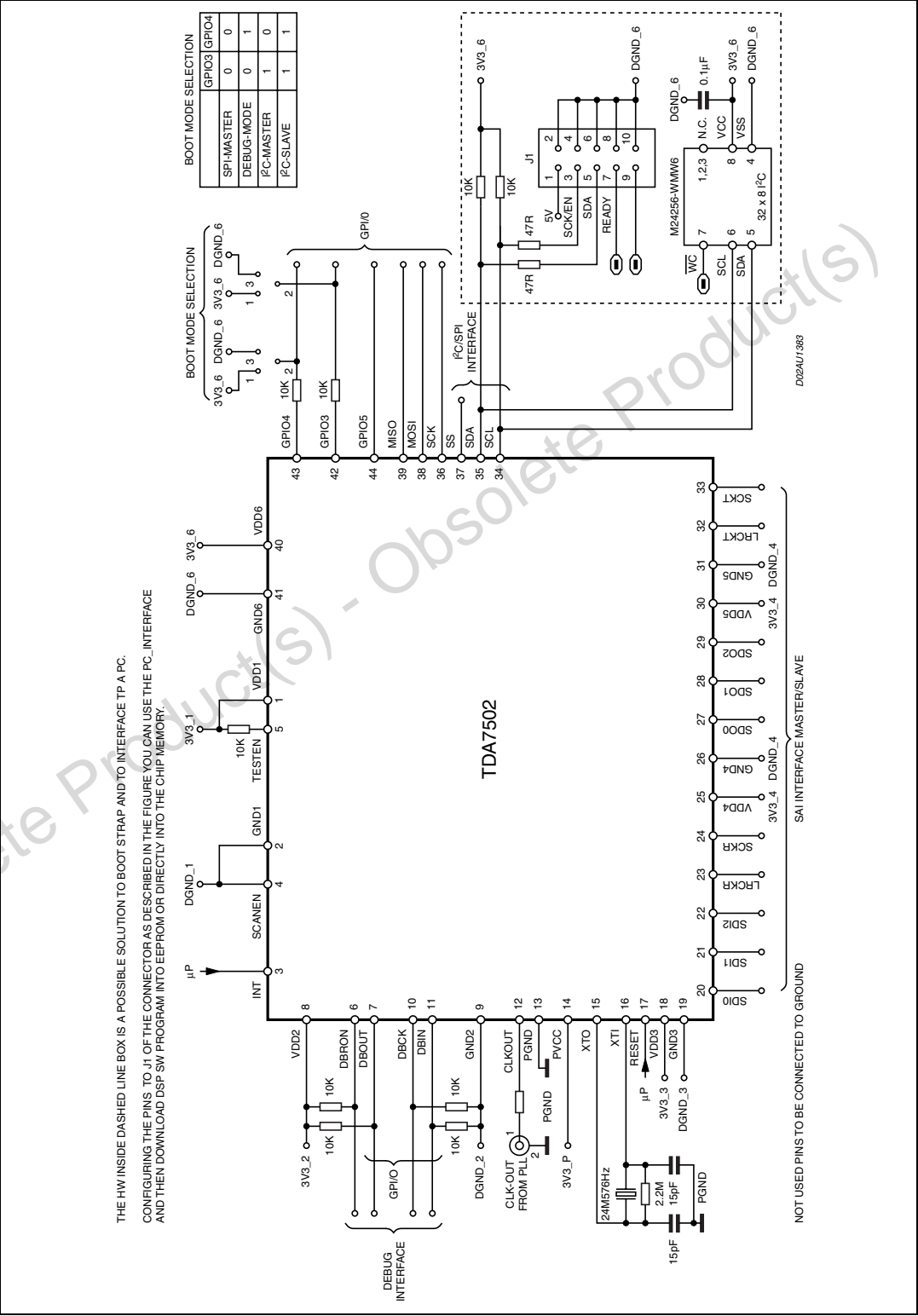
The PLL clock oscillator can accept an external clock at XTI or it can be configured to run an internal oscillator when a crystal is connected across pins XTI & XTO. There is an input divide block IDF (1 -> 32) at the XTI clock input and a multiply block MF (9 -> 128) in the PLL loop. Hence the PLL can multiply the external input clock by a ratio MF/IDF to generate the internal clock. This allows the internal clock to be within 2 MHz of any desired frequency even when XTI is much greater than 1 MHz. It is recommended that the input clock is not divided down to less than 1 MHz as this reduces the phase detector's update rate.

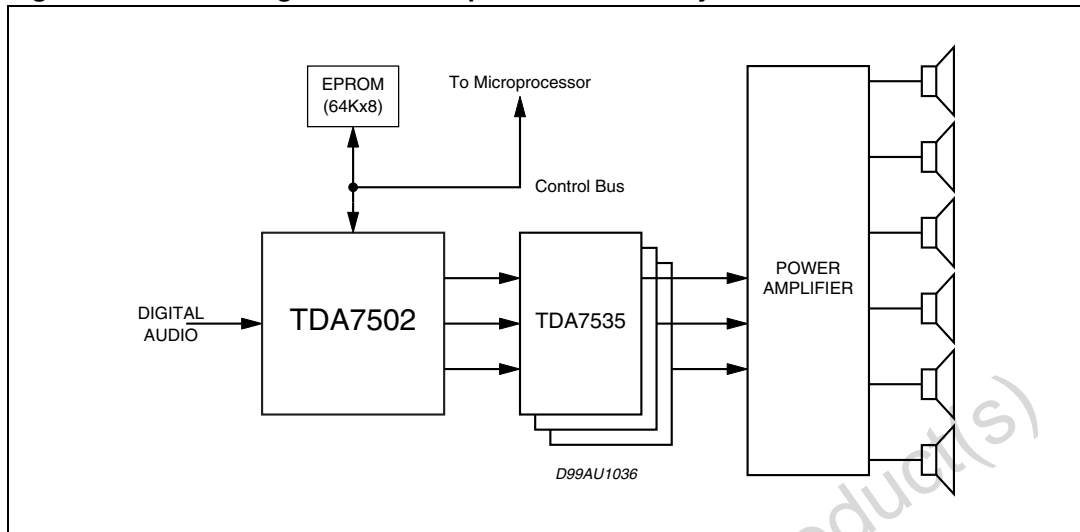
The clocks to the DSP can be selected to be either the VCO output divided by 2 to 16, or be driven by the XTI pin directly.

The crystal oscillator and the PLL will be gated off when entering the power-down mode (by setting a register on DSP0).

7 Application scheme

Figure 16. Application schematic for TDA7502



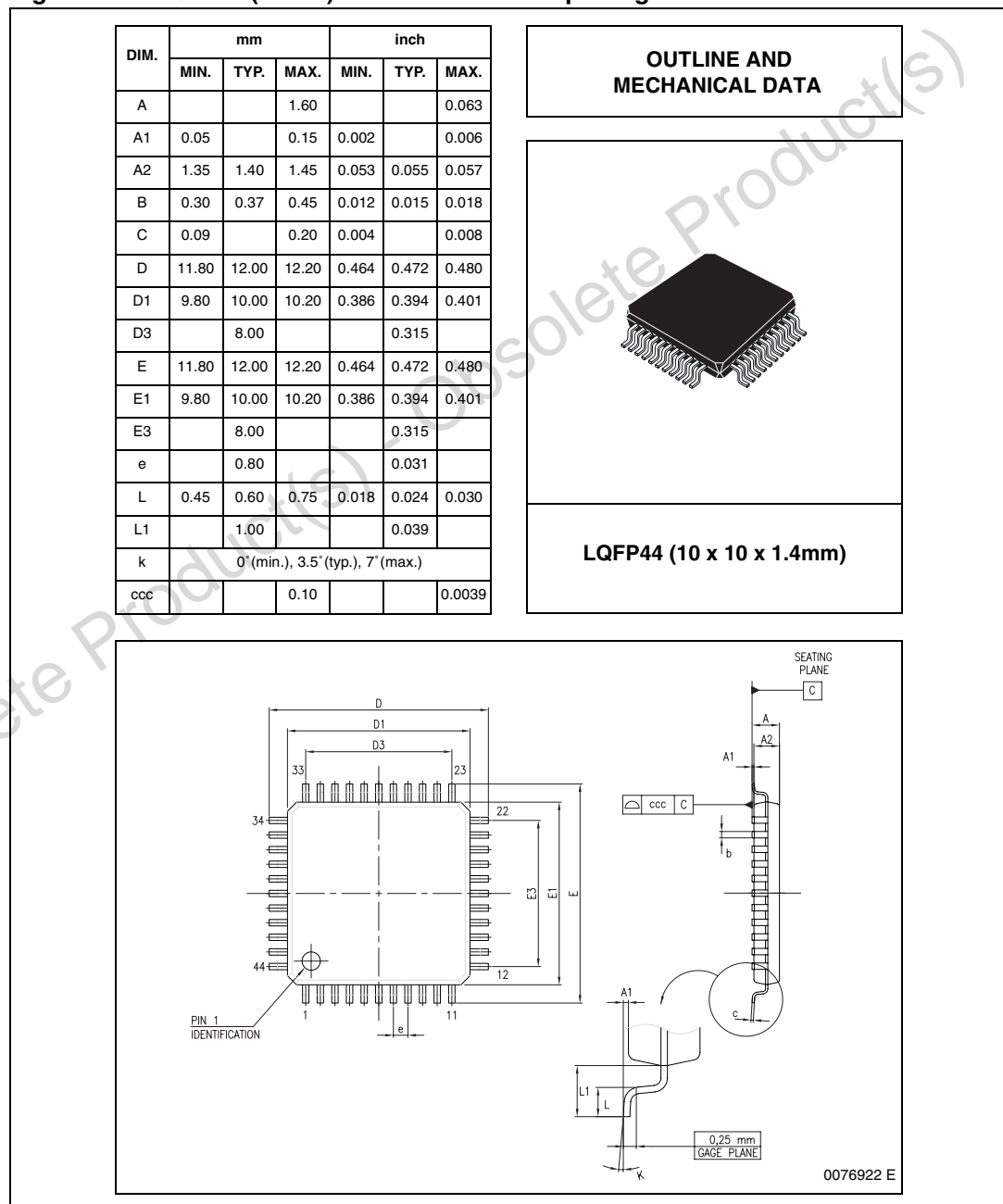
**Figure 17. Block diagram of car amplifier audio sub-system.**

## 8 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 18. TQFP44 (10x10) mechanical data & package dimensions**



## 9 Revision history

**Table 16. Revision history**

Date	Revision	Description of changes
January 2004	8	First Issue in EDOCS dms.
September 2004	9	Changed the style-sheet look. Cancelled the "Package Marking" information.
March 2005	10	Changed SPI interface description and Figure 4.
24-Nov-2006	11	Package changed, layout changes, text modifications.

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