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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12320vte25v

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- High-speed operation
 - All frequently-used instructions execute in one or two states
 - Maximum clock rate: 25 MHz
 - 8/16/32-bit register-register add/subtract: 40 ns
 - 8×8 -bit register-register multiply: 480 ns
 - $16 \div 8$ -bit register-register divide: 480 ns
 - 16×16 -bit register-register multiply: 800 ns
 - $32 \div 16$ -bit register-register divide: 800 ns
- CPU operating mode
 - Advanced mode
- Power-down state
 - Transition to power-down state by SLEEP instruction
 - CPU clock speed selection

2.1.2 Differences between H8S/2600 CPU and H8S/2000 CPU

The differences between the H8S/2600 CPU and the H8S/2000 CPU are as shown below.

- Register configuration

The MAC register is supported only by the H8S/2600 CPU.
- Basic instructions

The four instructions MAC, CLRMAC, LDMAC, and STMAC are supported only by the H8S/2600 CPU.
- Number of execution states

The number of execution states of the MULXU and MULXS instructions.

Instruction	Mnemonic	Internal Operation	
		H8S/2600	H8S/2000
MULXU	MULXU.B Rs, Rd	3	12
	MULXU.W Rs, ERd	4	20
MULXS	MULXS.B Rs, Rd	4	13
	MULXS.W Rs, ERd	5	21

There are also differences in the address space, CCR and EXR functions, power-down state, etc., depending on the product.

2.6.4 Basic Instruction Formats

The CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op field), a register field (r field), an effective address extension (EA field), and a condition field (cc).

Figure 2.9 shows examples of instruction formats.

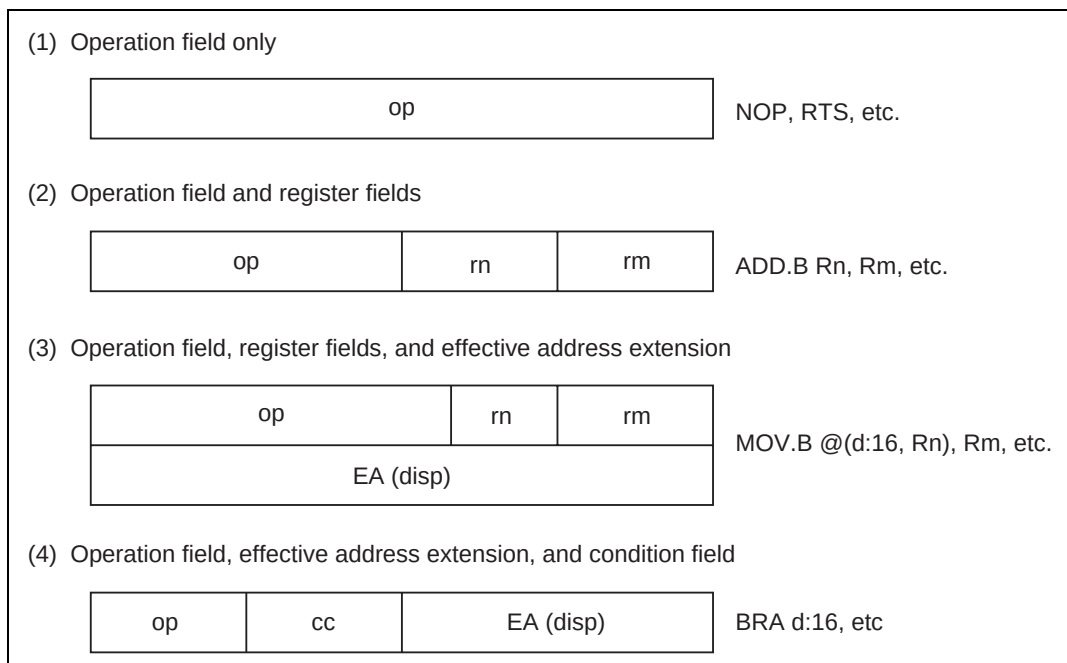


Figure 2.9 Instruction Formats (Examples)

(1) Operation Field: Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.

(2) Register Field: Specifies a general register. Address registers are specified by 3 bits, data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.

(3) Effective Address Extension: Eight, 16, or 32 bits specifying immediate data, an absolute address, or a displacement.

(4) Condition Field: Specifies the branching condition of Bcc instructions.

Bit 6—Data Transfer Enable 1A (DTE1A): Enables or disables data transfer on channel 1A.

Bit 6

DTE1A	Description	
0	Data transfer disabled	(Initial value)
1	Data transfer enabled	

Bit 5—Data Transfer Enable 0B (DTE0B): Enables or disables data transfer on channel 0B.

Bit 5

DTE0B	Description	
0	Data transfer disabled	(Initial value)
1	Data transfer enabled	

Bit 4—Data Transfer Enable 0A (DTE0A): Enables or disables data transfer on channel 0A.

Bit 4

DTE0A	Description	
0	Data transfer disabled	(Initial value)
1	Data transfer enabled	

Bits 3 to 0—Data Transfer End Interrupt Enable (DTIE): These bits enable or disable an interrupt to the CPU or DTC when transfer ends. If the DTIE bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC.

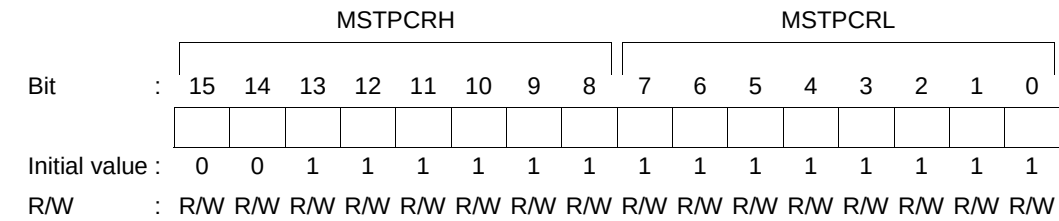
A transfer end interrupt can be canceled either by clearing the DTIE bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the transfer counter and address register again, and then setting the DTE bit to 1.

Bit 3—Data Transfer Interrupt Enable 1B (DTIE1B): Enables or disables the channel 1B transfer end interrupt.

Bit 3

DTIE1B	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

7.4.3 Module Stop Control Register (MSTPCR)



unless the prescribed register is accessed in a DMA transfer. If the same interrupt is used as an activation source for more than one channel, the interrupt request flag is cleared when the highest-priority channel is activated first. Transfer requests for other channels are held pending in the DMAC, and activation is carried out in order of priority.

When DTE = 0, such as after completion of a transfer, a request from the selected activation source is not sent to the DMAC, regardless of the DTA bit. In this case, the relevant interrupt request is sent to the CPU or DTC.

In case of overlap with a CPU interrupt source or DTC activation source (DTA = 0), the interrupt request flag is not cleared by the DMAC.

Activation by External Request: If an external request ($\overline{\text{DREQ}}$ pin) is specified as an activation source, the relevant port should be set to input mode in advance.

Level sensing or edge sensing can be used for external requests.

External request operation in normal mode (short address mode or full address mode) is described below.

When edge sensing is selected, a 1-byte or 1-word transfer is executed each time a high-to-low transition is detected on the $\overline{\text{DREQ}}$ pin. The next transfer may not be performed if the next edge is input before transfer is completed.

When level sensing is selected, the DMAC stands by for a transfer request while the $\overline{\text{DREQ}}$ pin is held high. While the $\overline{\text{DREQ}}$ pin is held low, transfers continue in succession, with the bus being released each time a byte or word is transferred. If the $\overline{\text{DREQ}}$ pin goes high in the middle of a transfer, the transfer is interrupted and the DMAC stands by for a transfer request.

Activation by Auto-Request: Auto-request activation is performed by register setting only, and transfer continues to the end.

With auto-request activation, cycle steal mode or burst mode can be selected.

In cycle steal mode, the DMAC releases the bus to another bus master each time a byte or word is transferred. DMA and CPU cycles usually alternate.

In burst mode, the DMAC keeps possession of the bus until the end of the transfer, and transfer is performed continuously.

Single Address Mode: The DMAC can operate in dual address mode in which read cycles and write cycles are separate cycles, or single address mode in which read and write cycles are executed in parallel.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value :		0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. Set the WAITPS bit before setting the DDR bit clear to 0 and the WAITE bit in BCRL to 1.

Bit 7

WAITPS	Description
0	$\overline{\text{WAIT}}$ input is PF ₂ pin (Initial value)
1	$\overline{\text{WAIT}}$ input is P5 ₃ pin

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. Set the BREQOPS bit before setting the BREQOE bit in BCRL to 1.

Bit 6

BREQOPS	Description
0	$\overline{\text{BREQO}}$ output is PF ₂ pin (Initial value)
1	$\overline{\text{BREQO}}$ output is P5 ₃ pin

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS1}}$, $\overline{\text{CS6}}$, and $\overline{\text{CS7}}$ output. For details, see section 9.7, Port 6, and section 9.14, Port G.

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS2}}$, $\overline{\text{CS3}}$, $\overline{\text{CS4}}$, and $\overline{\text{CS5}}$ output. For details, see section 9.7, Port 6, and section 9.14, Port G.

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 9.13, Port F.

- Example of input capture operation

Figure 10.13 shows an example of input capture operation.

In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

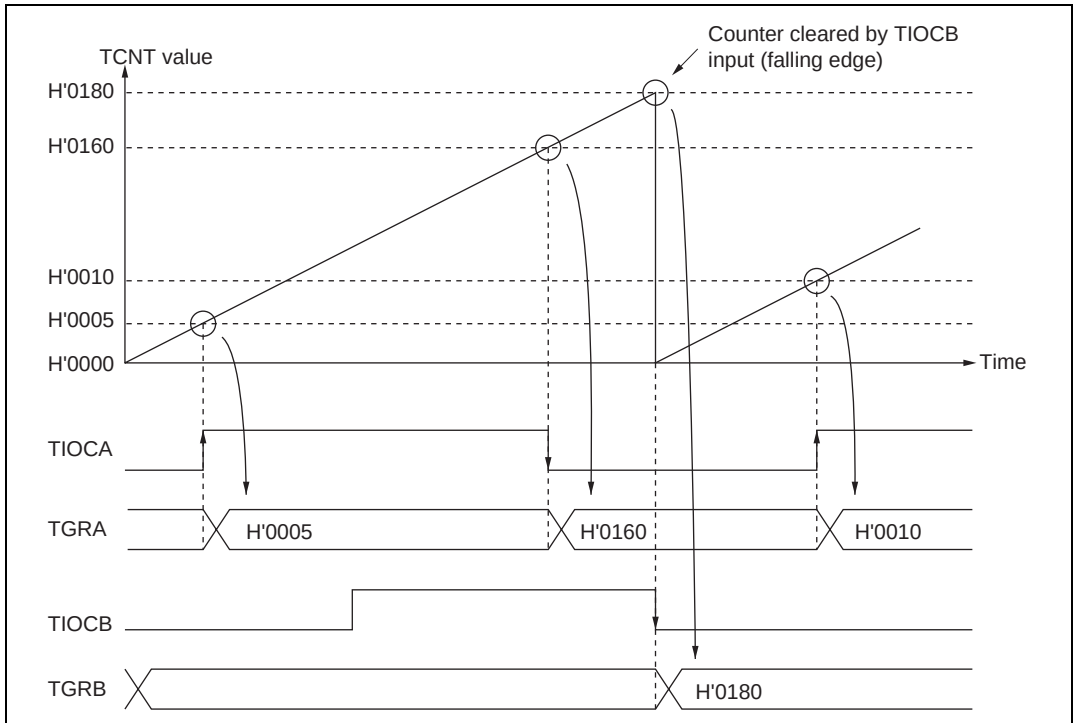


Figure 10.13 Example of Input Capture Operation

Figure 10.27 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

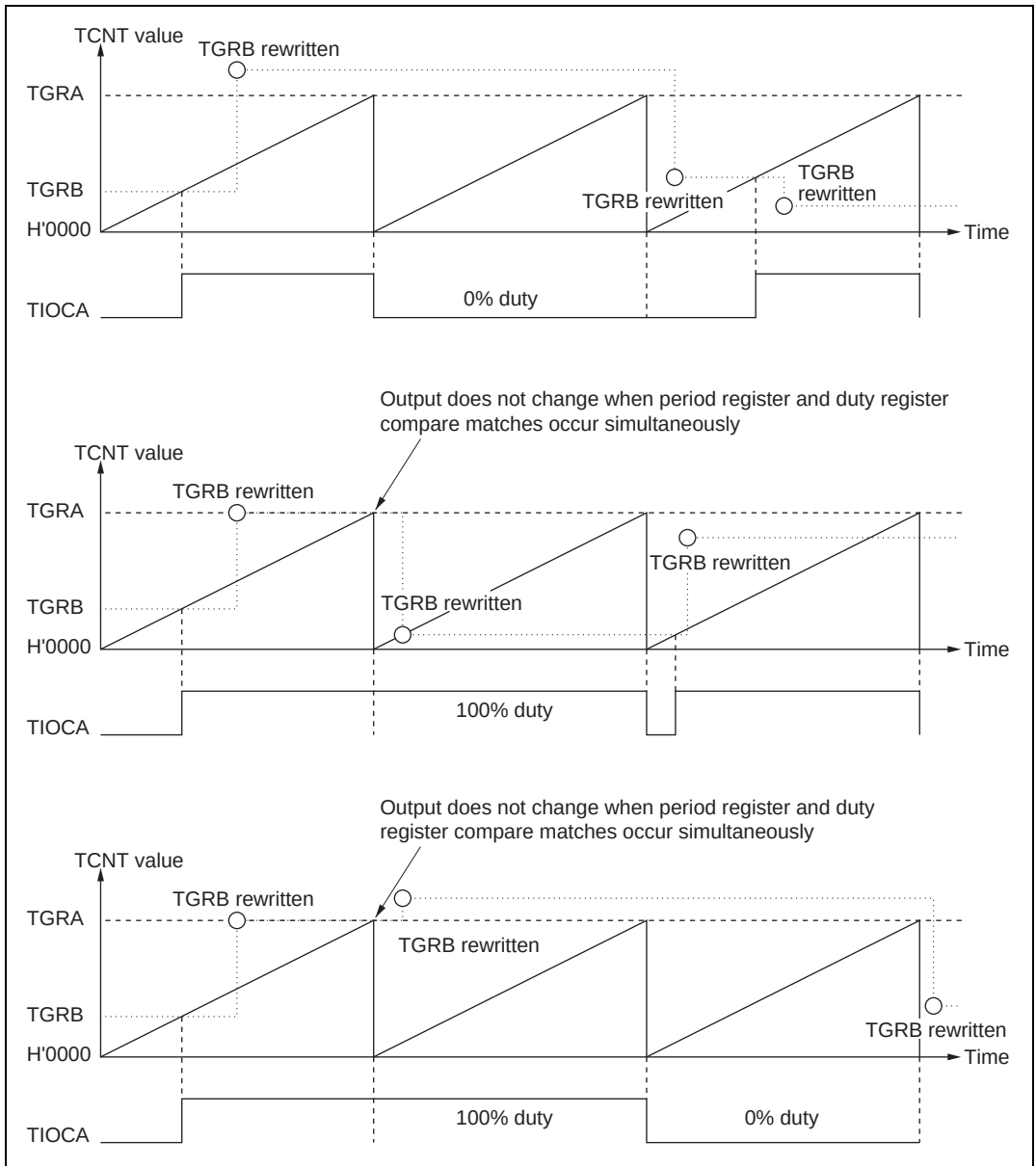


Figure 10.27 Examples of PWM Mode Operation (3)

12.3.3 Timing of TCNT External Reset

TCNT is cleared at the rising edge of an external reset input, depending on the settings of the CCLR1 and CCLR0 bits in TCR. The clear pulse width must be at least 1.5 states. Figure 12.7 shows the timing of this operation.

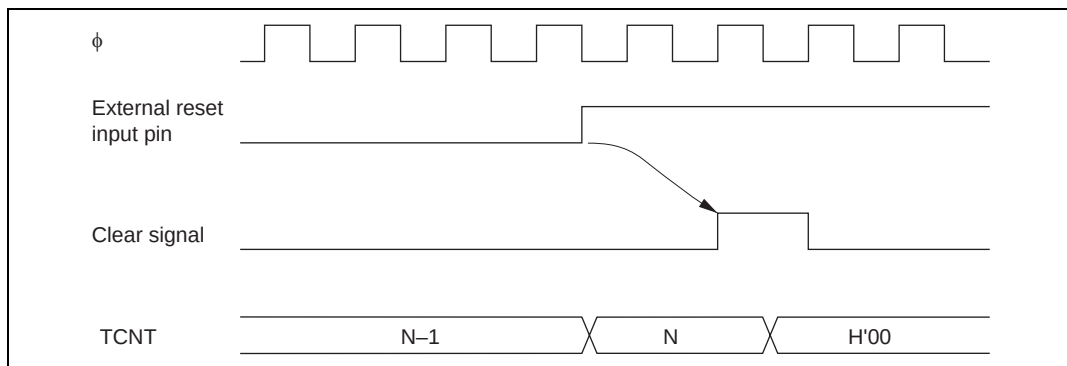


Figure 12.7 Timing of Clearance by External Reset

12.3.4 Timing of Overflow Flag (OVF) Setting

The OVF in TCSR is set to 1 when TCNT overflows (changes from $H'FF$ to $H'00$). Figure 12.8 shows the timing of this operation.

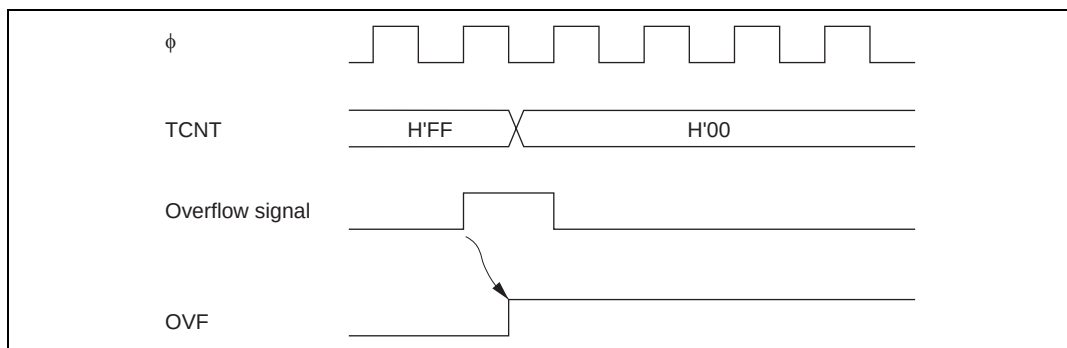


Figure 12.8 Timing of OVF Setting

Bit 5—A/D Start (ADST): Selects starting or stopping of A/D conversion. Holds a value of 1 during A/D conversion.

The ADST bit can be set to 1 by software, a timer conversion start trigger, or the A/D external trigger input pin ($\overline{\text{ADTRG}}$).

Bit 5

ADST	Description
0	A/D conversion stopped (Initial value)
1	- Single mode: A/D conversion is started. Cleared to 0 automatically when conversion on the specified channel ends - Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode

Bit 4—Scan Mode (SCAN): Selects single mode or scan mode as the A/D conversion operating mode. See section 16.4, Operation, for details of single mode and scan mode operation. Only set the SCAN bit while conversion is stopped (ADST = 0).

Bit 4

SCAN	Description
0	Single mode (Initial value)
1	Scan mode

Bit 3—Clock Select (CKS): Used together with the CKS1 bit in ADCR to set the A/D conversion time. Only change the conversion time while conversion is stopped (ADST = 0).

ADCR3 CKS1	Bit 3 CKS	Description
0	0	Conversion time = 530 states (max.)
	1	Conversion time = 68 states (max.)
1	0	Conversion time = 266 states (max.) (Initial value)
	1	Conversion time = 134 states (max.)

Bits 2 to 0—Channel Select 2 to 0 (CH2 to CH0): These bits are used together with the SCAN bit to select the analog input channels.

Only set the input channel(s) while conversion is stopped (ADST = 0).

19.15.2 User Program Mode

When set to user program mode, the chip can program and erase its flash memory by executing a user program/erase control program. Therefore, on-board reprogramming of the on-chip flash memory can be carried out by providing on-board means of FWE control and supply of programming data, and storing a program/erase control program in part of the program area as necessary.

To select user program mode, select a mode that enables the on-chip flash memory (mode 6 or 7), and apply a high level to the FWE pin. In this mode, on-chip supporting modules other than flash memory operate as they normally would in modes 6 and 7.

The flash memory itself cannot be read while the SWE bit is set to 1 to perform programming or erasing, so the control program that performs programming and erasing should be run in on-chip RAM or external memory. When the program is located in external memory, an instruction for programming the flash memory and the following instruction should be located in on-chip RAM.

Figure 19.40 shows the procedure for executing the program/erase control program when transferred to on-chip RAM.

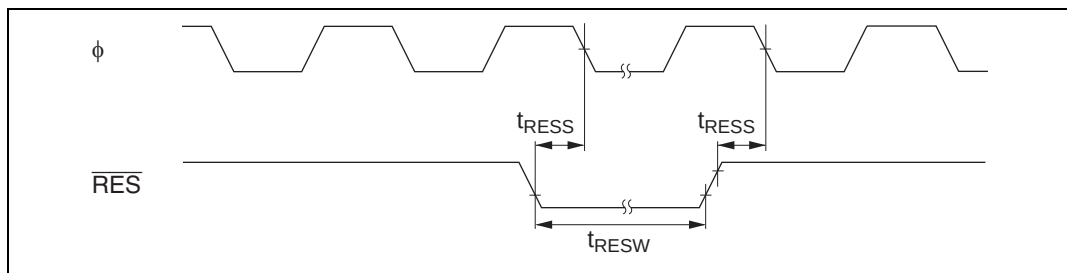


Figure 22.4 Reset Input Timing

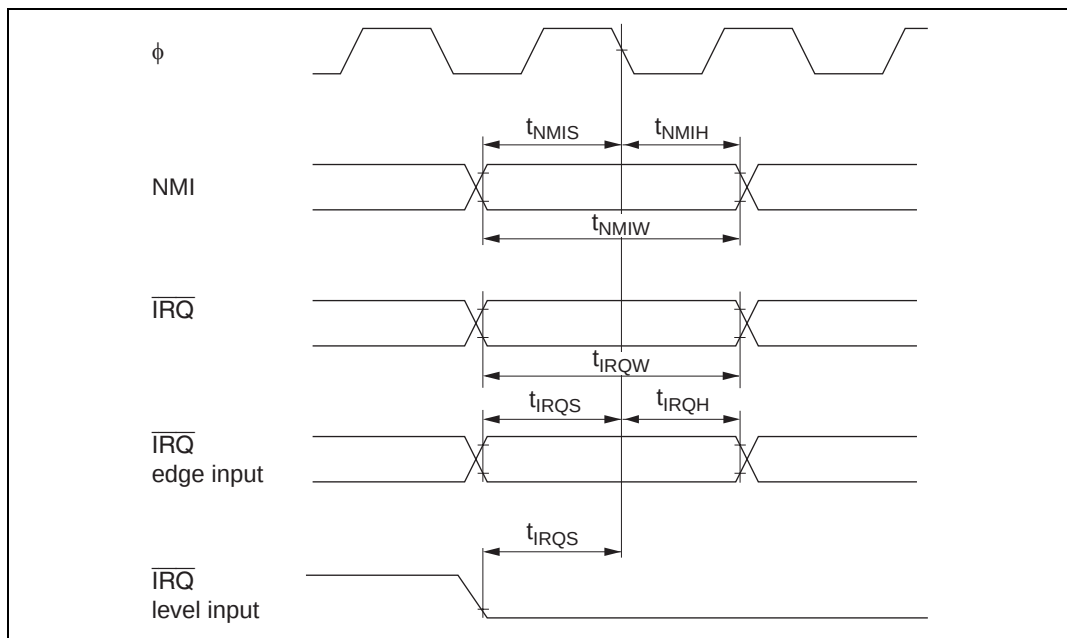


Figure 22.5 Interrupt Input Timing

TMDR4—Timer Mode Register 4

H'FE91

TPU4

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

Mode				
0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

* : Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

DTVECR—DTC Vector Register**H'FF37****DTC**

Bit	:	7	6	5	4	3	2	1	0
		SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0
Initial value :		0	0	0	0	0	0	0	0
Read/Write :		R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Sets vector number for DTC software activation

DTC Software Activation Enable

0	DTC software activation is disabled [Clearing conditions] • When the DISEL bit is 0 and the specified number of transfers have not ended • When SWDTEND is requested to the CPU, then 0 is written to the SWDTE bit
1	DTC software activation is enabled [Holding conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended • During data transfer due to software activation

Note: * DTVEC6 to DTVEC 0 bits can be written to when SWDTE = 0.

RDR0—Receive Data Register 0**H'FF7D SCI0, Smart Card Interface 0**

Bit	:	7	6	5	4	3	2	1	0
Initial value :		0	0	0	0	0	0	0	0
Read/Write :		R	R	R	R	R	R	R	R

Stores received serial data

SCMR0—Smart Card Mode Register 0**H'FF7E SCI0, Smart Card Interface 0**

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	SDIR	SINV	—	SMIF
Initial value :		1	1	1	1	0	0	1	0
Read/Write :		—	—	—	—	R/W	R/W	—	R/W

Smart Card
Interface Mode Select

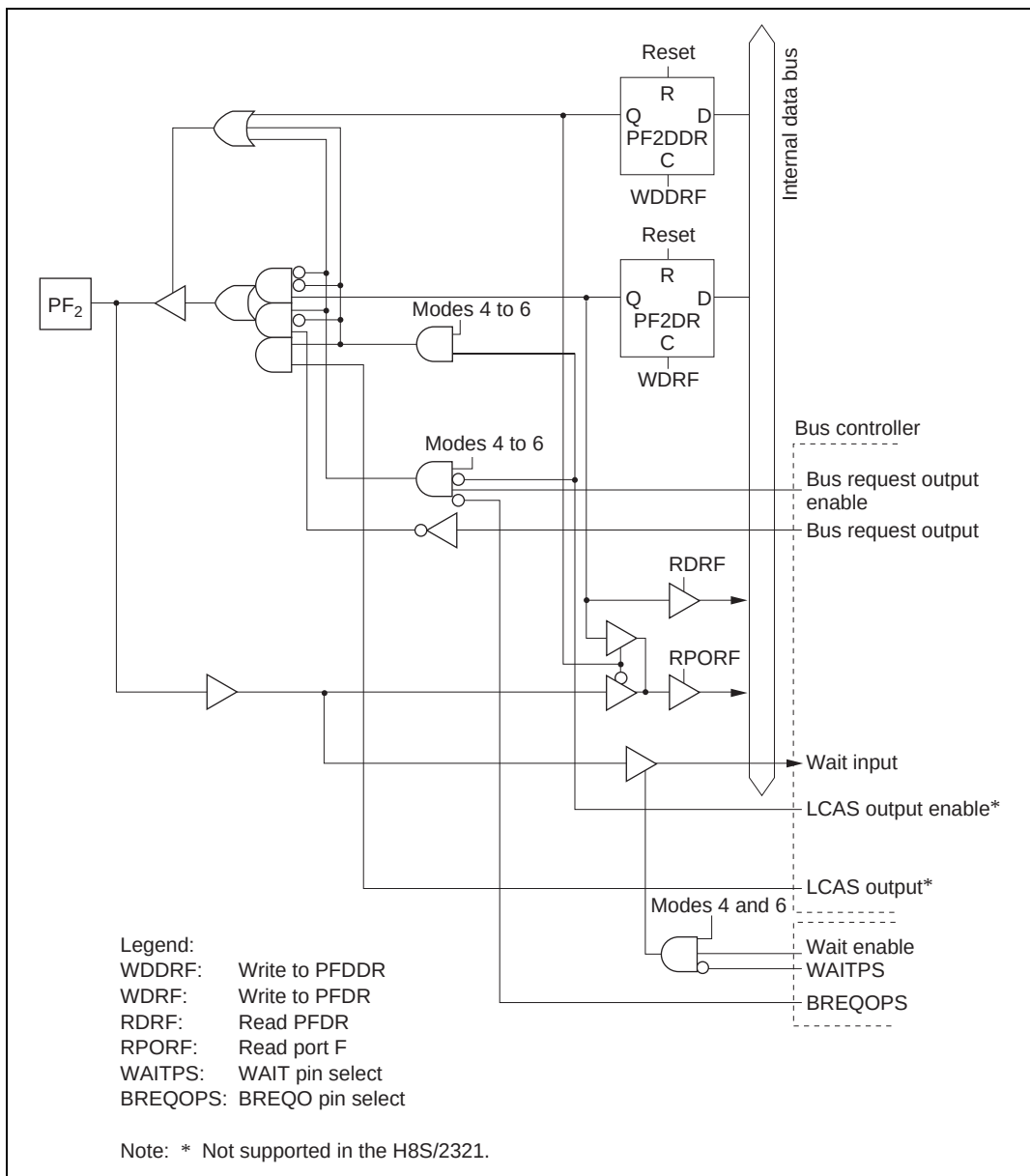
0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

Figure C.12 (c) Port F Block Diagram (Pin PF₂)