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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12321vf20v

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Bit 3 FLSHE	Description
0	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB (Initial value)
1	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB

Bits 2 and 1—Reserved: These bits are always read as 0. Only 0 should be written to these bits.

Bit 0—Reserved: In the H8S/2328B F-ZTAT and H8S/2326 F-ZTAT, this bit is always read as 0 and should only be written with 0. In the H8S/2329B F-ZTAT, this bit is reserved and should only be written with 0.

3.3 Operating Mode Descriptions

3.3.1 Mode 1

The H8S/2329 does not support mode 1. Do not select the mode 1 setting.

3.3.2 Mode 2 (H8S/2329B F-ZTAT Only)

This is a flash memory boot mode. See section 19, ROM, for details. This is the same as advanced on-chip ROM enabled expansion mode, except when erasing and reprogramming flash memory.

3.3.3 Mode 3 (H8S/2329B F-ZTAT Only)

This is a flash memory boot mode. See section 19, ROM, for details. This is the same as advanced single-chip ROM mode, except when erasing and reprogramming flash memory.

3.3.4 Mode 4 (Expanded Mode with On-Chip ROM Disabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Ports A, B, and C function as an address bus, port D functions as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. However, note that if 8-bit access is designated by the bus controller for all areas, the bus mode switches to 8 bits.

Port C Data Register (PCDR)

Bit	:	7	6	5	4	3	2	1	0
		PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCDR is an 8-bit readable/writable register that stores output data for the port C pins (PC_7 to PC_0).

PCDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port C Register (PORTC)

Bit	:	7	6	5	4	3	2	1	0
		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PC_7 to PC_0.

PORTC is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port C pins (PC_7 to PC_0) must always be performed on PCDR.

If a port C read is performed while PCDDR bits are set to 1, the PCDR values are read. If a port C read is performed while PCDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTC contents are determined by the pin states, as PCDDR and PCDR are initialized. PORTC retains its prior state in software standby mode.

Bit 1 TGIEB	Description	
0	Interrupt requests (TGIB) by TGFB disabled	(Initial value)
1	Interrupt requests (TGIB) by TGFB enabled	

Bit 0—TGR Interrupt Enable A (TGIEA): Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1.

Bit 0 TGIEA	Description	
0	Interrupt requests (TGIA) by TGFA disabled	(Initial value)
1	Interrupt requests (TGIA) by TGFA enabled	

10.2.5 Timer Status Registers (TSR)

Channel 0: TSR0

Channel 3: TSR3

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

Channel 1: TSR1

Channel 2: TSR2

Channel 4: TSR4

Channel 5: TSR5

Bit	:	7	6	5	4	3	2	1	0
		TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

Figure 10.27 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

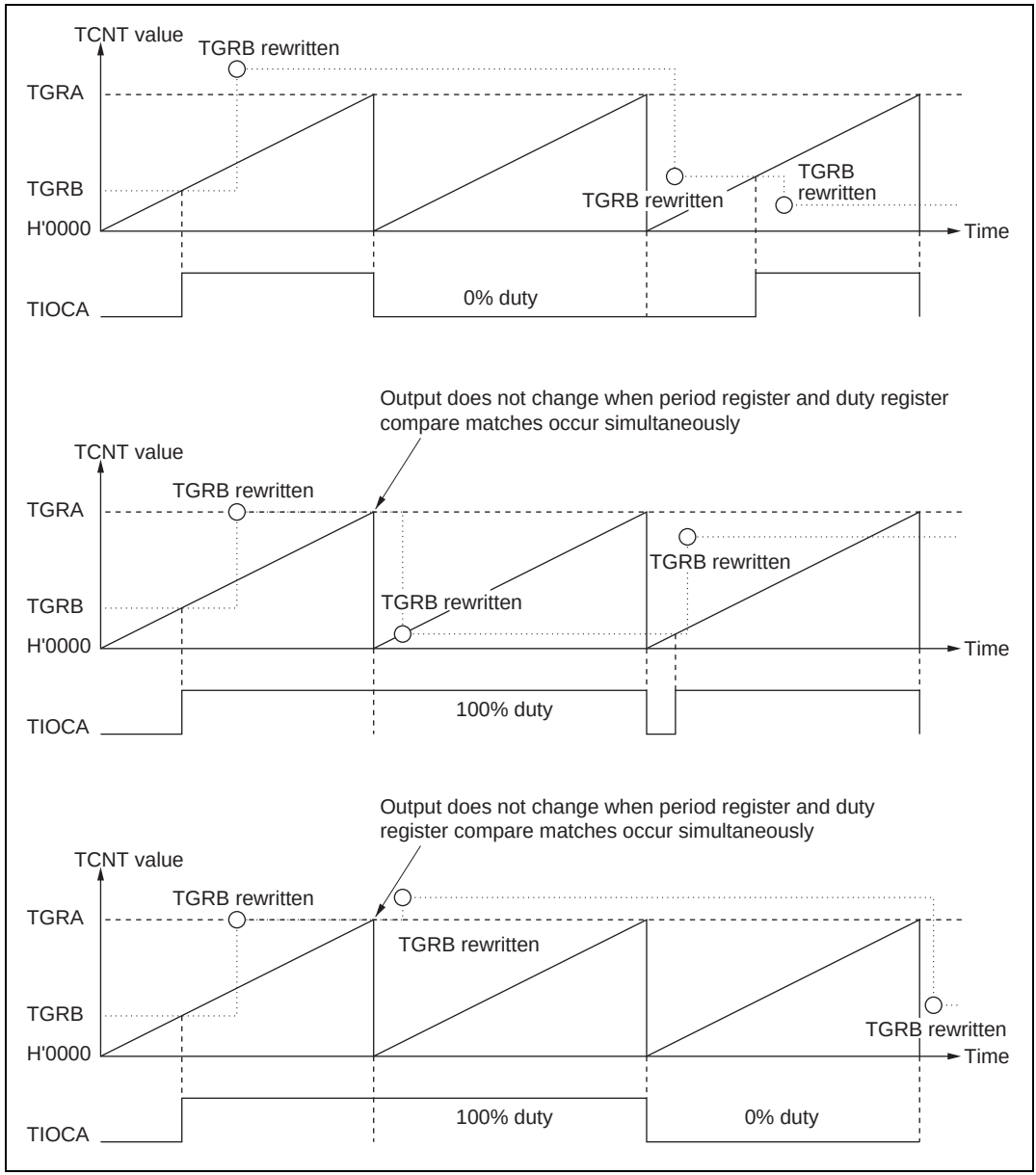


Figure 10.27 Examples of PWM Mode Operation (3)

15.3 Operation

15.3.1 Overview

The main functions of the smart card interface are as follows.

- One frame consists of 8-bit data plus a parity bit.
- In transmission, a guard time of at least 2 etu (1 etu in block transfer mode) (elementary time unit: the time for transfer of 1 bit) is left between the end of the parity bit and the start of the next frame.
- If a parity error is detected during reception, a low error signal level is output for one etu period, 10.5 etu after the start bit. (This does not apply to block transfer mode.)
- If the error signal is sampled during transmission, the same data is transmitted automatically after the elapse of 2 etu or longer. (This does not apply to block transfer mode.)
- Only asynchronous communication is supported; there is no synchronous communication function.

15.3.2 Pin Connections

Figure 15.2 shows a schematic diagram of smart card interface related pin connections.

In communication with an IC card, since both transmission and reception are carried out on a single data communication line, the chip's TxD pin and RxD pin should both be connected to the line, as shown in the figure. The data communication line should be pulled up to the V_{CC} power supply with a resistor.

When the clock generated on the smart card interface is used by an IC card, the SCK pin output is input to the CLK pin of the IC card. No connection is needed if the IC card uses an internal clock.

Chip port output is used as the reset signal.

Other pins must normally be connected to the power supply or ground.

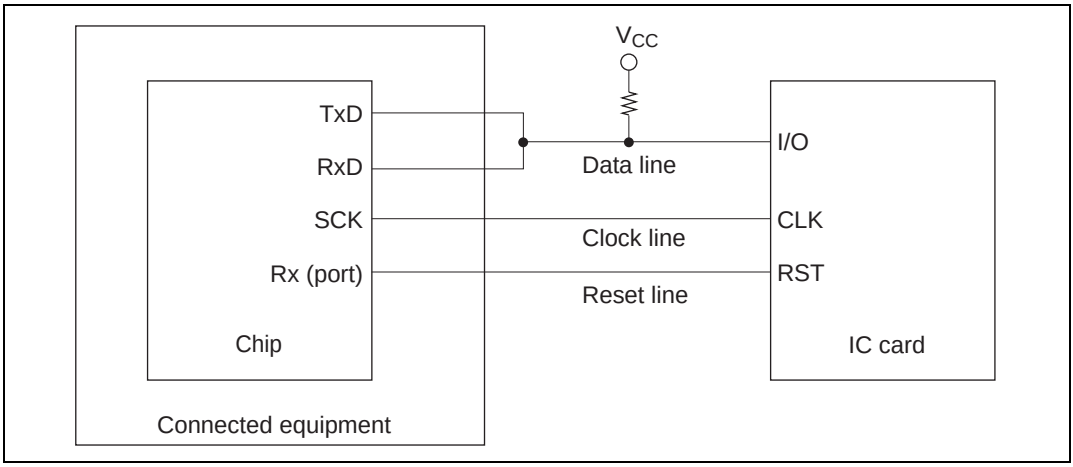
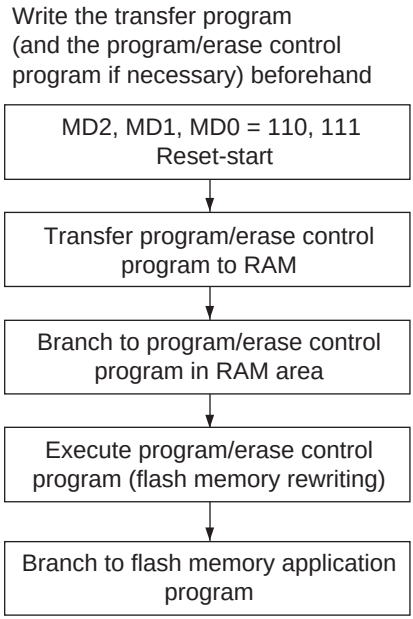


Figure 15.2 Schematic Diagram of Smart Card Interface Pin Connections

Note: If an IC card is not connected, and the TE and RE bits are both set to 1, closed transmission/reception is possible, enabling self-diagnosis to be carried out.

Figure 19.13 shows the procedure for executing the program/erase control program when transferred to on-chip RAM.



Note: The watchdog timer should be activated to prevent overprogramming or overerasing due to program runaway, etc.

Figure 19.13 User Program Mode Execution Procedure

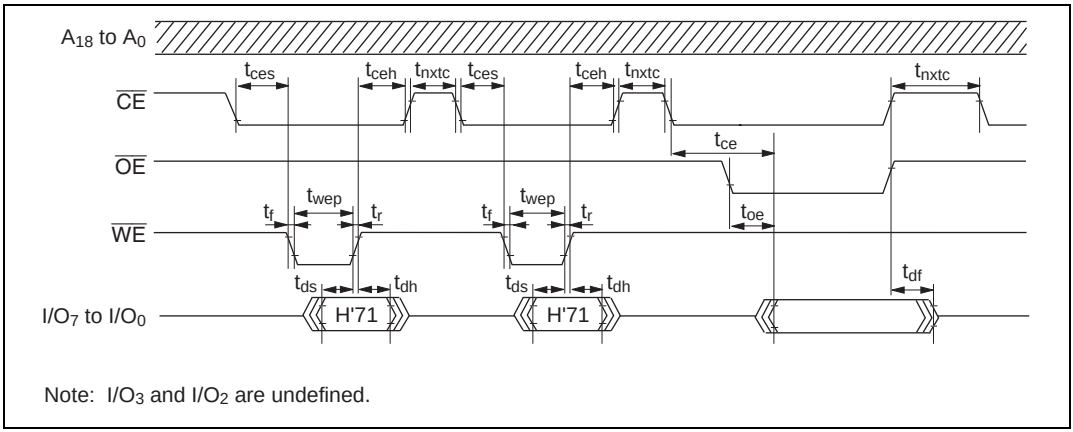


Figure 19.27 Status Read Mode Timing Waveforms

Table 19.22 Status Read Mode Return Commands

Pin Name	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Attribute	Normal end identification	Command error	Program-ming error	Erase error	—	—	Program-ming or erase count exceeded	Effective address error
Initial value	0	0	0	0	0	0	0	0
Indications	Normal end: 0 Abnormal end: 1	Command error: 1 Otherwise: 0	Program-ming error: 1 Otherwise: 0	Erase error: 1 Otherwise: 0	—	—	Count exceeded: 1 Otherwise: 0	Effective address error: 1 Otherwise: 0

Note: I/O_3 and I/O_2 are undefined.

19.13.7 Block Configuration

On-chip 256-kbyte flash memory is divided into three 64-kbyte blocks, one 32-kbyte block, and eight 4-kbyte blocks.

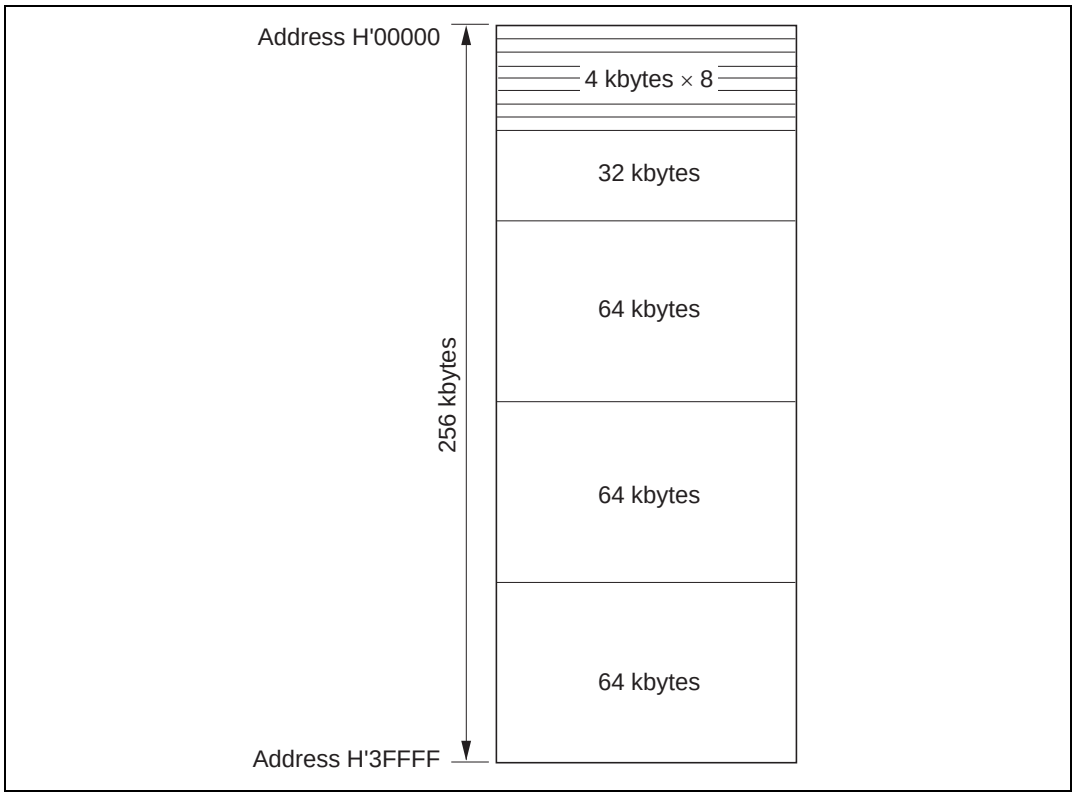


Figure 19.35 Flash Memory Block Configuration

19.22 Overview of Flash Memory (H8S/2326 F-ZTAT)

19.22.1 Features

The H8S/2326 F-ZTAT has 512 kbytes of on-chip flash memory. The features of the flash memory are summarized below.

- Four flash memory operating modes
  - Program mode
  - Erase mode
  - Program-verify mode
  - Erase-verify mode
- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erasing is performed by block erase (in single-block units). To erase the entire flash memory, the individual blocks must be erased sequentially. Block erasing can be performed as required on 4-kbyte, 32-kbyte, and 64-kbyte blocks.
- Programming/erase times

  The flash memory programming time is 10.0 ms (typ.) for simultaneous 128-byte programming, equivalent to 78 μs (typ.) per byte, and the erase time is 50 ms (typ.).
- Reprogramming capability

  The flash memory can be reprogrammed minimum 100 times.
- On-board programming modes

  There are two modes in which flash memory can be programmed/erased/verified on-board:
  - Boot mode
  - User program mode
- Automatic bit rate adjustment

  With data transfer in boot mode, the bit rate of the chip can be automatically adjusted to match the transfer bit rate of the host.
- Flash memory emulation by RAM

  Part of the RAM area can be overlapped onto flash memory, to emulate flash memory updates in real time.
- Protect modes

  There are three protect modes, hardware, software, and error protect, which allow protected status to be designated for flash memory program/erase/verify operations.

19.25 Programming/Erasing Flash Memory

In the on-board programming modes, flash memory programming and erasing is performed by software, using the CPU. There are four flash memory operating modes: program mode, erase mode, program-verify mode, and erase-verify mode. Transition to these modes can be made for addresses H'000000 to H'03FFFF by setting the PSU1, ESU1, P1, E1, PV1, and EV1 bits in FLMCR1, and for addresses H'040000 to H'07FFFF by setting the PSU2, ESU2, P2, E2, PV2, and EV2 bits in FLMCR2.

The flash memory cannot be read while being programmed or erased. Therefore, the program that controls flash memory programming/erasing (the programming control program) should be located and executed in on-chip RAM, external memory, or flash memory except for the above address areas. When the program is located in external memory, an instruction for programming the flash memory and the following instruction should be located in on-chip RAM. The DMAC or DTC should not be activated before or after the instruction for programming the flash memory is executed.

Notes: 1. Operation is not guaranteed if setting/resetting of the SWE1, ESU1, PSU1, EV1, PV1, E1, and P1 bits in FLMCR1 or setting/resetting of the SWE2, ESU2, PSU2, EV2, PV2, E2, and P2 bits in FLMCR2 is executed by a program in flash memory.
2. When programming or erasing, set FWE to 1 (programming/erasing is not performed when FWE = 0).
3. Perform programming in the erased state. Do not perform additional programming on previously programmed addresses.
4. Do not program addresses H'000000 to H'03FFFF and H'040000 to H'07FFFF simultaneously. Operation is not guaranteed when programming is performed simultaneously.

19.25.1 Program Mode (n = 1 for addresses H'000000 to H'03FFFF and n = 2 for addresses H'040000 to H'07FFFF)

Follow the procedure shown in the program/program-verify flowchart in figure 19.70 to write data or programs to flash memory. Performing program operations according to this flowchart will enable data or programs to be written to flash memory without subjecting the device to voltage stress or sacrificing program data reliability. Programming should be carried out 128 bytes at a time.

For the wait times (x, y, z1, z2, z3 α, ß, γ, ε, η, and θ) after bits are set or cleared in flash memory control register n (FLMCRn) and the maximum number of programming operations (N), see section 22.2.6, Flash Memory Characteristics.

Table 19.54 Software Protection

Item	Description	Functions	
		Program	Erase
SWE bit protection	• Clearing the SWE1 bit to 0 in FLMCR1 sets the program/erase-protected state for area H'000000 to H'03FFFF (Execute in on-chip RAM, external memory, or addresses H'040000 to H'07FFFF) • Clearing the SWE2 bit to 0 in FLMCR2 sets the program/erase-protected state for area H'040000 to H'07FFFF (Execute in on-chip RAM, external memory, or addresses H'000000 to H'03FFFF)	Yes	Yes
Block specification protection	• Erase protection can be set for individual blocks by settings in erase block registers 1 and 2 (EBR1, EBR2). • Setting EBR1 and EBR2 to H'00 places all blocks in the erase-protected state.	—	Yes
Emulation protection	• Setting the RAMS bit to 1 in the RAM emulation register (RAMER) places all blocks in the program/erase-protected state.	Yes	Yes

19.26.3 Error Protection

In error protection, an error is detected when MCU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

If the MCU malfunctions during flash memory programming/erasing, the FLER bit is set to 1 in FLMCR2 and the error protection state is entered. The FLMCR1, FLMCR2, EBR1, and EBR2 settings are retained, but program mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be re-entered by re-setting the P1, P2, E1, or E2 bit. However, PV1, PV2, EV1, and EV2 bit setting is enabled, and a transition can be made to verify mode.

20.4 Duty Adjustment Circuit

When the oscillator frequency is 5 MHz or higher, the duty adjustment circuit adjusts the duty cycle of the clock signal from the oscillator to generate the system clock (ϕ).

20.5 Medium-Speed Clock Divider

The medium-speed clock divider divides the system clock to generate ϕ/2, ϕ/4, ϕ/8, ϕ/16, and ϕ/32.

20.6 Bus Master Clock Selection Circuit

The bus master clock selection circuit selects the system clock (ϕ) or one of the medium-speed clocks (ϕ/2, ϕ/4, ϕ/8, ϕ/16, or ϕ/32) to be supplied to the bus master, according to the settings of the SCK2 to SCK0 bits in SCKCR.

(7) System Control Instructions

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes) #xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	|	Operation	Condition Code I	H	N	Z	V	C	No. of States*1 Advanced
TRAPA	TRAPA #xx:2	—										PC→@-SP,CCR→@-SP, EXR→@-SP,<vector>→PC	1	—	—	—	—	—	8 [9]
RTE	RTE	—										EXR←@SP+,CCR←@SP+, PC←@SP+	↕	↕	↕	↕	↕	↕	5 [9]
SLEEP	SLEEP	—										Transition to power-down state	—	—	—	—	—	—	2
LDC	LDC #xx:8,CCR	B	2									#xx:8→CCR	↕	↕	↕	↕	↕	↕	1
	LDC #xx:8,EXR	B	4									#xx:8→EXR	—	—	—	—	—	—	2
	LDC Rs,CCR	B		2								Rs8→CCR	↕	↕	↕	↕	↕	↕	1
	LDC Rs,EXR	B		2								Rs8→EXR	—	—	—	—	—	—	1
	LDC @ERs,CCR	W			4							@ERs→CCR	↕	↕	↕	↕	↕	↕	3
	LDC @ERs,EXR	W			4							@ERs→EXR	—	—	—	—	—	—	3
	LDC @(d:16,ERs),CCR	W				6						@(d:16,ERs)→CCR	↕	↕	↕	↕	↕	↕	4
	LDC @(d:16,ERs),EXR	W				6						@(d:16,ERs)→EXR	—	—	—	—	—	—	4
	LDC @(d:32,ERs),CCR	W				10						@(d:32,ERs)→CCR	↕	↕	↕	↕	↕	↕	6
	LDC @(d:32,ERs),EXR	W				10						@(d:32,ERs)→EXR	—	—	—	—	—	—	6
	LDC @ERs+,CCR	W					4					@ERs→CCR,ERs32+2→ERs32	↕	↕	↕	↕	↕	↕	4
	LDC @ERs+,EXR	W					4					@ERs→EXR,ERs32+2→ERs32	—	—	—	—	—	—	4
	LDC @aa:16,CCR	W						6				@aa:16→CCR	↕	↕	↕	↕	↕	↕	4
	LDC @aa:16,EXR	W						6				@aa:16→EXR	—	—	—	—	—	—	4
	LDC @aa:32,CCR	W						8				@aa:32→CCR	↕	↕	↕	↕	↕	↕	5
	LDC @aa:32,EXR	W						8				@aa:32→EXR	—	—	—	—	—	—	5

A.2 Instruction Codes

Table A.2 shows the instruction codes.

Instruction	1	2	3	4	5	6	7	8	9
STC EXR,@(d:16,ERd)	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC CCR,@(d:32,ERd)	R:W 2nd	R:W 3rd	R:W 4th	R:W 5th	R:W NEXT	W:W EA			
STC EXR,@(d:32,ERd)	R:W 2nd	R:W 3rd	R:W 4th	R:W 5th	R:W NEXT	W:W EA			
STC CCR,@–ERd	R:W 2nd	R:W NEXT	Internal operation, 1 state	W:W EA					
STC EXR,@–ERd	R:W 2nd	R:W NEXT	Internal operation, 1 state	W:W EA					
STC CCR,@aa:16	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC EXR,@aa:16	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC CCR,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:W NEXT	W:W EA				
STC EXR,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:W NEXT	W:W EA				
STM.L(ERn–ERn+1),@–SP	R:W 2nd	R:W:M NEXT	Internal operation, 1 state	W:W:M stack (H)*3	W:W stack (L)*3				
STM.L(ERn–ERn+2),@–SP	R:W 2nd	R:W:M NEXT	Internal operation, 1 state	W:W:M stack (H)*3	W:W stack (L)*3				
STM.L(ERn–ERn+3),@–SP	R:W 2nd	R:W:M NEXT	Internal operation, 1 state	W:W:M stack (H)*3	W:W stack (L)*3				
STMAC MACH,ERd	Cannot be used in the chip								
STMAC MACL,ERd									
SUB.B Rs,Rd	R:W NEXT								
SUB.W #xx:16,Rd	R:W 2nd	R:W NEXT							
SUB.W Rs,Rd	R:W NEXT								
SUB.L #xx:32,ERd	R:W 2nd	R:W 3rd	R:W NEXT						
SUB.L ERs,ERd	R:W NEXT								
SUBS #1/2/4,ERd	R:W NEXT								
SUBX #xx:8,Rd	R:W NEXT								
SUBX Rs,Rd	R:W NEXT								
TAS @ERd*8	R:W 2nd	R:W NEXT	R:B:M EA	W:B EA					
TRAPA #x:2 Advanced	R:W NEXT	Internal operation, 1 state	W:W stack (L)	W:W stack (H)	W:W stack (EXR)	R:W:M VEC	R:W VEC+2	Internal operation, 1 state	R:W*7
XOR.B #xx8,Rd	R:W NEXT								
XOR.B Rs,Rd	R:W NEXT								
XOR.W #xx:16,Rd	R:W 2nd	R:W NEXT							
XOR.W Rs,Rd	R:W NEXT								
XOR.L #xx:32,ERd	R:W 2nd	R:W 3rd	R:W NEXT						

PORTG—Port G Register **H'FF5F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	—	—	PG4	PG3	PG2	PG1	PG0
Initial value	Undefined	Undefined	Undefined	—*	—*	—*	—*	—*
Read/Write	—	—	—	R	R	R	R	R

State of port G pins

Note: * Determined by the state of pins PG_4 to PG_0.

P1DR—Port 1 Data Register **H'FF60** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 1 pins ($P1_7$ to $P1_0$)

P2DR—Port 2 Data Register **H'FF61** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 2 pins ($P2_7$ to $P2_0$)

TSR0—Timer Status Register 0 H'FFD5 TPU0

Bit	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC*1 is activated by TGIA interrupt while DTA bit of DMABCR in DMAC*1 is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Note: 1. The DMAC is not supported in the H8S/2321.

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Input Capture/Output Compare Flag C

0	[Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Input Capture/Output Compare Flag D

0	[Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Note: * Can only be written with 0 for flag clearing.

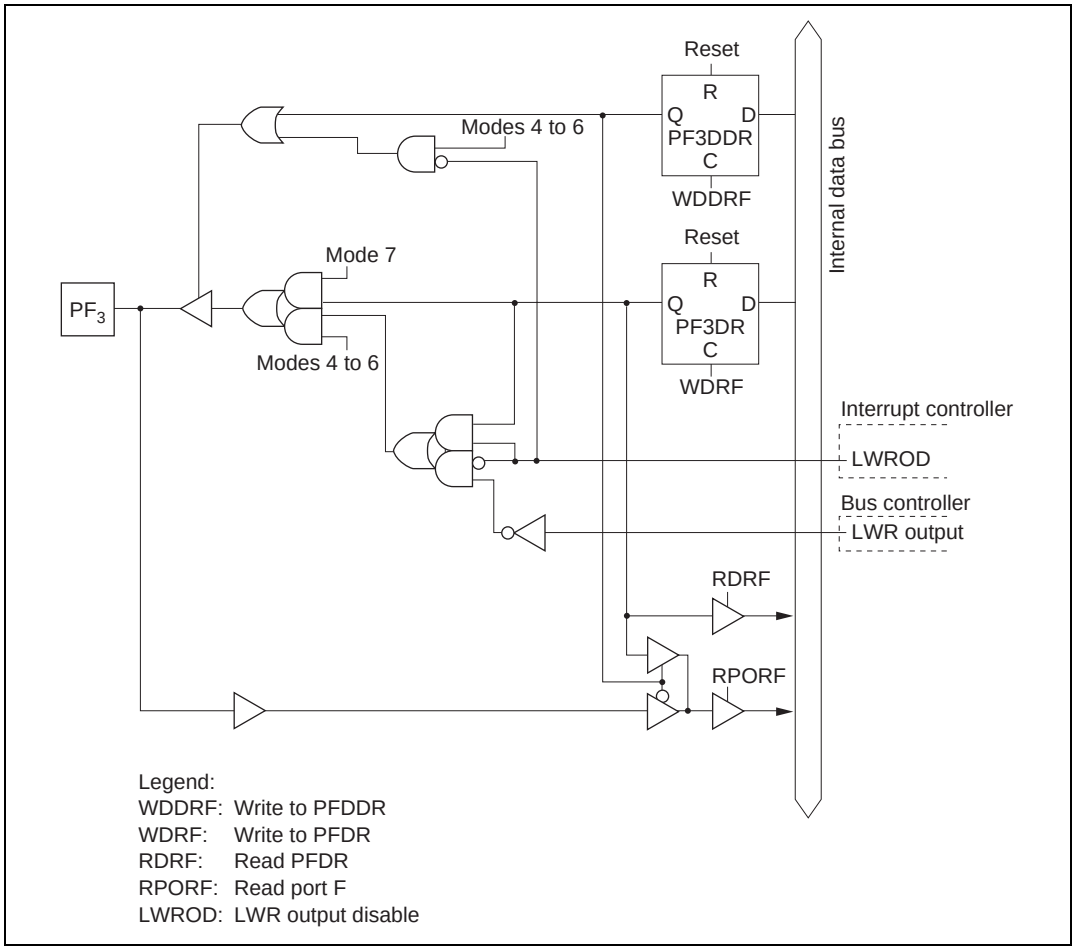


Figure C.12 (d) Port F Block Diagram (Pin PF_3)