Renesas - D12321VF25V Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12321vf25v

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.1.3 Register Configuration

The H8S/2329 Group and H8S/2328 Group have a mode control register (MDCR) that indicates the inputs at the mode pins (MD_2 to MD_0), and a system control register (SYSCR) and a system control register 2 (SYSCR2)*2 that control the operation of the chip. Table 3.3 summarizes these registers.

Table 3.3 Registers

Name	Abbreviation	R/W	Initial Value	Address*1
Mode control register	MDCR	R	Undefined	H'FF3B
System control register	SYSCR	R/W	H'01	H'FF39
System control register 2*2	SYSCR2	R/W	H'00	H'FF42

Notes: 1. Lower 16 bits of the address.

2. The SYSCR2 register can only be used in the F-ZTAT versions. In the mask ROM and ROMless versions this register will return an undefined value if read, and cannot be modified.

3.2 Register Descriptions

3.2.1 Mode Control Register (MDCR)

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value :	1	0	0	0	0	—*	—*	—*
R/W :	—	—	—	—	—	R	R	R

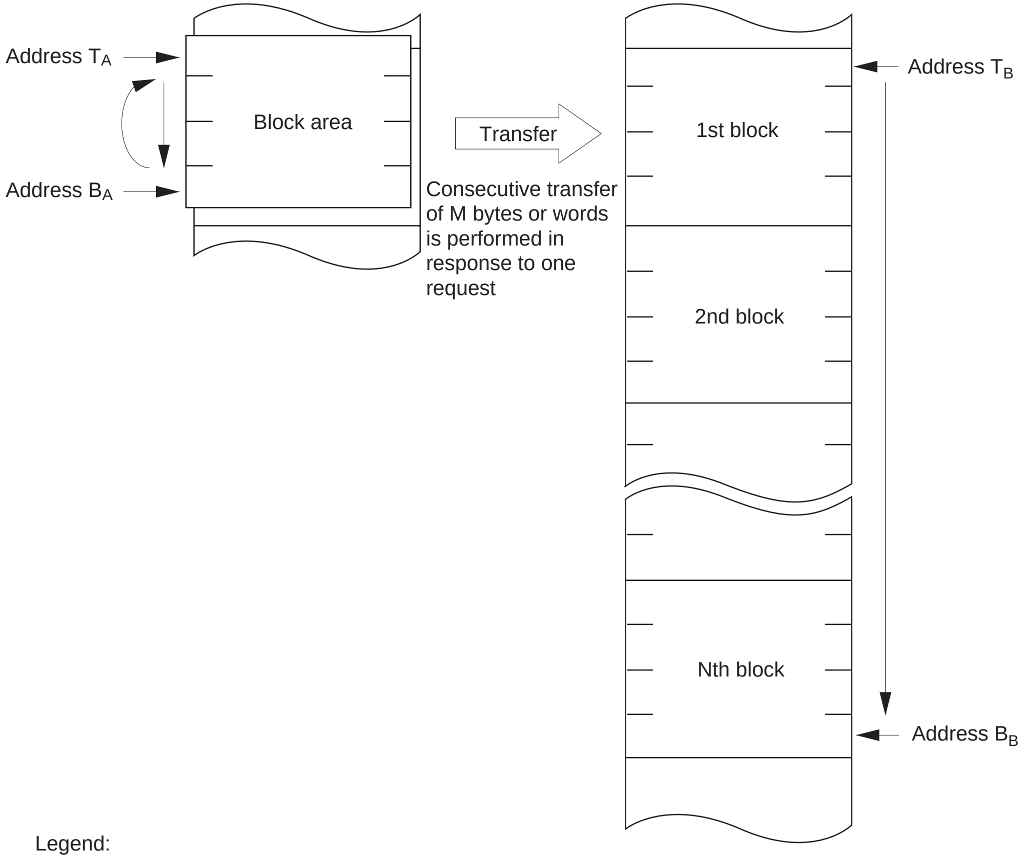
Note: * Determined by pins MD_2 to MD_0.

MDCR is an 8-bit read-only register that indicates the current operating mode of the H8S/2329 Group and H8S/2328 Group chip.

Bit 7—Reserved: This bit is always read as 1, and cannot be modified.

Bits 6 to 3—Reserved: These bits are always read as 0, and cannot be modified.

Bits 2 to 0—Mode Select 2 to 0 (MDS2 to MDS0): These bits indicate the input levels at pins MD_2 to MD_0 (the current operating mode). Bits MDS2 to MDS0 correspond to pins MD_2 to MD_0. MDS2 to MDS0 are read-only bits, and cannot be written to. The mode pin (MD_2 to MD_0) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.



Legend:
Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \cdot (-1)^{SAID} \cdot (2^{DTSZ} \cdot (N-1))$
Address $B_B = L_B + DAIDE \cdot (-1)^{DAID} \cdot (2^{DTSZ} \cdot (M \cdot N-1))$
Where : L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRB
M = Value set in ETCRAH and ETCRAL

Figure 7.14 Operation in Block Transfer Mode (BLKDIR = 1)

ETCRAL is decremented by 1 each time a byte or word transfer is performed. In response to a single transfer request, burst transfer is performed until the value in ETCRAL reaches H'00. ETCRAL is then loaded with the value in ETCRAH. At this time, the value in the MAR register for which a block designation has been given by the BLKDIR bit in DMACRA is restored in accordance with the DTSZ, SAID/DAID, and SAIDE/DAIDE bits in DMACR.

Write Data Buffer Function: When the WDBE bit of BCRL in the bus controller is set to 1, enabling the write data buffer function, dual address transfer external write cycles or single address transfers and internal accesses (on-chip memory or internal I/O registers) are executed in parallel.

- Write Data Buffer Function and DMAC Register Setting

  If the setting of a register that controls external accesses is changed during execution of an external access by means of the write data buffer function, the external access may not be performed normally. Registers that control external accesses should only be manipulated when external reads, etc., are used with DMAC operation disabled, and the operation is not performed in parallel with external access.

- Write Data Buffer Function and DMAC Operation Timing

  The DMAC can start its next operation during external access using the write data buffer function. Consequently, the $\overline{\text{DREQ}}$ pin sampling timing, $\overline{\text{TEND}}$ output timing, etc., are different from the case in which the write data buffer function is disabled. Also, internal bus cycles maybe hidden, and not visible.

- Write Data Buffer Function and $\overline{\text{TEND}}$ Output

  A low level is not output at the $\overline{\text{TEND}}$ pin if the bus cycle in which a low level is to be output at the $\overline{\text{TEND}}$ pin is an internal bus cycle, and an external write cycle is executed in parallel with this cycle. Note, for example, that a low level may not be output at the $\overline{\text{TEND}}$ pin if the write data buffer function is used when data transfer is performed between an internal I/O register and on-chip memory.

  If at least one of the DMAC transfer addresses is an external address, a low level is output at the $\overline{\text{TEND}}$ pin.

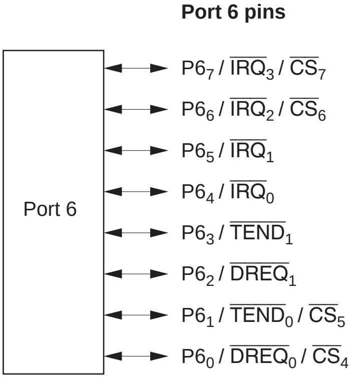
  Figure 7.42 shows an example in which a low level is not output at the $\overline{\text{TEND}}$ pin.

9.7 Port 6

9.7.1 Overview

Port 6 is an 8-bit I/O port. Port 6 pins also function as interrupt input pins ($\overline{IRQ}_0$ to $\overline{IRQ}_3$), DMAC* I/O pins ($\overline{DREQ}_0$, $\overline{TEND}_0$, $\overline{DREQ}_1$, and $\overline{TEND}_1$), and bus control output pins ($\overline{CS}_4$ to $\overline{CS}_7$). The functions of pins $P6_5$ to $P6_2$ are the same in all operating modes, while the functions of pins $P6_7$, $P6_6$, $P6_1$, and $P6_0$ change according to the operating mode. Switching of $\overline{CS}_4$ to $\overline{CS}_7$ output can be performed by setting PFCR2. Pins $P6_7$ to $P6_4$ are Schmitt-triggered inputs. Figure 9.6 shows the port 6 pin configuration.

Note: * The DMAC is not supported in the H8S/2321.



Pin functions in modes 4 to 6

$P6_7$ (I/O) / $\overline{IRQ}_3$ (input) / $\overline{CS}_7$ (output)

$P6_6$ (I/O) / $\overline{IRQ}_2$ (input) / $\overline{CS}_6$ (output)

$P6_5$ (I/O) / $\overline{IRQ}_1$ (input)

$P6_4$ (I/O) / $\overline{IRQ}_0$ (input)

$P6_3$ (I/O) / $\overline{TEND}_1$* (output)

$P6_2$ (I/O) / $\overline{DREQ}_1$* (input)

$P6_1$ (I/O) / $\overline{TEND}_0$* (output) / $\overline{CS}_5$ (output)

$P6_0$ (I/O) / $\overline{DREQ}_0$* (input) / $\overline{CS}_4$ (output)

Pin functions in mode 7

$P6_7$ (I/O) / $\overline{IRQ}_3$ (input)

$P6_6$ (I/O) / $\overline{IRQ}_2$ (input)

$P6_5$ (I/O) / $\overline{IRQ}_1$ (input)

$P6_4$ (I/O) / $\overline{IRQ}_0$ (input)

$P6_3$ (I/O) / $\overline{TEND}_1$* (output)

$P6_2$ (I/O) / $\overline{DREQ}_1$* (input)

$P6_1$ (I/O) / $\overline{TEND}_0$* (output)

$P6_0$ (I/O) / $\overline{DREQ}_0$* (input)

Note: * The $\overline{TEND}_1$, $\overline{DREQ}_1$, $\overline{TEND}_0$, and $\overline{DREQ}_0$ pin functions are not supported in the H8S/2321.

Figure 9.6 Port 6 Pin Functions

Contention between TCNT Write and Overflow/Underflow: If there is an up-count or down-count in the T_2 state of a TCNT write cycle, and overflow/underflow occurs, the TCNT write takes precedence and the TCFV/TCFU flag in TSR is not set.

Figure 10.57 shows the operation timing when there is contention between TCNT write and overflow.

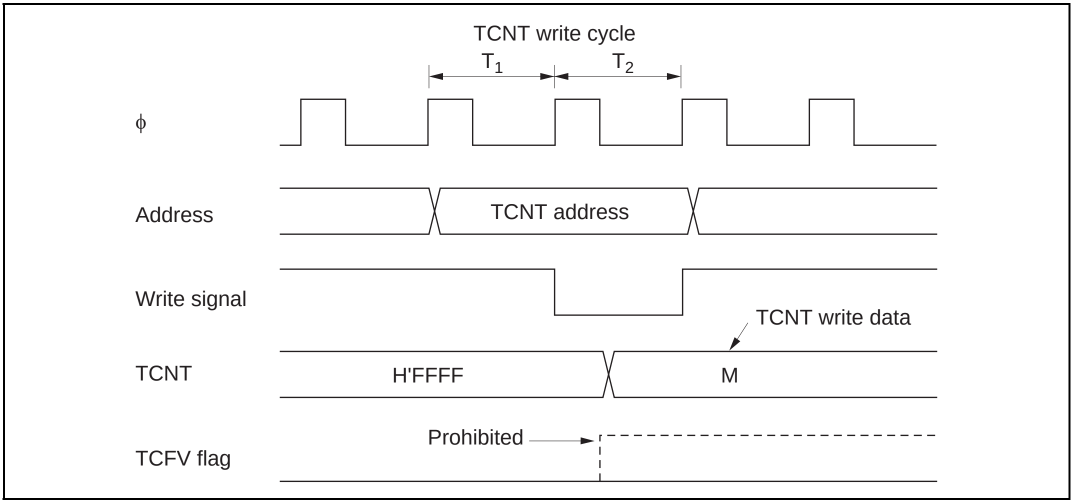


Figure 10.57 Contention between TCNT Write and Overflow

Multiplexing of I/O Pins: In the chip, the TCLKA input pin is multiplexed with the TIOCC0 I/O pin, the TCLKB input pin with the TIOCD0 I/O pin, the TCLKC input pin with the TIOCB1 I/O pin, and the TCLKD input pin with the TIOCB2 I/O pin. When an external clock is input, compare match output should not be performed from a multiplexed pin.

Interrupts and Module Stop Mode: If module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DMAC* or DTC activation source. Interrupts should therefore be disabled before entering module stop mode.

Note: * The DMAC is not supported in the H8S/2321.

Bit 6 WT/$\overline{\text{IT}}$	Description
0	Interval timer: Sends the CPU an interval timer interrupt request (WOVI) when TCNT overflows (Initial value)
1	Watchdog timer: Generates the $\overline{\text{WDTOVF}}$ signal[*1] when TCNT overflows[*2]

Notes: 1. The $\overline{\text{WDTOVF}}$ pin function cannot be used in the F-ZTAT versions.

2. For details of the case where TCNT overflows in watchdog timer mode, see section 13.2.3, Reset Control/Status Register (RSTCSR).

Bit 5—Timer Enable (TME): Selects whether TCNT runs or is halted.

Bit 5 TME	Description
0	TCNT is initialized to H'00 and halted (Initial value)
1	TCNT counts

Bits 4 and 3—Reserved: These bits cannot be modified and are always read as 1.

Bits 2 to 0—Clock Select 2 to 0 (CKS2 to CKS0): These bits select one of eight internal clock sources, obtained by dividing the system clock (ϕ), for input to TCNT.

			Description	
Bit 2 CKS2	Bit 1 CKS1	Bit 0 CKS0	Clock	Overflow Period (when ϕ = 20 MHz)*
0	0	0	ϕ/2 (Initial value)	25.6 µs
		1	ϕ/64	819.2 µs
	1	0	ϕ/128	1.6 ms
		1	ϕ/512	6.6 ms
1	0	0	ϕ/2048	26.2 ms
		1	ϕ/8192	104.9 ms
	1	0	ϕ/32768	419.4 ms
		1	ϕ/131072	1.68 s

Note: * The overflow period is the time from when TCNT starts counting up from H'00 until overflow occurs.

- Full-duplex communication capability
  - The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously
  - Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data
- Choice of LSB-first or MSB-first transfer
  - Can be selected regardless of the communication mode*[1] (except in the case of asynchronous mode 7-bit data)
- Built-in baud rate generator allows any bit rate to be selected
- Choice of serial clock source: internal clock from baud rate generator or external clock from SCK pin
- Four interrupt sources
  - Four interrupt sources—transmit-data-empty, transmit-end, receive-data-full, and receive error—that can issue requests independently
  - The transmit-data-empty and receive-data-full interrupts can activate the DMA controller (DMAC)*[2] or data transfer controller (DTC) to execute data transfer
- Module stop mode can be set
  - As the initial setting, SCI operation is halted. Register access is enabled by exiting module stop mode

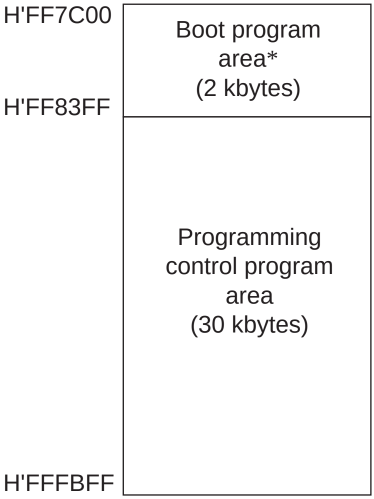
Notes: 1. Descriptions in this section refer to LSB-first transfer.
2. The DMAC is not supported in the H8S/2321.

Table 14.12 SCI Interrupt Sources

Channel	Interrupt Source	Description	DTC Activation	DMAC[*2] Activation	Priority[*1]
0	ERI	Interrupt due to receive error (ORER, FER, or PER)	Not possible	Not possible	High
	RXI	Interrupt due to receive data full state (RDRF)	Possible	Possible	
	TXI	Interrupt due to transmit data empty state (TDRE)	Possible	Possible	
	TEI	Interrupt due to transmission end (TEND)	Not possible	Not possible	
1	ERI	Interrupt due to receive error (ORER, FER, or PER)	Not possible	Not possible	
	RXI	Interrupt due to receive data full state (RDRF)	Possible	Possible	
	TXI	Interrupt due to transmit data empty state (TDRE)	Possible	Possible	
	TEI	Interrupt due to transmission end (TEND)	Not possible	Not possible	
2	ERI	Interrupt due to receive error (ORER, FER, or PER)	Not possible	Not possible	
	RXI	Interrupt due to receive data full state (RDRF)	Possible	Not possible	
	TXI	Interrupt due to transmit data empty state (TDRE)	Possible	Not possible	
	TEI	Interrupt due to transmission end (TEND)	Not possible	Not possible	Low

Notes: 1. This table shows the initial state immediate after a reset. Relative priorities among channels can be changed by the interrupt controller.
2. The DMAC is not supported in the H8S/2321.

A TEI interrupt is requested when the TEND flag is set to 1 while the TEIE bit is set to 1. The TEND flag is cleared at the same time as the TDRE flag. Consequently, if a TEI interrupt and a TXI interrupt are requested simultaneously, the TXI interrupt may be accepted first, with the result that the TDRE and TEND flags are cleared. Note that the TEI interrupt will not be accepted in this case.



Note: * The boot program area cannot be used until a transition is made to the execution state for the programming control program transferred to RAM. Note that the boot program remains stored in this area after a branch is made to the programming control program.

Figure 19.12 RAM Areas in Boot Mode

Notes on Use of Boot Mode

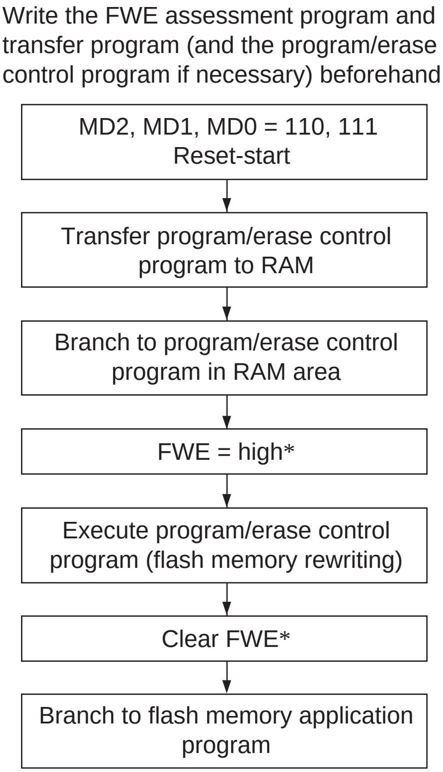
- When the chip comes out of reset in boot mode, it measures the low-level period of the input at the SCI's RxD1 pin. The reset should end with RxD1 high. After the reset ends, it takes approximately 100 states before the chip is ready to measure the low-level period of the RxD1 pin.

- In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.

- Interrupts cannot be used while the flash memory is being programmed or erased.

- The RxD1 and TxD1 pins should be pulled up on the board.

- Before branching to the programming control program (RAM area H'FF8400 to H'FFFBFF), the chip terminates transmit and receive operations by the on-chip SCI (channel 1) (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. The transmit data output pin, TxD1, goes to the high-level output state (P31DDR = 1, P31DR = 1).



Notes: Do not apply a constant high level to the FWE pin. Apply a high level to the FWE pin only when the flash memory is programmed or erased. Also, while a high level is applied to the FWE pin, the watchdog timer should be activated to prevent overprogramming or overerasing due to program runaway, etc.

* For further information on FWE application and disconnection, see section 19.21, Flash Memory Programming and Erasing Precautions.

Figure 19.40 User Program Mode Execution Procedure

19.20 Flash Memory PROM Mode

19.20.1 PROM Mode Setting

Programs and data can be written and erased in PROM mode as well as in the on-board programming modes. In PROM mode, the on-chip ROM can be freely programmed using a PROM programmer that supports the Renesas microcomputer device type with 256-kbyte on-chip flash memory (FZTAT256V3A). Flash memory read mode, auto-program mode, auto-erase mode, and status read mode are supported with this device type. In auto-program mode, auto-erase mode, and status read mode, a status polling procedure is used, and in status read mode, detailed internal signals are output after execution of an auto-program or auto-erase operation.

Table 19.34 shows PROM mode pin settings.

Table 19.34 PROM Mode Pin Settings

Pin Names	Settings/External Circuit Connection
Mode pins: MD2, MD1, MD0	Low-level input
Mode setting pins: P66, P65, P64	High-level input to P66, low-level input to P65 and P64
FWE pin	High-level input (in auto-program and auto-erase modes)
$\overline{\text{STBY}}$ pin	High-level input (do not select hardware standby mode)
$\overline{\text{RES}}$ pin	Reset circuit
XTAL, EXTAL pins	Oscillator circuit
Other pins requiring setting: P32, P25	High-level input to P32, low-level input to P25

Bit 2—Program-Verify 1 (PV1): Selects program-verify mode transition or clearing for addresses H'000000 to H'03FFFF. Do not set the SWE1, ESU1, PSU1, EV1, E1, or P1 bit at the same time.

Bit 2 PV1	Description	
0	Program-verify mode cleared	(Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1, SWE1 = 1	

Bit 1—Erase 1 (E1): Selects erase mode transition or clearing for addresses H'000000 to H'03FFFF. Do not set the SWE1, ESU1, PSU1, EV1, PV1, or P1 bit at the same time.

Bit 1 E1	Description	
0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE1 = 1, and ESU1 = 1	

Bit 0—Program 1 (P1): Selects program mode transition or clearing for addresses H'000000 to H'03FFFF. Do not set the SWE1, PSU1, ESU1, EV1, PV1, or E1 bit at the same time.

Bit 0 P1	Description	
0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE1 = 1, and PSU1 = 1	

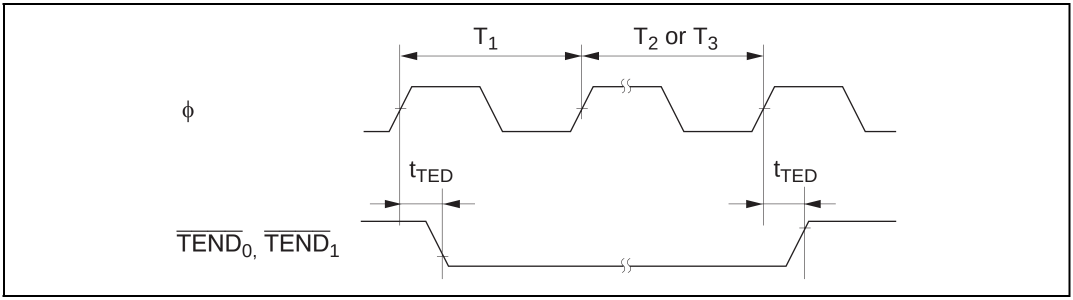


Figure 22.18 DMAC $\overline{\text{TEND}}$ Output Timing

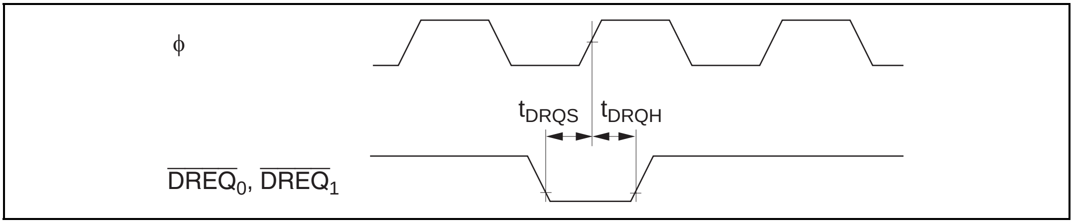


Figure 22.19 DMAC $\overline{\text{DREQ}}$ Input Timing

				Condition A		Condition B			Test Conditions
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 22.28
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure 22.29
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 22.30

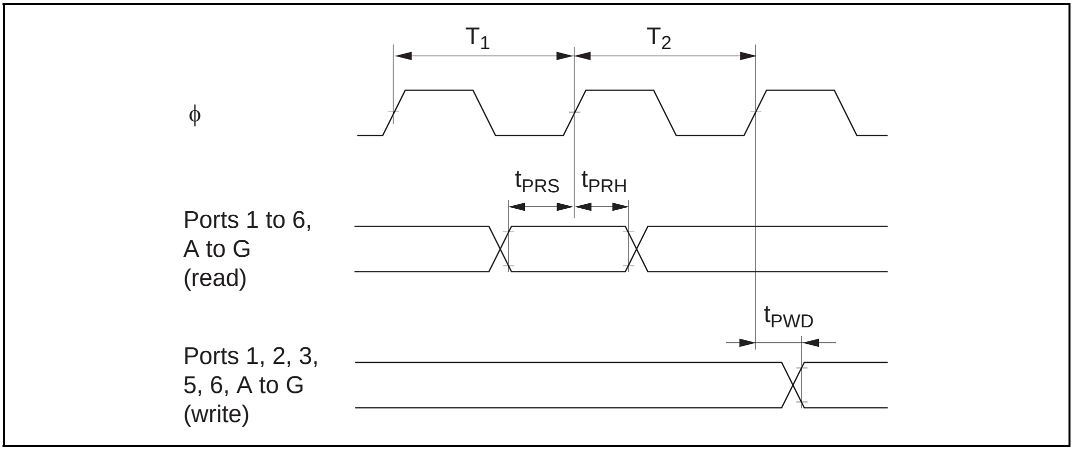


Figure 22.20 I/O Port Input/Output Timing

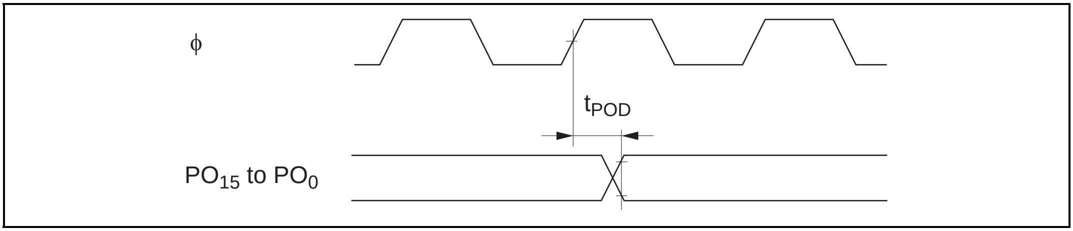


Figure 22.21 PPG Output Timing

22.2.2 DC Characteristics

Table 22.13 DC Characteristics

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $P6_4$ to $P6_7$ PA_4 to PA_7 Port 5 (when using $\overline{\text{IRQ}}$)	V_T^-	V_{CC} × 0.2	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7	V	
		$V_T^+ – V_T^-$	V_{CC} × 0.07	—	—	V	
Input high voltage	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, NMI, MD_2 to MD_0,, FWE*2, EMLE*3	V_{IH}	V_{CC} × 0.9	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.7	—	V_{CC} + 0.3	V	
	Ports 3, 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 03	V	
Input low voltage	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, MD_2 to MD_0, FWE*2, EMLE*3	V_{IL}	–0.3	—	V_{CC} × 0.1	V	
	NMI, EXTAL, Ports 3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	V_{CC} × 0.2	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{\text{RES}}$	$\| I_{in} \|$	—	—	10.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{\text{STBY}}$, NMI, MD_2 to MD_0, FWE*2, EMLE*3		—	—	1.0	µA	
	Port 4		—	—	1.0	µA	V_{in} = 0.5 V to AV_{CC} – 0.5 V

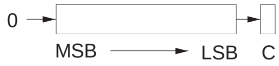
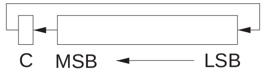
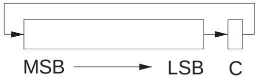
Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@−ERn/@ERn+	@aa	@(d,PC)	@@aa	—		I	H	N	Z	V	C	Advanced
SHLR	SHLR.B Rd	B		2								 0 MSB → LSB C	—	—	0	↕	0	↕	1
	SHLR.B #2,Rd	B		2									—	—	0	↕	0	↕	1
	SHLR.W Rd	W		2									—	—	0	↕	0	↕	1
	SHLR.W #2,Rd	W		2									—	—	0	↕	0	↕	1
	SHLR.L ERd	L		2									—	—	0	↕	0	↕	1
	SHLR.L #2,ERd	L		2									—	—	0	↕	0	↕	1
ROTXL	ROTXL.B Rd	B		2								 C MSB ← LSB	—	—	↕	↕	0	↕	1
	ROTXL.B #2,Rd	B		2									—	—	↕	↕	0	↕	1
	ROTXL.W Rd	W		2									—	—	↕	↕	0	↕	1
	ROTXL.W #2,Rd	W		2									—	—	↕	↕	0	↕	1
	ROTXL.L ERd	L		2									—	—	↕	↕	0	↕	1
	ROTXL.L #2,ERd	L		2									—	—	↕	↕	0	↕	1
ROTXR	ROTXR.B Rd	B		2								 MSB → LSB C	—	—	↕	↕	0	↕	1
	ROTXR.B #2,Rd	B		2									—	—	↕	↕	0	↕	1
	ROTXR.W Rd	W		2									—	—	↕	↕	0	↕	1
	ROTXR.W #2,Rd	W		2									—	—	↕	↕	0	↕	1
	ROTXR.L ERd	L		2									—	—	↕	↕	0	↕	1
	ROTXR.L #2,ERd	L		2									—	—	↕	↕	0	↕	1

Table A.3 Operation Code Map (3)

Instruction code

1st byte		2nd byte		3rd byte		4th byte	
AH	AL	BH	BL	CH	CL	DH	DL

Instruction when most significant bit of DH is 0.
Instruction when most significant bit of DH is 1.

AH AL BH BL CH \ CL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
01C05	MULXS		MULXS													
01D05		DIVXS		DIVXS												
01F06					OR	XOR	AND									
7Cr06 *1				BTST												
7Cr07 *1				BTST	BOR BIOR	BXOR BIXOR	BAND BIAND	BLD BILD								
7Dr06 *1	BSET	BNOT	BCLR					BST BIST								
7Dr07 *1	BSET	BNOT	BCLR													
7Eaa6 *2				BTST												
7Eaa7 *2				BTST	BOR BIOR	BXOR BIXOR	BAND BIAND	BLD BILD								
7Faa6 *2	BSET	BNOT	BCLR					BST BIST								
7Faa7 *2	BSET	BNOT	BCLR													

Notes: 1. r is the register specification field.
2. aa is the absolute address specification.

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF78	SMR0	C/$\overline{A}$/ GM*7	CHR/ BLK*8	PE	O/$\overline{E}$	STOP/ BCP1*9	MP/ BCP0*10	CKS1	CKS0	SCI0, smart card interface 0	8 bits
H'FF79	BRR0										
H'FF7A	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF7B	TDR0										
H'FF7C	SSR0	TDRE	RDRF	ORER	FER/ ERS*11	PER	TEND	MPB	MPBT		
H'FF7D	RDR0										
H'FF7E	SCMR0	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF80	SMR1	C/$\overline{A}$/ GM*7	CHR/ BLK*8	PE	O/$\overline{E}$	STOP/ BCP1*9	MP/ BCP0*10	CKS1	CKS0	SCI1, smart card interface 1	8 bits
H'FF81	BRR1										
H'FF82	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF83	TDR1										
H'FF84	SSR1	TDRE	RDRF	ORER	FER/ ERS*11	PER	TEND	MPB	MPBT		
H'FF85	RDR1										
H'FF86	SCMR1	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF88	SMR2	C/$\overline{A}$/ GM*7	CHR/ BLK*8	PE	O/$\overline{E}$	STOP/ BCP1*9	MP/ BCP0*10	CKS1	CKS0	SCI2, smart card interface 2	8 bits
H'FF89	BRR2										
H'FF8A	SCR2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF8B	TDR2										
H'FF8C	SSR2	TDRE	RDRF	ORER	FER/ ERS*11	PER	TEND	MPB	MPBT		
H'FF8D	RDR2										
H'FF8E	SCMR2	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF90	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter	8 bits
H'FF91	ADDRAL	AD1	AD0	—	—	—	—	—	—		
H'FF92	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF93	ADDRBL	AD1	AD0	—	—	—	—	—	—		
H'FF94	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF95	ADDRCL	AD1	AD0	—	—	—	—	—	—		
H'FF96	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF97	ADDRDL	AD1	AD0	—	—	—	—	—	—		
H'FF98	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0		
H'FF99	ADCR	TRGS1	TRGS0	—	—	CKS1	CH3	—	—		
H'FFA4	DADR0									D/A converter	8 bits
H'FFA5	DADR1										
H'FFA6	DACR01	DAOE1	DAOE0	DAE	—	—	—	—	—		

ADCSR—A/D Control/Status Register H'FF98 A/D Converter

Bit :	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/(W)[*1]	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel Select

Note: These bits select the analog input channels. Ensure that conversion is halted (ADST = 0) before making a channel selection.

Group Selection	Channel Selection		Single Mode (SCAN = 0)	Scan Mode (SCAN = 1)
CH2	CH1	CH0		
0	0	0	AN_0 (Initial value)	AN_0
		1	AN_1	AN_0, AN_1
	1	0	AN_2	AN_0 to AN_2
		1	AN_3	AN_0 to AN_3
1	0	0	AN_4	AN_4
		1	AN_5	AN_4, AN_5
	1	0	AN_6	AN_4 to AN_6
		1	AN_7	AN_4 to AN_7

Clock Select

Note: CKS is used in combination with bit 3 (CKS1) of ADCR.
See ADCR—A/D Control Register
H'FF99 A/D Converter.

Scan Mode

0	Single mode
1	Scan mode

A/D Start

0	A/D conversion stopped
1	• Single mode: A/D conversion is started. Cleared to 0 automatically when conversion ends • Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or transition to standby mode or module stop mode

A/D Interrupt Enable

0	A/D conversion end interrupt request disabled
1	A/D conversion end interrupt request enabled

A/D End Flag

0	[Clearing conditions] • When 0 is written to the ADF flag after reading ADF = 1 • When the DMAC[*2] or DTC is activated by an ADI interrupt, and ADDR is read
1	[Setting conditions] • Single mode: When A/D conversion ends • Scan mode: When A/D conversion ends on all specified channels

Notes: 1. Can only be written with 0 for flag clearing.
2. The DMAC is not supported in the H8S/2321.

Port Name Pin Name	**MCU Operating Mode**	**Reset**	**Hardware Standby Mode**	**Software Standby Mode**	**Bus-Released State**	**Program Execution State Sleep Mode**
$\overline{\text{PG}_0}$/$\overline{\text{CAS}}^{*3}$	4 to 6	T	T	[DRAME^{*4} = 0] kept [DRAME^{*4} · $\overline{\text{OPE}}$ = 1] T [DRAME^{*4} · OPE = 1] $\overline{\text{CAS}}^{*3}$	T	[DRAME^{*4} = 0] Input port [DRAME^{*4} = 1] $\overline{\text{CAS}}^{*3}$
	7	T	T	kept	kept	I/O port

Legend:

H: High level

L: Low level

T: High impedance

kept: Input port becomes high-impedance, output port retains state

DDR: Data direction register

OPE: Output port enable

WAITE: Wait input enable

WAITPS: WAIT pin select

BRLE: Bus release enable

BREQOE: BREQO pin enable

BREQOPS: BREQO pin select

DRAME: DRAM space setting

LCASE: DRAM space setting, 16-bit access setting

AnE: Address n enable (n = 23 to 21)

A20E: Address 20 enable

ASOD: AS output disable

CS167E: CS167 enable

CS25E: CS25 enable

LWROD: LWR output disable

Notes:
1. $\overline{\text{LCAS}}$ is not supported in the H8S/2321.
2. As the DRAM interface is not supported in the H8S/2321, LCASE is always 0.
3. $\overline{\text{CAS}}$ is not supported in the H8S/2321.
4. As the DRAM interface is not supported in the H8S/2321, DRAME is always 0.
5. The $\overline{\text{WDTOVF}}$ pin function is not usable on the F-ZTAT version.
6. A low level is output if a WDT overflow occurs while WT/IT is set to 1.