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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12322rvf20v

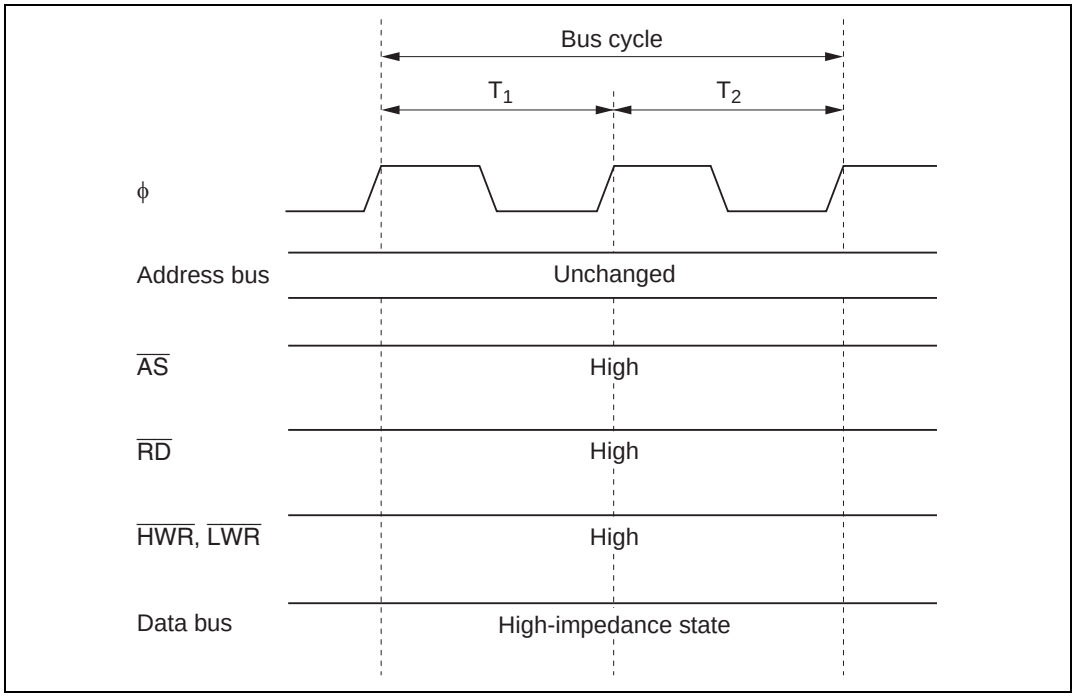

Figure 2.17 Pin States during On-Chip Supporting Module Access

2.9.4 External Address Space Access Timing

The external address space is accessed with an 8-bit or 16-bit data bus width in a two-state or three-state bus cycle. In three-state access, wait states can be inserted. For further details, refer to section 6, Bus Controller.

2.10 Usage Note

2.10.1 TAS Instruction

Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction. The TAS instruction is not generated by the Renesas H8S and H8/300 Series C/C++ compilers. If the TAS instruction is used as a user-defined intrinsic function, ensure that only register ER0, ER1, ER4, or ER5 is used.

6.2.7 DRAM Control Register (DRAMCR)

Bit	:	7	6	5	4	3	2	1	0
		RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DRAMCR is an 8-bit readable/writable register that selects the DRAM refresh mode and refresh counter clock, and controls the refresh timer.

DRAMCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Note: In the H8S/2321 this register is reserved and must not be accessed.

Bit 7—Refresh Control (RFSHE): Selects whether or not refresh control is performed. When refresh control is not performed, the refresh timer can be used as an interval timer.

Bit 7 RFSHE	Description	
0	Refresh control is not performed	(Initial value)
1	Refresh control is performed	

Bit 6—RAS-CAS Wait (RCW): Controls wait state insertion in DRAM interface CAS-before-RAS refreshing.

Bit 6 RCW	Description	
0	Wait state insertion in CAS-before-RAS refreshing disabled $\overline{RAS}$ falls in T_{Rr} cycle	(Initial value)
1	One wait state inserted in CAS-before-RAS refreshing $\overline{RAS}$ falls in T_{Rc1} cycle	

Bit 5—Refresh Mode (RMODE): When refresh control is performed (RFSHE = 1), selects whether or not self-refresh control is performed in software standby mode.

Bit 5 RMODE	Description	
0	Self-refreshing is not performed in software standby mode	(Initial value)
1	Self-refreshing is performed in software standby mode	

6.6 DMAC Single Address Mode and DRAM Interface (Not supported in the H8S/2321)

When burst mode is selected with the DRAM interface, the $\overline{\text{DACK}}$ output timing can be selected with the DDS bit. When DRAM space is accessed in DMAC single address mode at the same time, this bit selects whether or not burst access is to be performed.

6.6.1 When DDS = 1

Burst access is performed by determining the address only, irrespective of the bus master. The $\overline{\text{DACK}}$ output goes low from the T_{C1} state in the case of the DRAM interface.

Figure 6.28 shows the $\overline{\text{DACK}}$ output timing for the DRAM interface when DDS = 1.

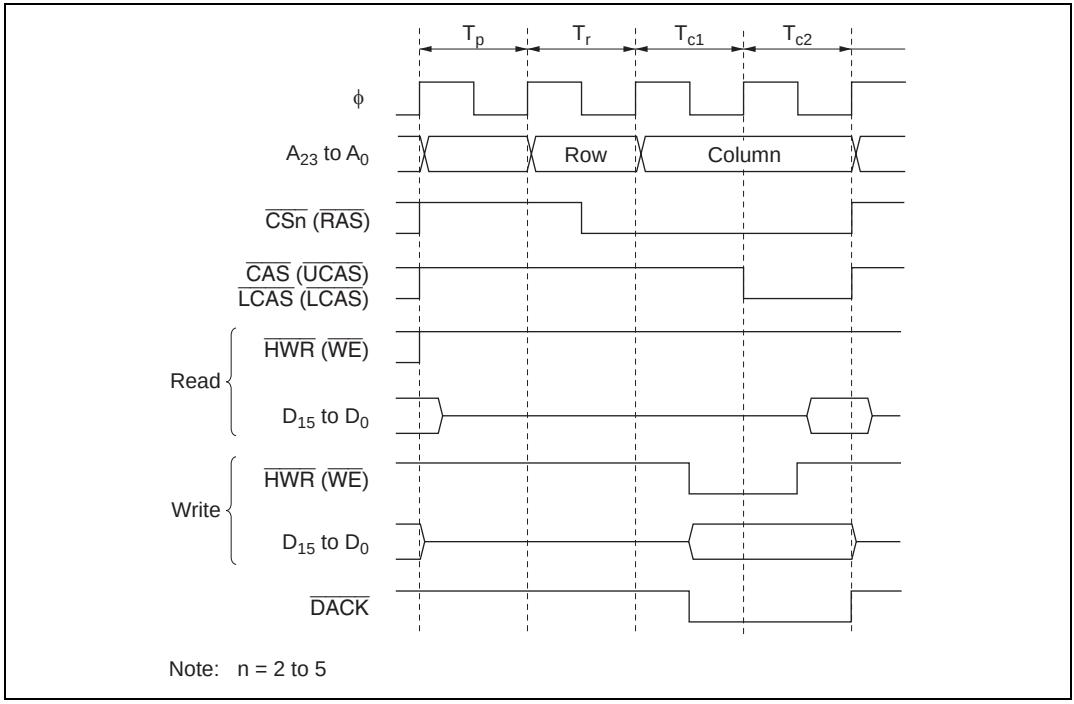

Figure 6.28 $\overline{\text{DACK}}$ Output Timing when DDS = 1 (Example of DRAM Access)

7.3.3 Execute Transfer Count Register (ETCR)

ETCR is a 16-bit readable/writable register that specifies the number of transfers. The function of this register is different in normal mode and in block transfer mode.

ETCR is not initialized by a reset or in standby mode.

Normal Mode

ETCRA

Transfer Counter

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined

In normal mode, ETCRA functions as a 16-bit transfer counter. ETCRA is decremented by 1 each time a transfer is performed, and transfer ends when the count reaches H'0000. ETCRB is not used at this time.

ETCRB

ETCRB is not used in normal mode.

Figure 7.34 shows an example of single address transfer using the write data buffer function. In this example, the CPU program area is in on-chip memory.

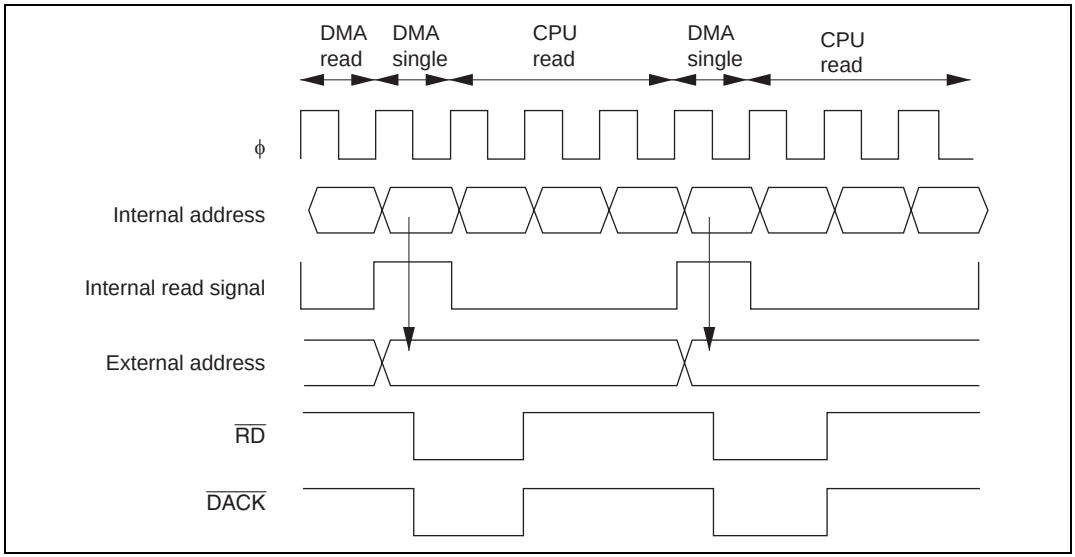

Figure 7.34 Example of Single Address Transfer Using Write Data Buffer Function

When the write data buffer function is activated, the DMAC recognizes that the bus cycle concerned has ended, and starts the next operation. Therefore, $\overline{\text{DREQ}}$ pin sampling is started one state after the start of the DMA write cycle or single address transfer.

7.5.13 DMAC Multi-Channel Operation

The DMAC channel priority order is: channel 0 > channel 1, and channel A > channel B. Table 7.13 summarizes the priority order for DMAC channels.

Table 7.13 DMAC Channel Priority Order

Short Address Mode	Full Address Mode	Priority
Channel 0A	Channel 0	High
Channel 0B		↑
Channel 1A	Channel 1	
Channel 1B		Low

Pin	Selection Method and Pin Functions

$P1_1/PO_9/TIOCB_0/\overline{DACK_1}$*2

The pin function is switched as shown below according to the combination of the TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOB3 to IOB0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit NDER9 in NDERH, bit SAE1*2 in DMABCRH, and bit P11DDR.

SAE1*2	0				1
TPU Channel 0 Setting	Table Below (1)	Table Below (2)			
P11DDR	—	0	1	1	—
NDER9	—	—	0	1	—
Pin function	$TIOCB_0$ output	$P1_1$ input	$P1_1$ output	PO_9 output	$\overline{DACK_1}$*2 output
		$TIOCB_0$ input*1			

Notes: 1. $TIOCB_0$ input when MD3 to MD0 = B'0000, and IOB3 to IOB0 = B'10xx.

2. The DMAC and the $\overline{DACK_1}$ pin function are not supported in the H8S/2321.

TPU Channel 0 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
$P1_0/PO_8/TIOCA_0/\overline{DACK}_0$*2	The pin function is switched as shown below according to the combination of the TPU channel 0 setting (by bits MD3 to MD0 in TMDR0, bits IOA3 to IOA0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit NDER8 in NDERH, bit SAE0*2 in DMABCRH, and bit P10DDR.

SAE0*2	0				1
TPU Channel 0 Setting	Table Below (1)	Table Below (2)			—
P10DDR	—	0	1	1	—
NDER8	—	—	0	1	—
Pin function	$TIOCA_0$ output	$P1_0$ input	$P1_0$ output	PO_8 output	$\overline{DACK}_0$*2 output
		$TIOCA_0$ input*1			

TPU Channel 0 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR2 to CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM mode 1 output*3	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_0$ input when MD3 to MD0 = B'0000, and IOA3 to IOA0 = B'10xx.
2. The DMAC and the $\overline{DACK}_0$ pin function are not supported in the H8S/2321.
3. $TIOCB_0$ output is disabled.

9.6.2 Register Configuration

Table 9.9 shows the port 5 register configuration.

Table 9.9 Port 5 Registers

Name	Abbreviation	R/W	Initial Value	Address*1
Port 5 data direction register	P5DDR	W	H'0*2	H'FEB4
Port 5 data register	P5DR	R/W	H'0*2	H'FF64
Port 5 register	PORT5	R	Undefined	H'FF54
Port function control register 2	PFCR2	R/W	H'30	H'FFAC
System control register	SYSCR	R/W	H'01	H'FF39

Notes: 1. Lower 16 bits of the address.
2. Value of bits 3 to 0.

Port 5 Data Direction Register (P5DDR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR
Initial value	:	Undefined	Undefined	Undefined	Undefined	0	0	0	0
R/W	:	—	—	—	—	W	W	W	W

P5DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 5. Bits 7 to 4 are reserved. P5DDR cannot be read; if it is, an undefined value will be read.

Setting a P5DDR bit to 1 makes the corresponding port 5 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P5DDR is initialized to H'0 (bits 3 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode. As the SCI is initialized, the pin states are determined by the P5DDR and P5DR specifications.

Port B Data Register (PBDR)

Bit	:	7	6	5	4	3	2	1	0
		PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBDR is an 8-bit readable/writable register that stores output data for the port B pins (PB_7 to PB_0). PBDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port B Register (PORTB)

Bit	:	7	6	5	4	3	2	1	0
		PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PB_7 to PB_0.

PORTB is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port B pins (PB_7 to PB_0) must always be performed on PBDR.

If a port B read is performed while PBDDR bits are set to 1, the PBDR values are read. If a port B read is performed while PBDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTB contents are determined by the pin states, as PBDDR and PBDR are initialized. PORTB retains its prior state in software standby mode.

Contention between TCNT Write and Clear Operations: If the counter clear signal is generated in the T_2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed.

Figure 10.49 shows the timing in this case.

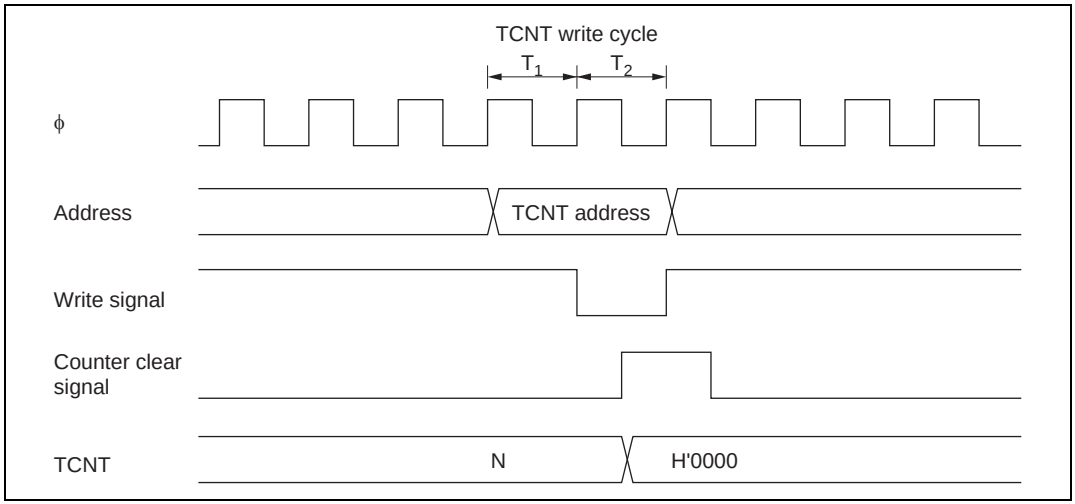

Figure 10.49 Contention between TCNT Write and Clear Operations

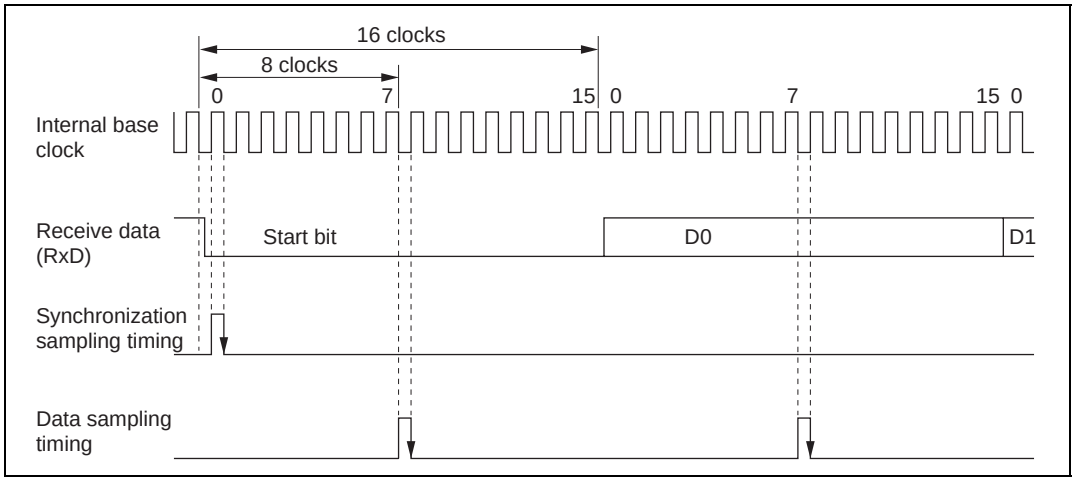

Figure 14.21 Receive Data Sampling Timing in Asynchronous Mode

Thus the receive margin in asynchronous mode is given by formula (1) below.

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)\,F - \frac{|D - 0.5|}{N}\,(1 + F) \right| \times 100\% \quad \text{... Formula (1)}$$

Where M : Receive margin (%)
N : Ratio of bit rate to clock (N = 16)
D : Clock duty (D = 0 to 1.0)
L : Frame length (L = 9 to 12)
F : Absolute value of clock rate deviation

Assuming values of F = 0 and D = 0.5 in formula (1), a receive margin of 46.875% is given by formula (2) below.

When D = 0.5 and F = 0,

$$M = \left(0.5 - \frac{1}{2 \times 16}\right) \times 100\%$$

$$= 46.875\% \quad \text{... Formula (2)}$$

However, this is a theoretical value, and a margin of 20% to 30% should be allowed in system design.

Serial Data Reception (Except Block Transfer Mode): Data reception in smart card mode uses the same processing procedure as for the normal SCI. Figure 15.7 shows an example of the transmission processing flow.

[1] Perform smart card interface mode initialization as described above in Initialization.

[2] Check that the ORER flag and PER flag in SSR are cleared to 0. If either is set, perform the appropriate receive error handling, then clear both the ORER and the PER flag to 0.

[3] Repeat steps [2] and [3] until it can be confirmed that the RDRF flag is set to 1.

[4] Read the receive data from RDR.

[5] When receiving data continuously, clear the RDRF flag to 0 and go back to step [2].

[6] To end reception, clear the RE bit to 0.

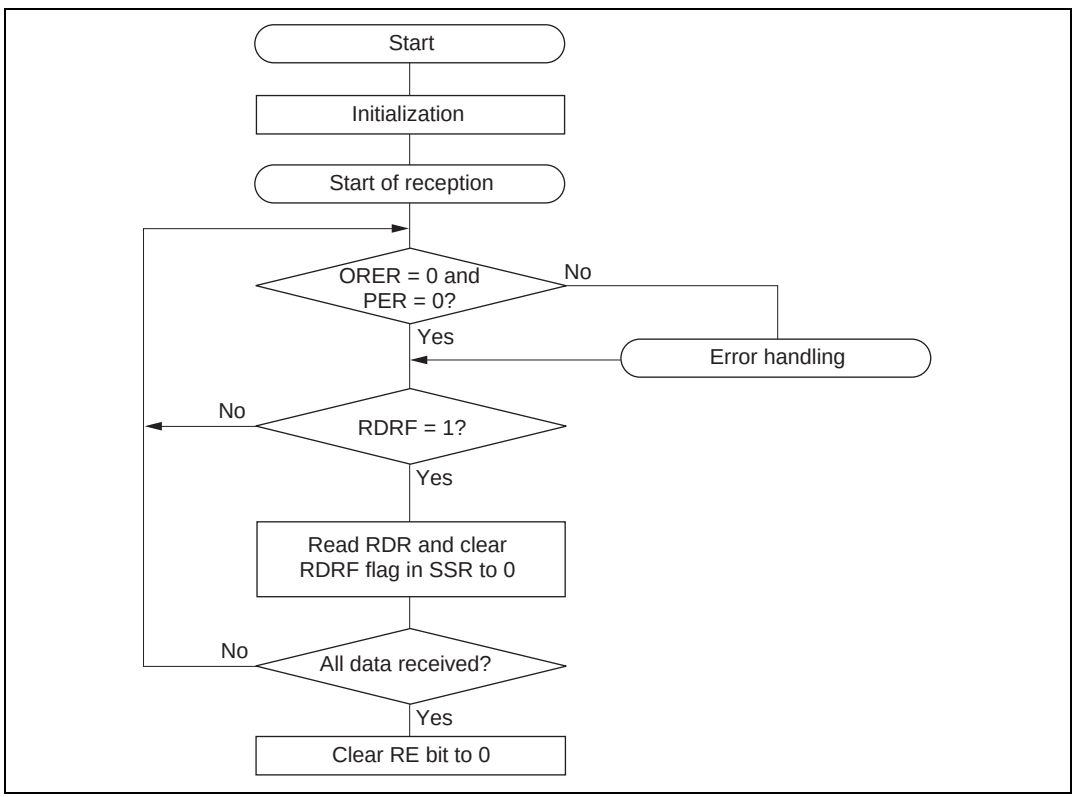

Figure 15.7 Sample Reception Flowchart

17.1.2 Block Diagram

Figure 17.1 shows a block diagram of the D/A converter.

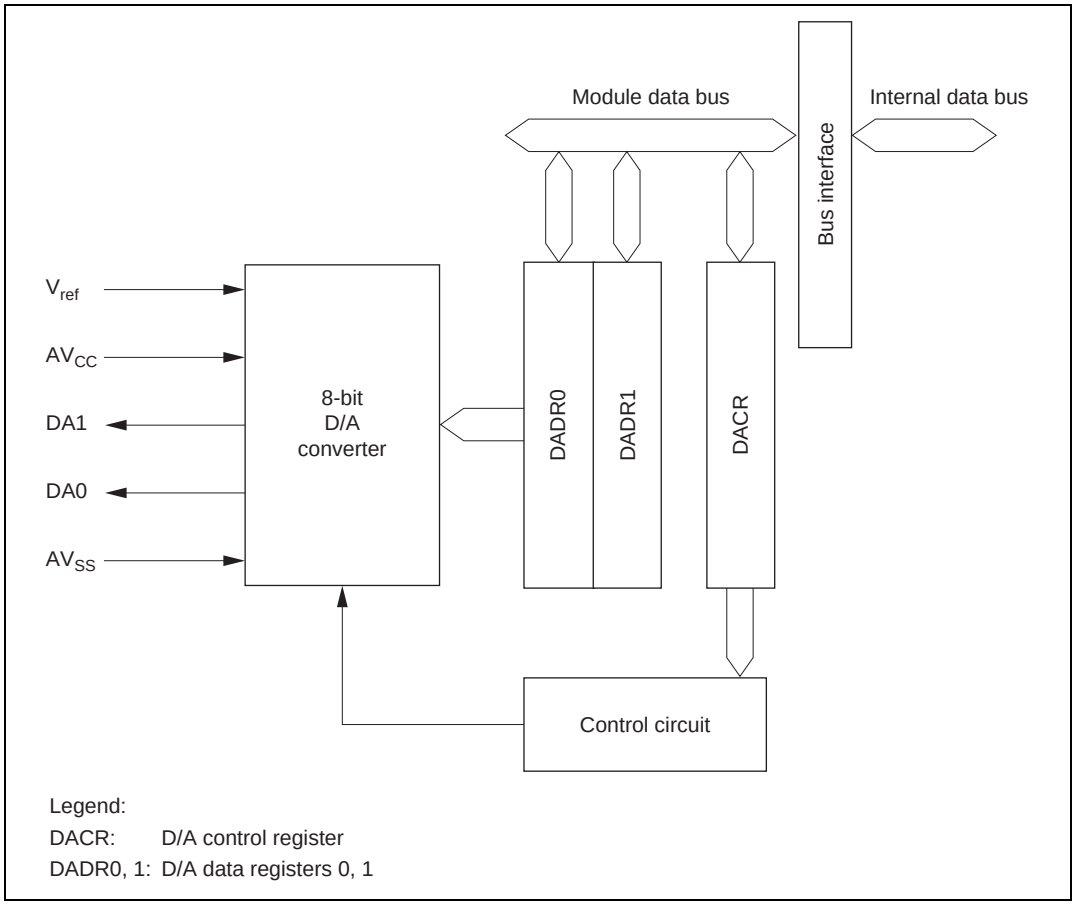

Figure 17.1 Block Diagram of D/A Converter

19.27.2 RAM Overlap

An example in which flash memory block area EB1 is overlapped is shown below.

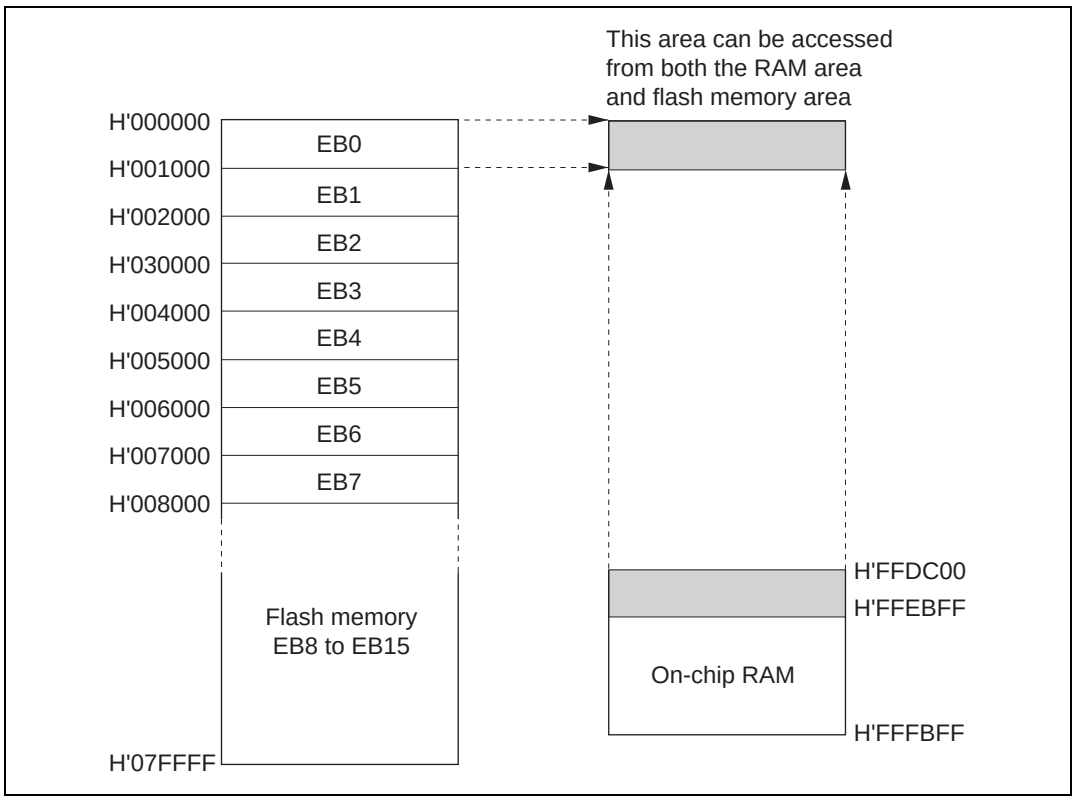

Figure 19.75 Example of RAM Overlap Operation

Example in which Flash Memory Block Area EB1 is Overlapped

1. Set bits RAMS, RAM2, RAM1, and RAM0 in RAMER to 1, 0, 0, 1, to overlap part of RAM onto the area (EB1) for which real-time programming is required.
2. Real-time programming is performed using the overlapping RAM.
3. After the program data has been confirmed, the RAMS bit is cleared, releasing RAM overlap.
4. The data written in the overlapping RAM is written into the flash memory space (EB1).

Notes: 1. When the RAMS bit is set to 1, program/erase protection is enabled for all blocks regardless of the value of RAM2, RAM1, and RAM0 (emulation protection). In this state, setting the P1 or E1 bit in flash memory control register 1 (FLMCR1), or setting

Crystal Resonator: Figure 20.3 shows the equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in table 20.3 and the same resonance frequency as the system clock (ϕ).

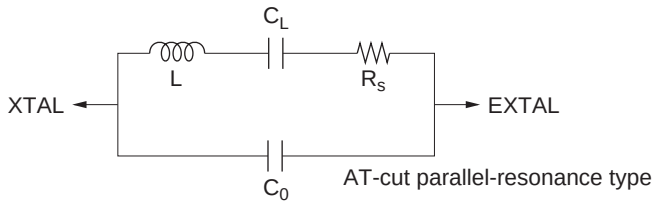

Figure 20.3 Crystal Resonator Equivalent Circuit

Table 20.3 Crystal Resonator Characteristics

Frequency (MHz)	2	4	8	12	16	20	25
R_S max (Ω)	500	120	80	60	50	40	40
C_0 max (pF)	7	7	7	7	7	7	7

Notes on Board Design: When a crystal resonator is connected, the following points should be noted:

Other signal lines should be routed away from the oscillator circuit to prevent induction from interfering with correct oscillation. See figure 20.4.

When designing the board, place the crystal resonator and its load capacitors as close as possible to the XTAL and EXTAL pins.

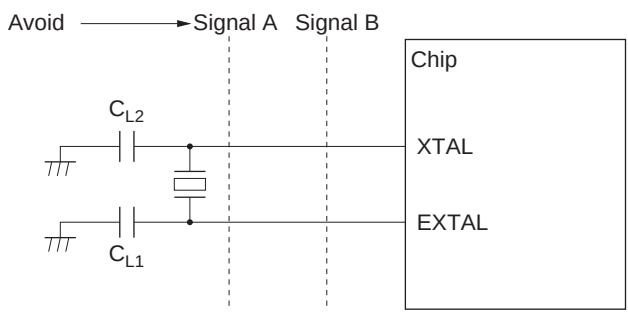

Figure 20.4 Example of Incorrect Board Design

22.2.5 D/A Conversion Characteristics

Table 22.21 D/A Conversion Characteristics

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

	Condition B				
Item	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	Bits	
Conversion time	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	LSB	4 MΩ resistive load

(5) Bit-Manipulation Instructions

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	—		I	H	N	Z	V	C	Advanced
BSET	BSET #xx:3,Rd	B		2								(#xx:3 of Rd8)←1	—	—	—	—	—	—	1
	BSET #xx:3,@ERd	B			4							(#xx:3 of @ERd)←1	—	—	—	—	—	—	4
	BSET #xx:3,@aa:8	B						4				(#xx:3 of @aa:8)←1	—	—	—	—	—	—	4
	BSET #xx:3,@aa:16	B						6				(#xx:3 of @aa:16)←1	—	—	—	—	—	—	5
	BSET #xx:3,@aa:32	B						8				(#xx:3 of @aa:32)←1	—	—	—	—	—	—	6
	BSET Rn,Rd	B		2								(Rn8 of Rd8)←1	—	—	—	—	—	—	1
	BSET Rn,@ERd	B			4							(Rn8 of @ERd)←1	—	—	—	—	—	—	4
	BSET Rn,@aa:8	B						4				(Rn8 of @aa:8)←1	—	—	—	—	—	—	4
	BSET Rn,@aa:16	B						6				(Rn8 of @aa:16)←1	—	—	—	—	—	—	5
	BSET Rn,@aa:32	B						8				(Rn8 of @aa:32)←1	—	—	—	—	—	—	6
BCLR	BCLR #xx:3,Rd	B		2								(#xx:3 of Rd8)←0	—	—	—	—	—	—	1
	BCLR #xx:3,@ERd	B			4							(#xx:3 of @ERd)←0	—	—	—	—	—	—	4
	BCLR #xx:3,@aa:8	B						4				(#xx:3 of @aa:8)←0	—	—	—	—	—	—	4
	BCLR #xx:3,@aa:16	B						6				(#xx:3 of @aa:16)←0	—	—	—	—	—	—	5
	BCLR #xx:3,@aa:32	B						8				(#xx:3 of @aa:32)←0	—	—	—	—	—	—	6
	BCLR Rn,Rd	B		2								(Rn8 of Rd8)←0	—	—	—	—	—	—	1
	BCLR Rn,@ERd	B			4							(Rn8 of @ERd)←0	—	—	—	—	—	—	4
	BCLR Rn,@aa:8	B						4				(Rn8 of @aa:8)←0	—	—	—	—	—	—	4
	BCLR Rn,@aa:16	B						6				(Rn8 of @aa:16)←0	—	—	—	—	—	—	5

MRB—DTC Mode Register B **H'F800—H'FBFF** **DTC**

Bit	7	6	5	4	3	2	1	0
	CHNE	DISEL	CHNS	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

Reserved
Only 0 should be written to these bits

DTC Chain Transfer Select

DTC Interrupt Select

0	After DTC data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0
1	After DTC data transfer ends, the CPU interrupt is enabled

DTC Chain Transfer Enable

CHNE	CHNS	Description
0	—	No chain transfer. (At end of DTC data transfer, DTC waits for activation)
1	0	Chain transfer every time
1	1	Chain transfer only when transfer counter = 0

SAR—DTC Source Address Register **H'F800—H'FBFF** **DTC**

Bit	23	22	21	20	19	- - -	4	3	2	1	0
						- - -					
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	- - -	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	- - -	—	—	—	—	—

Specifies DTC transfer data source address

DAR—DTC Destination Address Register **H'F800—H'FBFF** **DTC**

Bit	23	22	21	20	19	- - -	4	3	2	1	0
						- - -					
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	- - -	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	- - -	—	—	—	—	—

Specifies DTC transfer data destination address

TSR5—Timer Status Register 5 H'FEA5 TPU5

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt while DISEL bit of MRB in DTC is 0 • When DMAC is activated by TGIA interrupt while DTA bit of DMABCR in DMAC*1 is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Note: 1. The DMAC is not supported in the H8S/2321.

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0 for flag clearing.

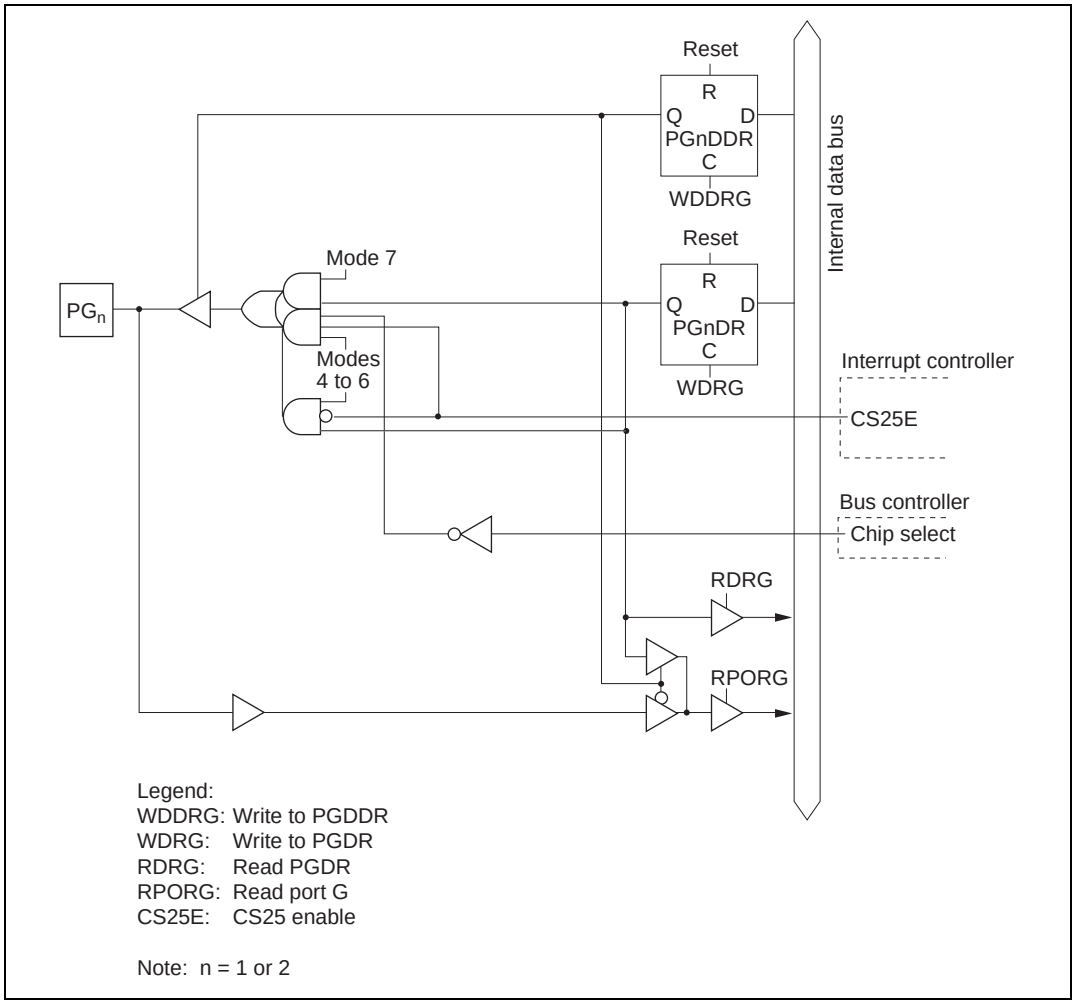

Figure C.13 (b) Port G Block Diagram (Pins PG_1 and PG_2)