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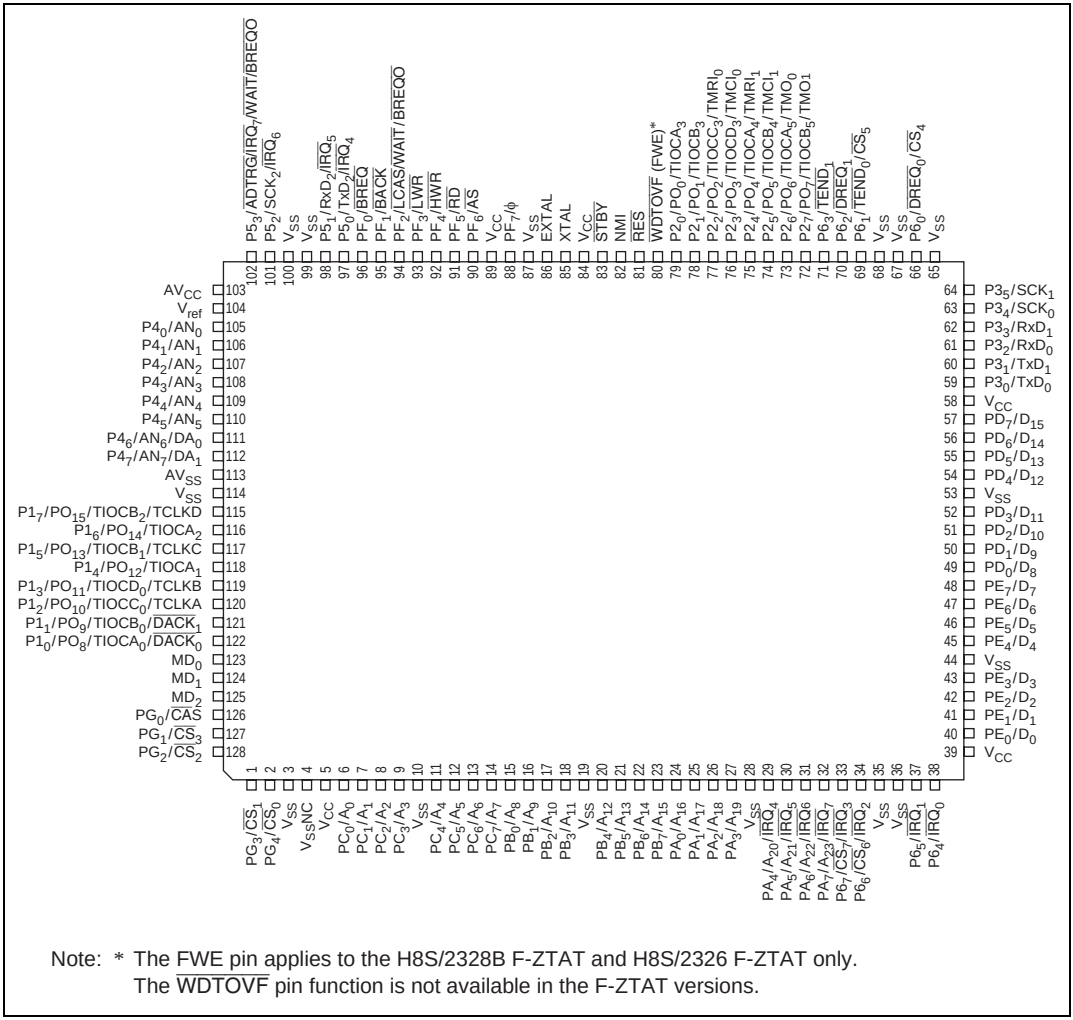
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12322rvf25v



Note: * The FWE pin applies to the H8S/2328B F-ZTAT and H8S/2326 F-ZTAT only.
The $\overline{\text{WDTOVF}}$ pin function is not available in the F-ZTAT versions.

Figure 1.4 Mask ROM Versions, F-ZTAT Versions, H8S/2324S, H8S/2322R, H8S/2320 Pin Arrangement (FP-128B: Top View)

Pin No.		Pin Name				
TFP-120	FP-128B	Mode 4*1	Mode 5*1	Mode 6	Mode 7	Flash Memory Programmer Mode
101	111	$P4_6/AN_6/DA_0$	$P4_6/AN_6/DA_0$	$P4_6/AN_6/DA_0$	$P4_6/AN_6/DA_0$	NC
102	112	$P4_7/AN_7/DA_1$	$P4_7/AN_7/DA_1$	$P4_7/AN_7/DA_1$	$P4_7/AN_7/DA_1$	NC
103	113	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	V_{SS}
104	114	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
105	115	$P1_7/PO_{15}/TIOCB_2/TCLKD$	$P1_7/PO_{15}/TIOCB_2/TCLKD$	$P1_7/PO_{15}/TIOCB_2/TCLKD$	$P1_7/PO_{15}/TIOCB_2/TCLKD$	NC
106	116	$P1_6/PO_{14}/TIOCA_2$	$P1_6/PO_{14}/TIOCA_2$	$P1_6/PO_{14}/TIOCA_2$	$P1_6/PO_{14}/TIOCA_2$	NC
107	117	$P1_5/PO_{13}/TIOCB_1/TCLKC$	$P1_5/PO_{13}/TIOCB_1/TCLKC$	$P1_5/PO_{13}/TIOCB_1/TCLKC$	$P1_5/PO_{13}/TIOCB_1/TCLKC$	NC
108	118	$P1_4/PO_{12}/TIOCA_1$	$P1_4/PO_{12}/TIOCA_1$	$P1_4/PO_{12}/TIOCA_1$	$P1_4/PO_{12}/TIOCA_1$	NC
109	119	$P1_3/PO_{11}/TIOCD_0/TCLKB$	$P1_3/PO_{11}/TIOCD_0/TCLKB$	$P1_3/PO_{11}/TIOCD_0/TCLKB$	$P1_3/PO_{11}/TIOCD_0/TCLKB$	NC
110	120	$P1_2/PO_{10}/TIOCC_0/TCLKA$	$P1_2/PO_{10}/TIOCC_0/TCLKA$	$P1_2/PO_{10}/TIOCC_0/TCLKA$	$P1_2/PO_{10}/TIOCC_0/TCLKA$	NC
111	121	$P1_1/PO_9/TIOCB_0/\overline{DACK_1}$*5	$P1_1/PO_9/TIOCB_0/\overline{DACK_1}$*5	$P1_1/PO_9/TIOCB_0/\overline{DACK_1}$*5	$P1_1/PO_9/TIOCB_0/\overline{DACK_1}$*5	NC
112	122	$P1_0/PO_8/TIOCA_0/\overline{DACK_0}$*6	$P1_0/PO_8/TIOCA_0/\overline{DACK_0}$*6	$P1_0/PO_8/TIOCA_0/\overline{DACK_0}$*6	$P1_0/PO_8/TIOCA_0/\overline{DACK_0}$*6	NC
113	123	MD_0	MD_0	MD_0	MD_0	V_{SS}
114	124	MD_1	MD_1	MD_1	MD_1	V_{SS}
115	125	MD_2	MD_2	MD_2	MD_2	V_{SS}
116	126	$PG_0/\overline{CAS}$ *6	$PG_0/\overline{CAS}$ *6	$PG_0/\overline{CAS}$ *6	PG_0	NC
117	127	$PG_1/\overline{CS_3}$	$PG_1/\overline{CS_3}$	$PG_1/\overline{CS_3}$	PG_1	NC
118	128	$PG_2/\overline{CS_2}$	$PG_2/\overline{CS_2}$	$PG_2/\overline{CS_2}$	PG_2	NC
119	1	$PG_3/\overline{CS_1}$	$PG_3/\overline{CS_1}$	$PG_3/\overline{CS_1}$	PG_3	NC
120	2	$PG_4/\overline{CS_0}$	$PG_4/\overline{CS_0}$	$PG_4/\overline{CS_0}$	PG_4	NC

Type	Symbol	Pin No. TFP-120	Pin No. FP-128B	I/O	Name and Function
I/O ports	$P6_7$ to $P6_0$	29 to 32, 63 to 60	33, 34, 37, 38, 71 to 69, 66	I/O	**Port 6:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port 6 data direction register (P6DDR).
	PA_7 to PA_0	28 to 25, 23 to 20	32 to 29, 27 to 24	I/O	**Port A:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port A data direction register (PADDR).
	PB_7 to PB_0	19 to 16, 14 to 11	23 to 20, 18 to 15	I/O	**Port B**[*5]**:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port B data direction register (PBDDR).
	PC_7 to PC_0	10 to 7, 5 to 2	14 to 11, 9 to 6	I/O	**Port C**[*5]**:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port C data direction register (PCDDR).
	PD_7 to PD_0	51 to 48, 46 to 43	57 to 54, 52 to 49	I/O	**Port D**[*5]**:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port D data direction register (PDDDR).
	PE_7 to PE_0	42 to 39, 37 to 34	48 to 45, 43 to 40	I/O	**Port E:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port E data direction register (PEDDR).
	PF_7 to PF_0	80, 82 to 88	88, 90 to 96	I/O	**Port F:** An 8-bit I/O port. Input or output can be designated for each bit by means of the port F data direction register (PFDDR).
	PG_4 to PG_0	120 to 116	2, 1, 128 to 126	I/O	**Port G:** A 5-bit I/O port. Input or output can be designated for each bit by means of the port G data direction register (PGDDR).

Notes: 1. Applies to the H8S/2328B F-ZTAT and H8S/2326 F-ZTAT only.
2. Applies to the H8S/2329B F-ZTAT only.
3. Not supported in the H8S/2321.
4. Not available in the F-ZTAT versions.
5. Cannot be used as an I/O port in the ROMless versions.

Table 4.2 Exception Vector Table

Exception Source		Vector Number	Vector Address[*1] Advanced Mode
Reset		0	H'0000 to H'0003
Reserved		1	H'0004 to H'0007
Reserved for system use		2	H'0008 to H'000B
		3	H'000C to H'000F
		4	H'0010 to H'0013
Trace		5	H'0014 to H'0017
Reserved for system use		6	H'0018 to H'001B
External interrupt	NMI	7	H'001C to H'001F
Trap instruction (4 sources)		8	H'0020 to H'0023
		9	H'0024 to H'0027
		10	H'0028 to H'002B
		11	H'002C to H'002F
Reserved for system use		12	H'0030 to H'0033
		13	H'0034 to H'0037
		14	H'0038 to H'003B
		15	H'003C to H'003F
External interrupt	IRQ0	16	H'0040 to H'0043
	IRQ1	17	H'0044 to H'0047
	IRQ2	18	H'0048 to H'004B
	IRQ3	19	H'004C to H'004F
	IRQ4	20	H'0050 to H'0053
	IRQ5	21	H'0054 to H'0057
	IRQ6	22	H'0058 to H'005B
	IRQ7	23	H'005C to H'005F
Internal interrupt[*2]		24 | 91	H'0060 to H'0063 | H'016C to H'016F

Notes: 1. Lower 16 bits of the address.

2. For details of internal interrupt vectors, see section 5.3.3, Interrupt Exception Vector Table.

6.2.3 Wait Control Registers H and L (WCRH, WCRL)

WCRH and WCRL are 8-bit readable/writable registers that select the number of program wait states for each area.

Program waits are not inserted in the case of on-chip memory or internal I/O registers.

WCRH and WCRL are initialized to H'FF by a reset and in hardware standby mode. They are not initialized in software standby mode.

WCRH

Bit	:	7	6	5	4	3	2	1	0
		W71	W70	W61	W60	W51	W50	W41	W40
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—Area 7 Wait Control 1 and 0 (W71, W70): These bits select the number of program wait states when area 7 in external space is accessed while the AST7 bit in ASTCR is set to 1.

Bit 7 W71	Bit 6 W70	Description
0	0	Program wait not inserted when external space area 7 is accessed
	1	1 program wait state inserted when external space area 7 is accessed
1	0	2 program wait states inserted when external space area 7 is accessed
	1	3 program wait states inserted when external space area 7 is accessed (Initial value)

Mode 6: In mode 6, port C pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.

Port C pin functions in mode 6 are shown in figure 9.14.

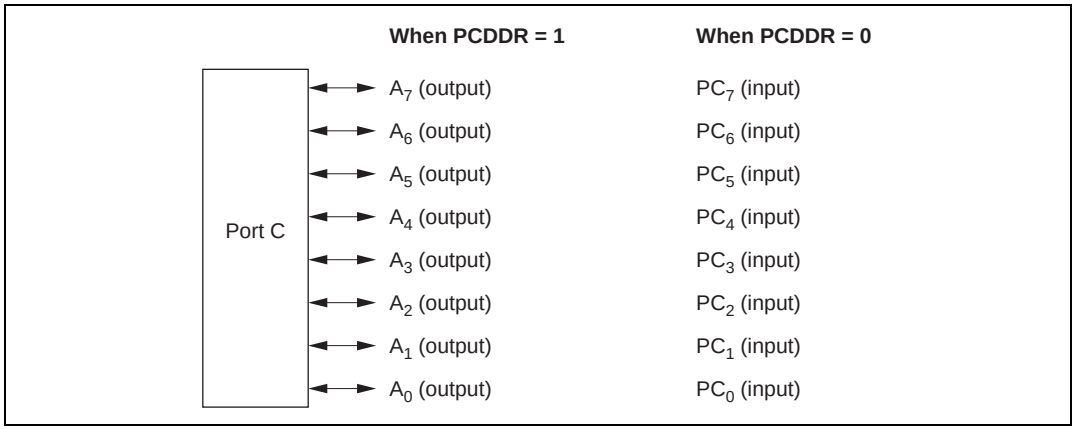


Figure 9.14 Port C Pin Functions (Mode 6)

Mode 7: In mode 7, port C pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PCDDR bit to 1 makes the corresponding port C pin an output port, while clearing the bit to 0 makes the pin an input port.

Port C pin functions in mode 7 are shown in figure 9.15.

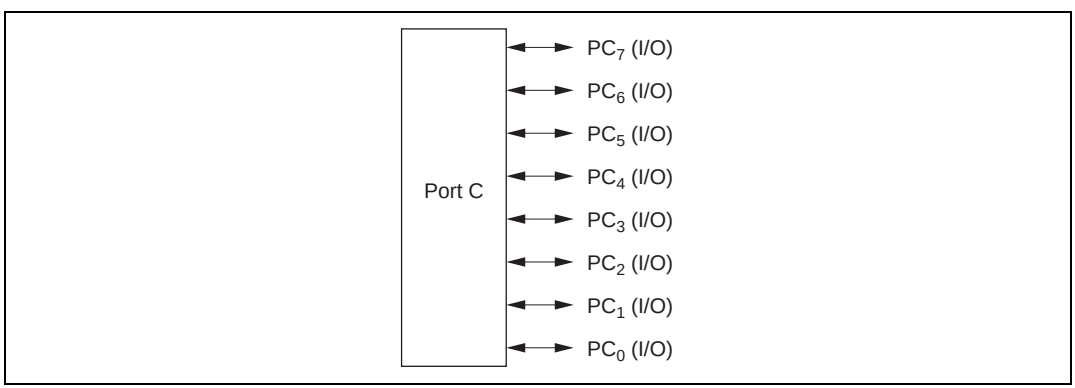


Figure 9.15 Port C Pin Functions (Mode 7)

9.13 Port F

9.13.1 Overview

Port F is an 8-bit I/O port. Port F pins also function as bus control signal input/output pins ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, $\overline{LWR}$, $\overline{LCAS}$*, $\overline{WAIT}$, $\overline{BREQO}$, $\overline{BREQ}$, and $\overline{BACK}$) and the system clock (ϕ) output pin. The $\overline{AS}$, $\overline{LWR}$, and $\overline{BREQO}$ output pins can be switched by means of settings in PFCR2 and SYSCR.

Figure 9.22 shows the port F pin configuration.

Note: * $\overline{LCAS}$ is not supported in the H8S/2321.

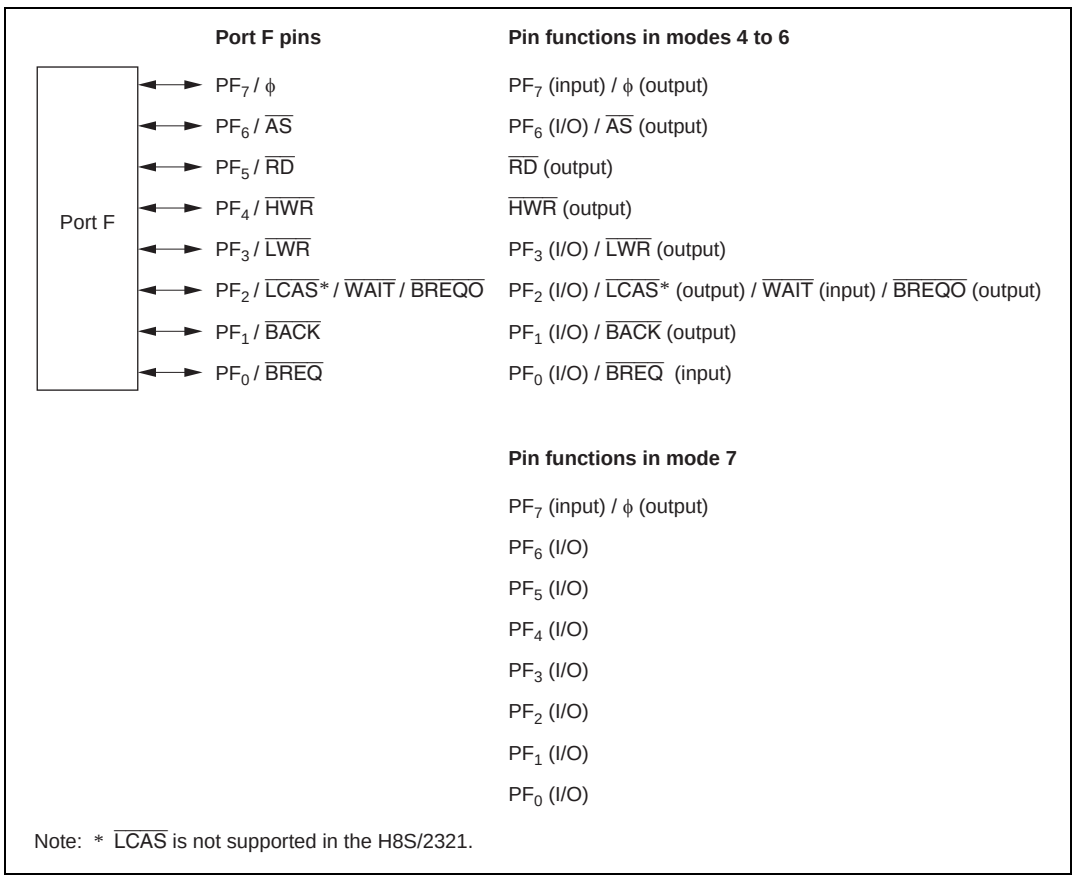


Figure 9.22 Port F Pin Functions

15.3.3 Data Format

Normal Transfer Mode: Figure 15.3 shows the smart card interface data format in the normal transfer mode. In reception in this mode, a parity check is carried out on each frame. If an error is detected an error signal is sent back to the transmitting end, and retransmission of the data is requested. If an error signal is sampled during transmission, the same data is retransmitted.

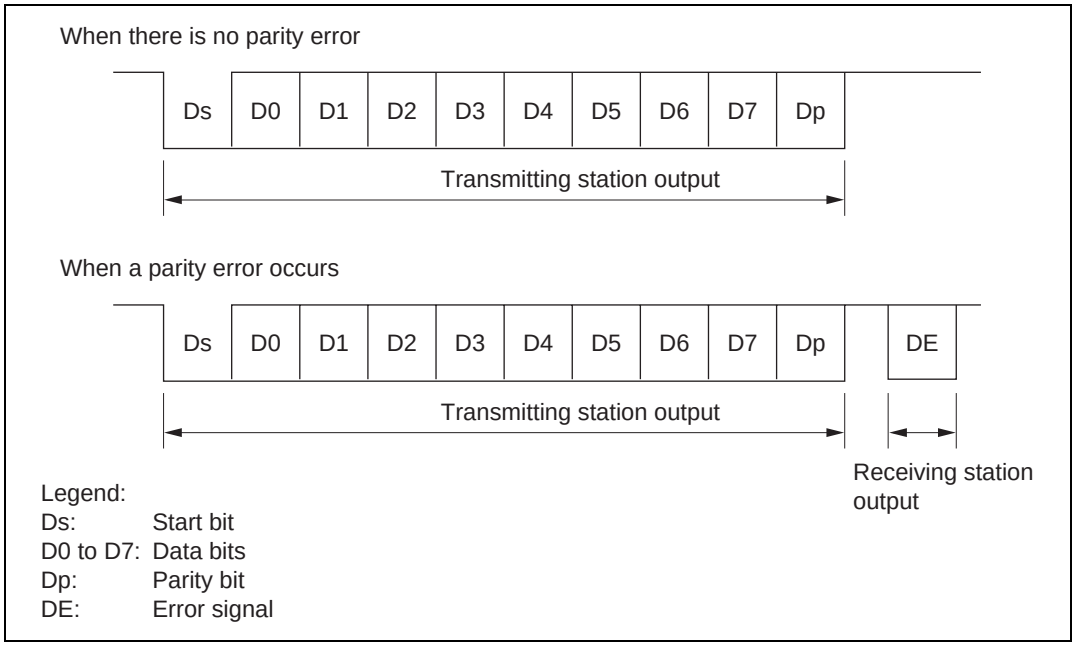
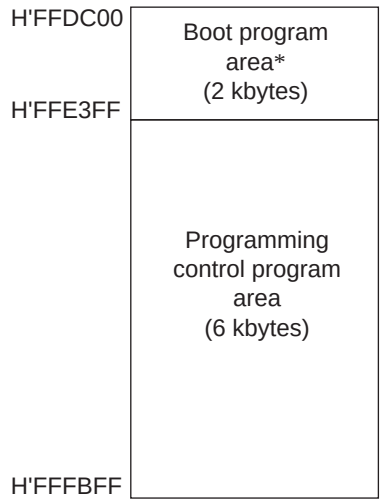


Figure 15.3 Smart Card Interface Data Format

On-Chip RAM Area Divisions in Boot Mode: In boot mode, the 2-kbyte area from H'FFDC00 to H'FFE3FF is reserved for use by the boot program, as shown in figure 19.69. The area to which the programming control program is transferred is H'FFE400 to H'FFFBFF. The boot program area can be used when the programming control program transferred into RAM enters the execution state. A stack area should be set up as required.



Note: * The boot program area cannot be used until a transition is made to the execution state for the programming control program transferred to RAM. Note that the boot program remains stored in this area after a branch is made to the programming control program.

Figure 19.69 RAM Areas in Boot Mode

Notes on Use of Boot Mode

- When the chip comes out of reset in boot mode, it measures the low-level period of the input at the SCI's RxD1 pin. The reset should end with RxD1 high. After the reset ends, it takes approximately 100 states before the chip is ready to measure the low-level period of the RxD1 pin.
- In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.
- Interrupts cannot be used while the flash memory is being programmed or erased.

19.29 Flash Memory PROM Mode

19.29.1 PROM Mode Setting

Programs and data can be written and erased in PROM mode as well as in the on-board programming modes. In PROM mode, the on-chip ROM can be freely programmed using a PROM programmer that supports the Renesas microcomputer device type with 512-kbyte on-chip flash memory (FZTAT512V3A). Flash memory read mode, auto-program mode, auto-erase mode, and status read mode are supported with this device type. In auto-program mode, auto-erase mode, and status read mode, a status polling procedure is used, and in status read mode, detailed internal signals are output after execution of an auto-program or auto-erase operation.

Table 19.55 shows PROM mode pin settings.

Table 19.55 PROM Mode Pin Settings

Pin Names	Settings/External Circuit Connection
Mode pins: MD2, MD1, MD0	Low-level input
Mode setting pins: P66, P65, P64	High-level input to P66, low-level input to P65 and P64
FWE pin	High-level input (in auto-program and auto-erase modes)
$\overline{\text{STBY}}$ pin	High-level input (do not select hardware standby mode)
$\overline{\text{RES}}$ pin	Reset circuit
XTAL, EXTAL pins	Oscillator circuit
Other pins requiring setting: P32, P25	High-level input to P32, low-level input to P25

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)								Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa		I	H	N	Z	V	C	Advanced
MOV	MOV.L ERs,@ERd	L			4						ERs32→@ERd	—	—	↕	↕	0	—	4
	MOV.L ERs,@(d:16,ERd)	L				6					ERs32→@(d:16,ERd)	—	—	↕	↕	0	—	5
	MOV.L ERs,@(d:32,ERd)	L				10					ERs32→@(d:32,ERd)	—	—	↕	↕	0	—	7
	MOV.L ERs,@-ERd	L					4				ERd32-4→ERd32,ERs32→@ERd	—	—	↕	↕	0	—	5
	MOV.L ERs,@aa:16	L						6			ERs32→@aa:16	—	—	↕	↕	0	—	5
	MOV.L ERs,@aa:32	L						8			ERs32→@aa:32	—	—	↕	↕	0	—	6
POP	POP.W Rn	W								2	@SP→Rn16,SP+2→SP	—	—	↕	↕	0	—	3
	POP.L ERn	L								4	@SP→ERn32,SP+4→SP	—	—	↕	↕	0	—	5
PUSH	PUSH.W Rn	W								2	SP-2→SP,Rn16→@SP	—	—	↕	↕	0	—	3
	PUSH.L ERn	L								4	SP-4→SP,ERn32→@SP	—	—	↕	↕	0	—	5
LDM	LDM @SP+,(ERm-ERn)	L								4	(@SP→ERn32,SP+4→SP) Repeated for each register restored	—	—	—	—	—	—	7/9/11 [1]
STM	STM (ERm-ERn),@-SP	L								4	(SP-4→SP,ERn32→@SP) Repeated for each register saved	—	—	—	—	—	—	7/9/11 [1]
MOVFPE	MOVFPE @aa:16,Rd	Cannot be used in the chip																[2]
MOVTPE	MOVTPE Rs,@aa:16	Cannot be used in the chip																[2]

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte	10th byte
BOR	BOR #xx:3,Rd	B	7	4	0 IMM	rd														
	BOR #xx:3,@ERd	B	7	C	0 erd	0	7	4	0 IMM	0										
	BOR #xx:3,@aa:8	B	7	E	abs		7	4	0 IMM	0										
	BOR #xx:3,@aa:16	B	6	A	1	0	abs				7	4	0 IMM	0						
	BOR #xx:3,@aa:32	B	6	A	3	0	abs								7	4	0 IMM	0		
BSET	BSET #xx:3,Rd	B	7	0	0 IMM	rd														
	BSET #xx:3,@ERd	B	7	D	0 erd	0	7	0	0 IMM	0										
	BSET #xx:3,@aa:8	B	7	F	abs		7	0	0 IMM	0										
	BSET #xx:3,@aa:16	B	6	A	1	8	abs				7	0	0 IMM	0						
	BSET #xx:3,@aa:32	B	6	A	3	8	abs								7	0	0 IMM	0		
	BSET Rn,Rd	B	6	0	rn	rd														
	BSET Rn,@ERd	B	7	D	0 erd	0	6	0	rn	0										
	BSET Rn,@aa:8	B	7	F	abs		6	0	rn	0										
	BSET Rn,@aa:16	B	6	A	1	8	abs				6	0	rn	0						
	BSET Rn,@aa:32	B	6	A	3	8	abs								6	0	rn	0		
BSR	BSR d:8	—	5	5	disp															
	BSR d:16	—	5	C	0	0	disp													
BST	BST #xx:3,Rd	B	6	7	0 IMM	rd														
	BST #xx:3,@ERd	B	7	D	0 erd	0	6	7	0 IMM	0										
	BST #xx:3,@aa:8	B	7	F	abs		6	7	0 IMM	0										
	BST #xx:3,@aa:16	B	6	A	1	8	abs				6	7	0 IMM	0						
	BST #xx:3,@aa:32	B	6	A	3	8	abs								6	7	0 IMM	0		
BTST	BTST #xx:3,Rd	B	7	3	0 IMM	rd														
	BTST #xx:3,@ERd	B	7	C	0 erd	0	7	3	0 IMM	0										
	BTST #xx:3,@aa:8	B	7	E	abs		7	3	0 IMM	0										
	BTST #xx:3,@aa:16	B	6	A	1	0	abs				7	3	0 IMM	0						
	BTST #xx:3,@aa:32	B	6	A	3	0	abs								7	3	0 IMM	0		
	BTST Rn,Rd	B	6	3	rn	rd														
	BTST Rn,@ERd	B	7	C	0 erd	0	6	3	rn	0										

Instruction	H	N	Z	V	C	Definition
SUB	↕	↕	↕	↕	↕	H = Sm–4 · $\overline{Dm–4}$ + $\overline{Dm–4}$ · Rm–4 + Sm–4 · Rm–4
						N = Rm
						Z = $\overline{Rm}$ · $\overline{Rm–1}$ · ····· · $\overline{R0}$
						V = $\overline{Sm}$ · Dm · $\overline{Rm}$ + Sm · $\overline{Dm}$ · Rm
						C = Sm · $\overline{Dm}$ + $\overline{Dm}$ · Rm + Sm · Rm
SUBS	—	—	—	—	—	
SUBX	↕	↕	↕	↕	↕	H = Sm–4 · $\overline{Dm–4}$ + $\overline{Dm–4}$ · Rm–4 + Sm–4 · Rm–4
						N = Rm
						Z = Z' · $\overline{Rm}$ · ····· · $\overline{R0}$
						V = $\overline{Sm}$ · Dm · $\overline{Rm}$ + Sm · $\overline{Dm}$ · Rm
						C = Sm · $\overline{Dm}$ + $\overline{Dm}$ · Rm + Sm · Rm
TAS	—	↕	↕	0	—	N = Dm
						Z = $\overline{Dm}$ · $\overline{Dm–1}$ · ····· · $\overline{D0}$
TRAPA	—	—	—	—	—	
XOR	—	↕	↕	0	—	N = Rm
						Z = $\overline{Rm}$ · $\overline{Rm–1}$ · ····· · $\overline{R0}$
XORC	↕	↕	↕	↕	↕	Stores the corresponding bits of the result.
						No flags change when the operand is EXR.

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FE90	TCR4	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU4	16 bits
H'FE91	TMDR4	—	—	—	—	MD3	MD2	MD1	MD0		
H'FE92	TIOR4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE94	TIER4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FE95	TSR4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FE96	TCNT4										
H'FE97											
H'FE98	TGR4A										
H'FE99											
H'FE9A	TGR4B										
H'FE9B											
H'FEA0	TCR5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU5	16 bits
H'FEA1	TMDR5	—	—	—	—	MD3	MD2	MD1	MD0		
H'FEA2	TIOR5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FEA4	TIER5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FEA5	TSR5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FEA6	TCNT5										
H'FEA7											
H'FEA8	TGR5A										
H'FEA9											
H'FEAA	TGR5B										
H'FEAB											
H'FEB0	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	Ports	8 bits
H'FEB1	P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR		
H'FEB2	P3DDR	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FEB4	P5DDR	—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR		
H'FEB5	P6DDR	P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR		
H'FEB9	PADDR	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR		
H'FEBA	PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR		
H'FEBB	PCDDR	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR		
H'FEBC	PDDDR	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR		
H'FEBD	PEDDR	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR		
H'FEBE	PFDDR	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR		
H'FEBF	PGDDR	—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR		

DMATCR—DMA Terminal Control Register H'FF01 DMAC
(Not supported in H8S/2321)

Bit	:	7	6	5	4	3	2	1	0
DMATCR	:	—	—	TEE1	TEE0	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	—	R/W	R/W	—	—	—	—

Transfer End Enable 0

0	$\overline{\text{TEND}}_0$ pin output disabled
1	$\overline{\text{TEND}}_0$ pin output enabled

Transfer End Enable 1

0	$\overline{\text{TEND}}_1$ pin output disabled
1	$\overline{\text{TEND}}_1$ pin output enabled

NDERH — Next Data Enable Register H **H'FF48** **PPG**
NDERL — Next Data Enable Register L **H'FF49** **PPG**

NDERH

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Enable/Disable

0	Pulse outputs PO_{15} to PO_8 are disabled
1	Pulse outputs PO_{15} to PO_8 are enabled

NDERL

Bit	7	6	5	4	3	2	1	0
	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Enable/Disable

0	Pulse outputs PO_7 to PO_0 are disabled
1	Pulse outputs PO_7 to PO_0 are enabled

RDR0—Receive Data Register 0 **H'FF7D** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR0—Smart Card Mode Register 0 **H'FF7E** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

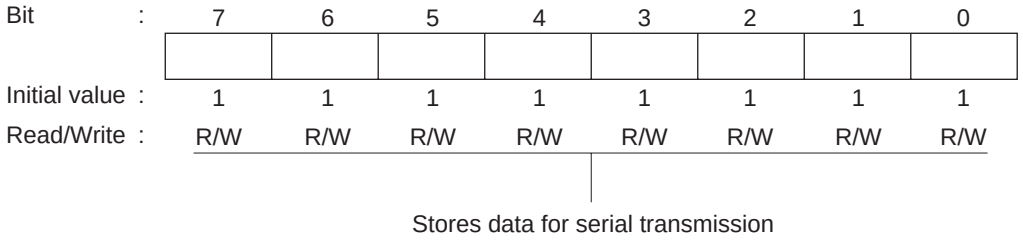
Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

TDR2—Transmit Data Register 2 **H'FF8B SCI2, Smart Card Interface 2**



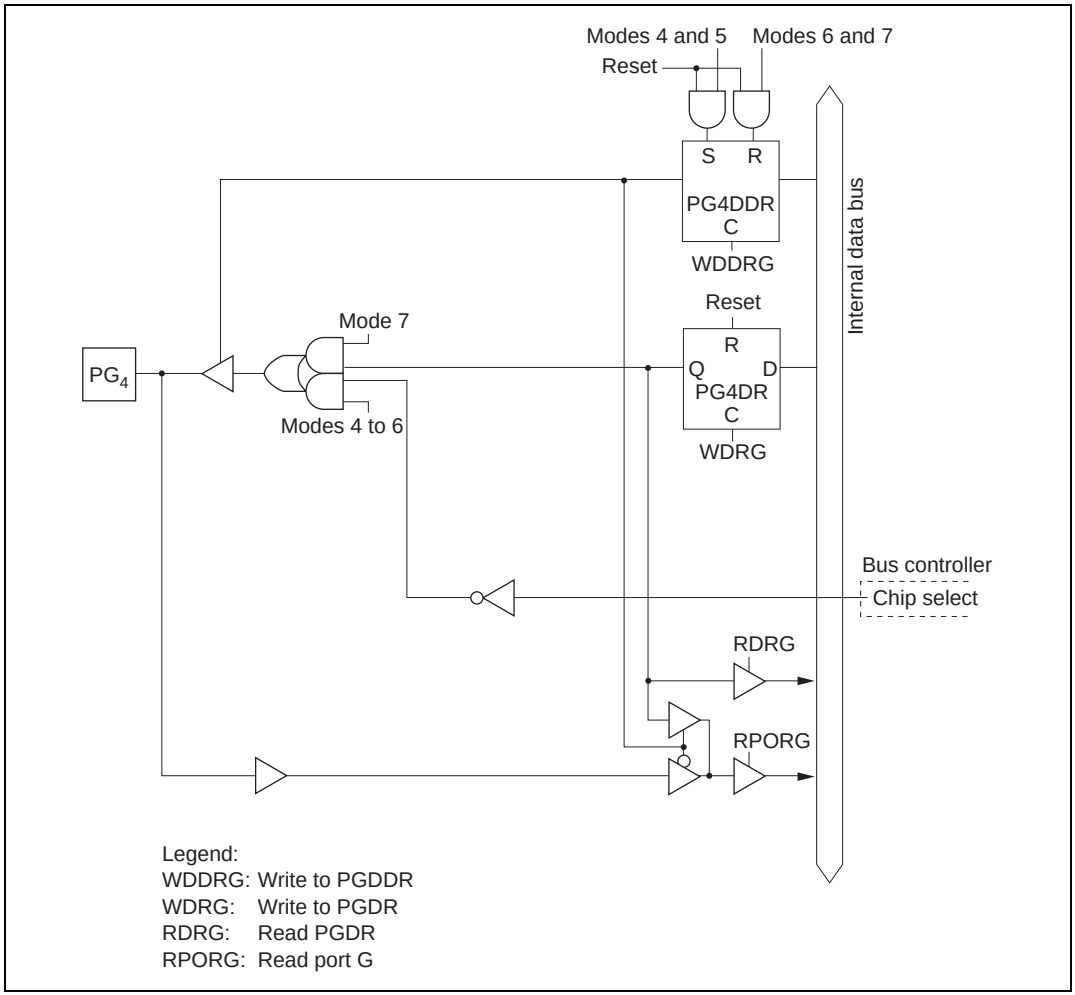


Figure C.13 (d) Port G Block Diagram (Pin PG_4)