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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12322rvte20v

6.1.2 Block Diagram

Figure 6.1 shows a block diagram of the bus controller.

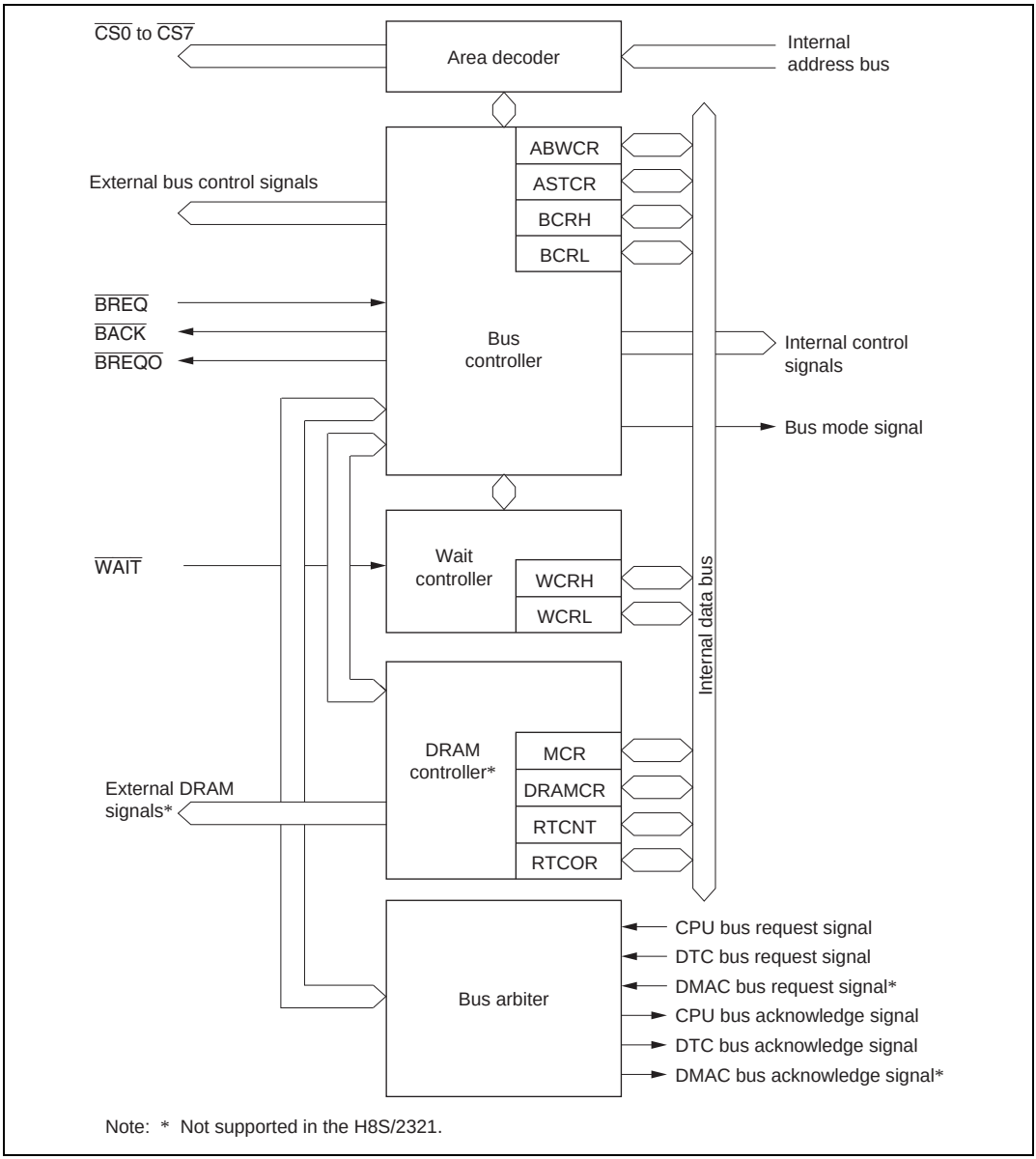

Figure 6.1 Block Diagram of Bus Controller

- RAS up mode

  To select RAS up mode, clear the RCDM bit in MCR to 0. Each time access to DRAM space is interrupted and another space is accessed, the $\overline{RAS}$ signal goes high again. Burst operation is only performed if DRAM space is continuous. Figure 6.22 shows an example of the timing in RAS up mode.

  In the case of burst ROM space access, the $\overline{RAS}$ signal is not restored to the high level.

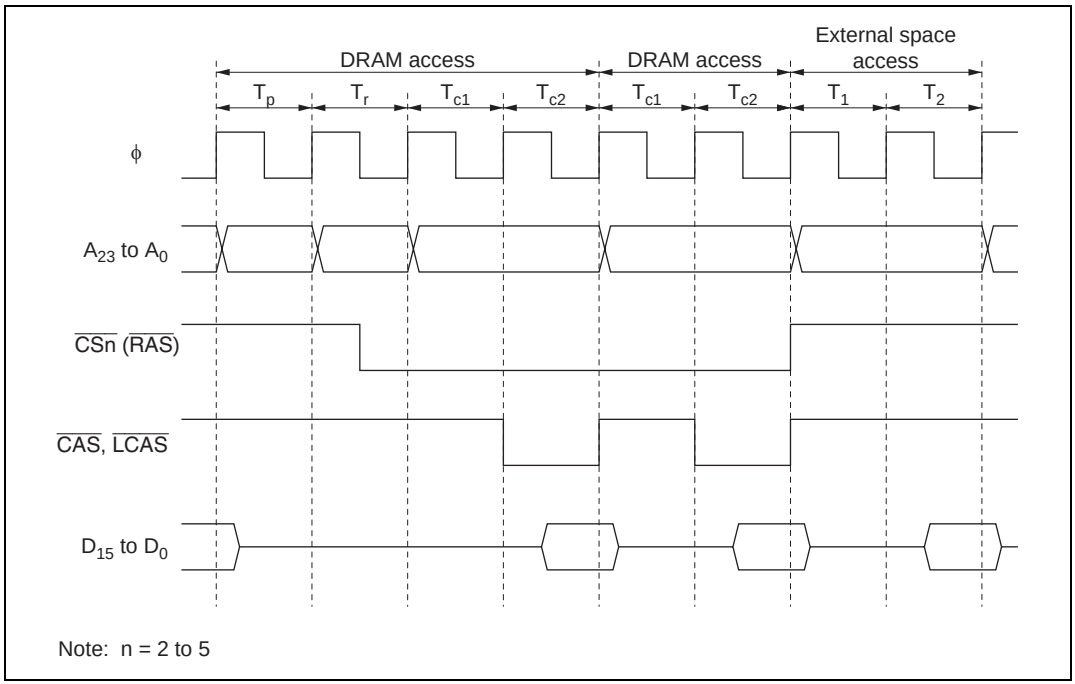

Figure 6.22 Example of Operation Timing in RAS Up Mode

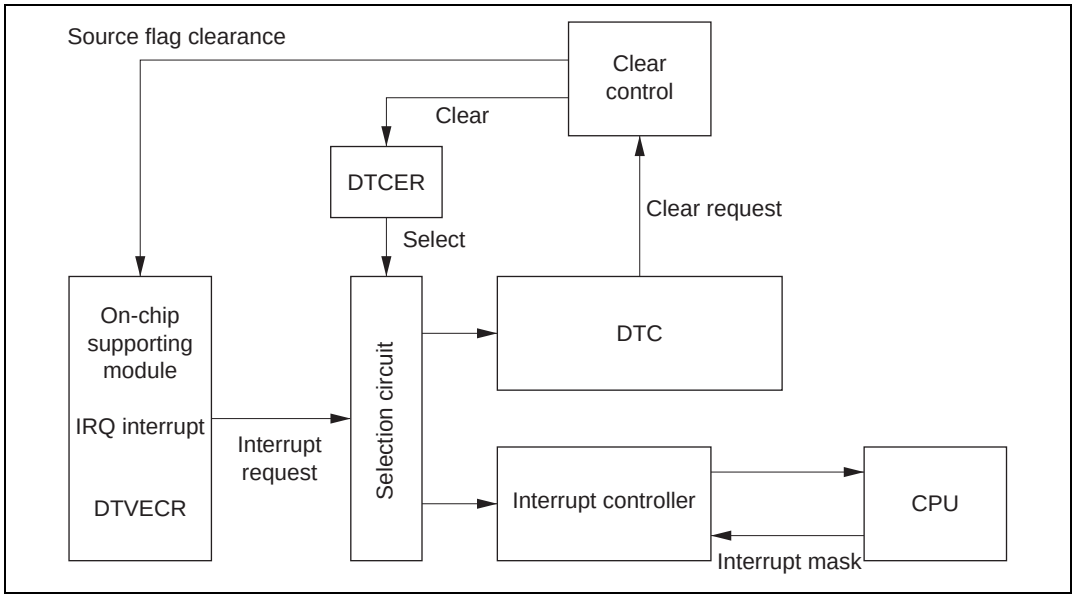

Figure 8.3 Block Diagram of DTC Activation Source Control

When an interrupt has been designated a DTC activation source, existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities.

8.3.3 DTC Vector Table

Figure 8.4 shows the correspondence between DTC vector addresses and register information.

Table 8.5 shows the correspondence between activation, vector addresses, and DTCER bits. When the DTC is activated by software, the vector address is obtained from: H'0400 + (DTVECR[6:0] << 1) (where << 1 indicates a 1-bit left shift). For example, if DTVECR is H'10, the vector address is H'0420.

The DTC reads the start address of the register information from the vector address set for each activation source, and then reads the register information from that start address. The register information can be placed at predetermined addresses in the on-chip RAM. The start address of the register information should be an integral multiple of four.

The configuration of the vector address is a 2-byte unit. These two bytes specify the lower bits of the address in the on-chip RAM.

9.2.3 Pin Functions

Port 1 pins also function as PPG output pins (PO_{15} to PO_8), TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, $TIOCA_0$, $TIOCB_0$, $TIOCC_0$, $TIOCD_0$, $TIOCA_1$, $TIOCB_1$, $TIOCA_2$, and $TIOCB_2$), and DMAC* output pins ($\overline{DACK}_0$ and $\overline{DACK}_1$). Port 1 pin functions are shown in table 9.3.

Note: * The DMAC is not supported in the H8S/2321.

Table 9.3 Port 1 Pin Functions

Pin	Selection Method and Pin Functions
$P1_7/PO_{15}/TIOCB_2/TCLKD$	The pin function is switched as shown below according to the combination of the TPU channel 2 setting (by bits MD3 to MD0 in TMDR2, bits IOB3 to IOB0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bits TPSC2 to TPSC0 in TCR0 and TCR5, bit NDER15 in NDERH, and bit P17DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)		
P17DDR	—	0	1	1
NDER15	—	—	0	1
Pin function	$TIOCB_2$ output	$P1_7$ input	$P1_7$ output	PO_{15} output
		$TIOCB_2$ input*1		
	TCLKD input*2			

Notes: 1. $TIOCB_2$ input when MD3 to MD0 = B'0000 or B'01xx, and IOB3 = 1.
2. TCLKD input when the setting for either TCR0 or TCR5 is: TPSC2 to TPSC0 = B'111.
TCLKD input when channels 2 and 4 are set to phase counting mode.

TPU Channel 2 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

9.3 Port 2

9.3.1 Overview

Port 2 is an 8-bit I/O port. Port 2 pins also function as PPG output pins (PO_7 to PO_0), TPU I/O pins ($TIOCA_3$, $TIOCB_3$, $TIOCC_3$, $TIOCD_3$, $TIOCA_4$, $TIOCB_4$, $TIOCA_5$, and $TIOCB_5$) and 8-bit timer I/O pins ($TMRI_0$, $TMCI_0$, TMO_0, $TMRI_1$, $TMCI_1$, TMO_1). Port 2 pin functions are the same in all operating modes. Port 2 uses Schmitt-triggered input.

Figure 9.2 shows the port 2 pin configuration.

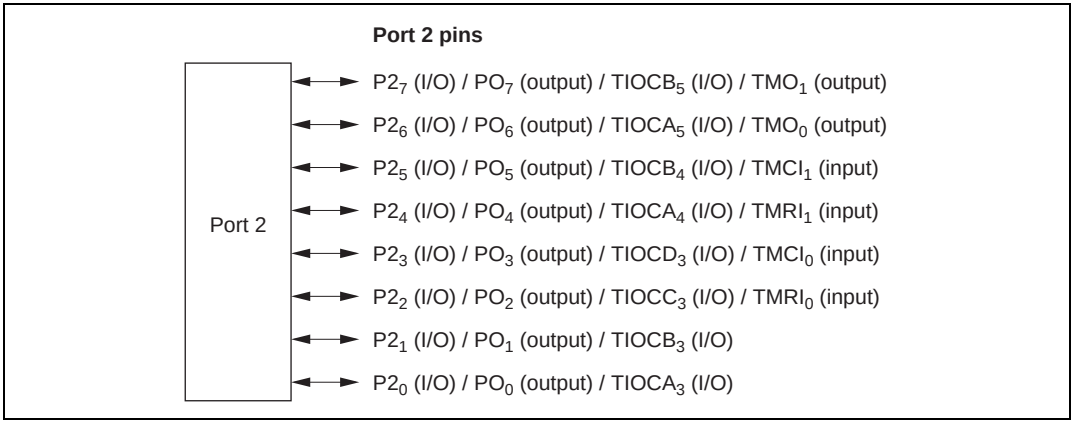

Figure 9.2 Port 2 Pin Functions

Pin	Selection Method and Pin Functions
$P2_4/PO_4/TIOCA_4/TMRI_1$	This pin is used as the 8-bit timer counter reset pin when bits CCLR1 and CCLR0 in TCR1 are both set to 1. The pin function is switched as shown below according to the combination of the TPU channel 4 setting (by bits MD3 to MD0 in TMDR4, bits IOA3 to IOA0 in TIOR4, and bits CCLR1 and CCLR0 in TCR4), bit NDER4 in NDERL, and bit P24DDR.

TPU Channel 4 Setting	Table Below (1)	Table Below (2)		
P24DDR	—	0	1	1
NDER4	—	—	0	1
Pin function	$TIOCA_4$ output	$P2_4$ input	$P2_4$ output	PO_4 output
		$TIOCA_4$ input*1		
	$TMRI_1$ input			

TPU Channel 4 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_4$ input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 to IOA0 = B'10xx.

2. $TIOCB_4$ output is disabled.

Bit 0—Address 20 Enable (A20E): Enables or disables address output 20 (A_{20}). This bit is valid in modes 4 to 6.

Bit 0 A20E	Description	
0	DR is output when PA4DDR = 1	
1	A_{20} is output when PA4DDR = 1	(Initial value)

System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Reserved: Only 0 should be written to this bit.

Bit 6—Reserved: This bit is always read as 0, and cannot be modified.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select either of two interrupt control modes for the interrupt controller. For details of the interrupt control modes, see section 5.4.1, Interrupt Control Modes and Interrupt Operation.

Bit 5 INTM1	Bit 4 INTM0	Interrupt Control Mode	Description	
0	0	0	Interrupt control by I bit	(Initial value)
	1	—	Setting prohibited	
1	0	2	Interrupt control by bits I2 to I0	
	1	—	Setting prohibited	

Bit 3—NMI Edge Select (NMIEG): Selects the input edge for the NMI pin.

Bit 3 NMIEG	Description	
0	Interrupt requested at falling edge of NMI input	(Initial value)
1	Interrupt requested at rising edge of NMI input	

9.9.4 MOS Input Pull-Up Function

Port B has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7, and can be specified as on or off on an individual bit basis.

When a PBDDR bit is cleared to 0 in mode 6 or 7, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 9.17 summarizes the MOS input pull-up states.

Table 9.17 MOS Input Pull-Up States (Port B)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 5	Off	Off	Off	Off
6, 7			On/off	On/off

Legend:

Off: MOS input pull-up is always off.

On/off: On when PBDDR = 0 and PBPCR = 1; otherwise off.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. For details, see section 9.6, Port 5.

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. For details, see section 9.6, Port 5.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output. Change the CS167E setting only when the DDR bits are cleared to 0.

Bit 5 CS167E	Description	
0	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output enabled	(Initial value)

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output. Change the CS25E setting only when the DDR bits are cleared to 0.

Bit 4 CS25E	Description	
0	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output enabled	(Initial value)

Bit 3—AS Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 9.13, Port F.

Bits 2 to 0—Reserved: These bits are always read as 0.

Contention between TCNT Write and Clear Operations: If the counter clear signal is generated in the T_2 state of a TCNT write cycle, TCNT clearing takes precedence and the TCNT write is not performed.

Figure 10.49 shows the timing in this case.

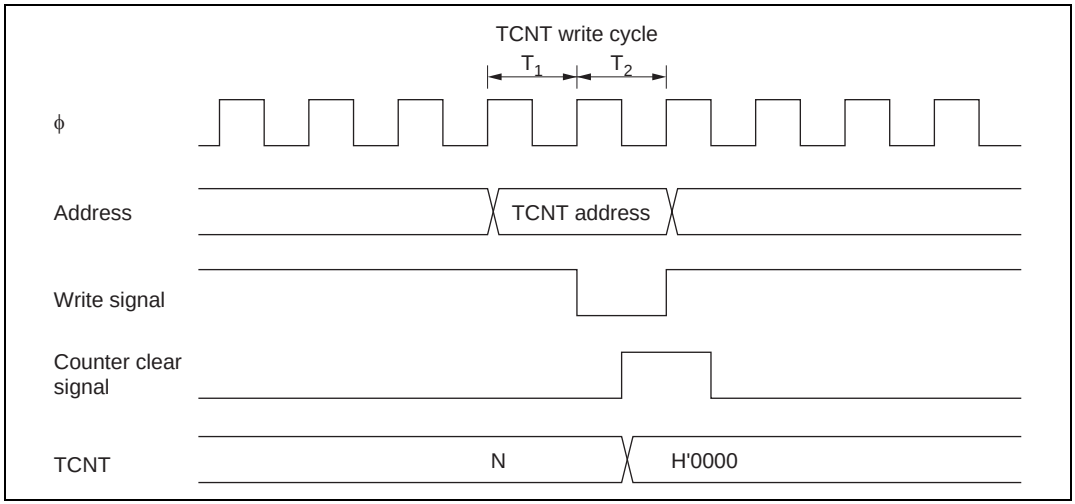

Figure 10.49 Contention between TCNT Write and Clear Operations

Contention between TGR Write and Input Capture: If the input capture signal is generated in the T_2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 10.54 shows the timing in this case.

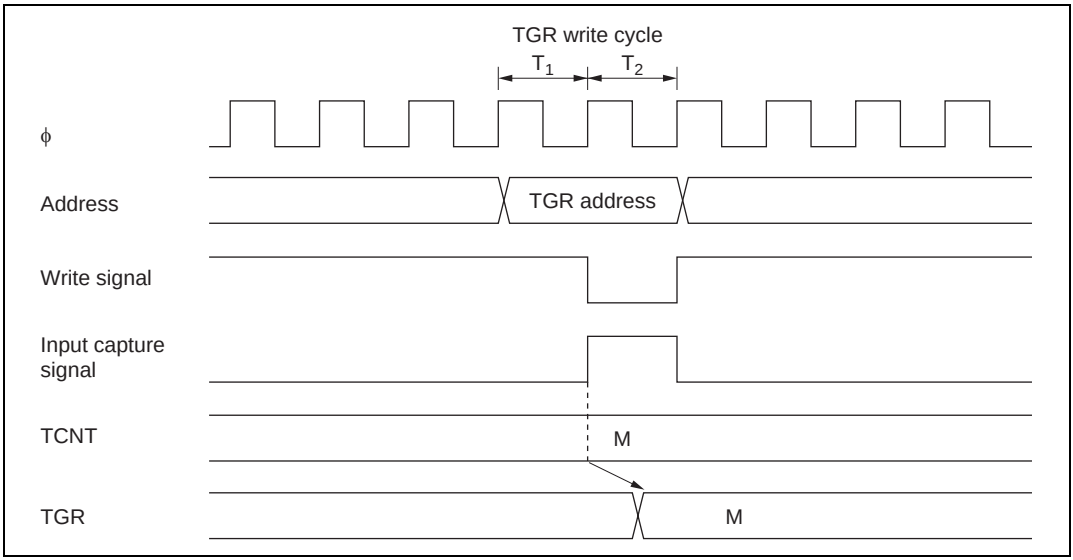

Figure 10.54 Contention between TGR Write and Input Capture

13.4 Interrupts

During interval timer mode operation, an overflow generates an interval timer interrupt (WOVI). The interval timer interrupt is requested whenever the OVF flag is set to 1 in TCSR.

13.5 Usage Notes

13.5.1 Contention between Timer Counter (TCNT) Write and Increment

If a timer counter clock pulse is generated during the T_2 state of a TCNT write cycle, the write takes priority and the timer counter is not incremented. Figure 13.8 shows this operation.

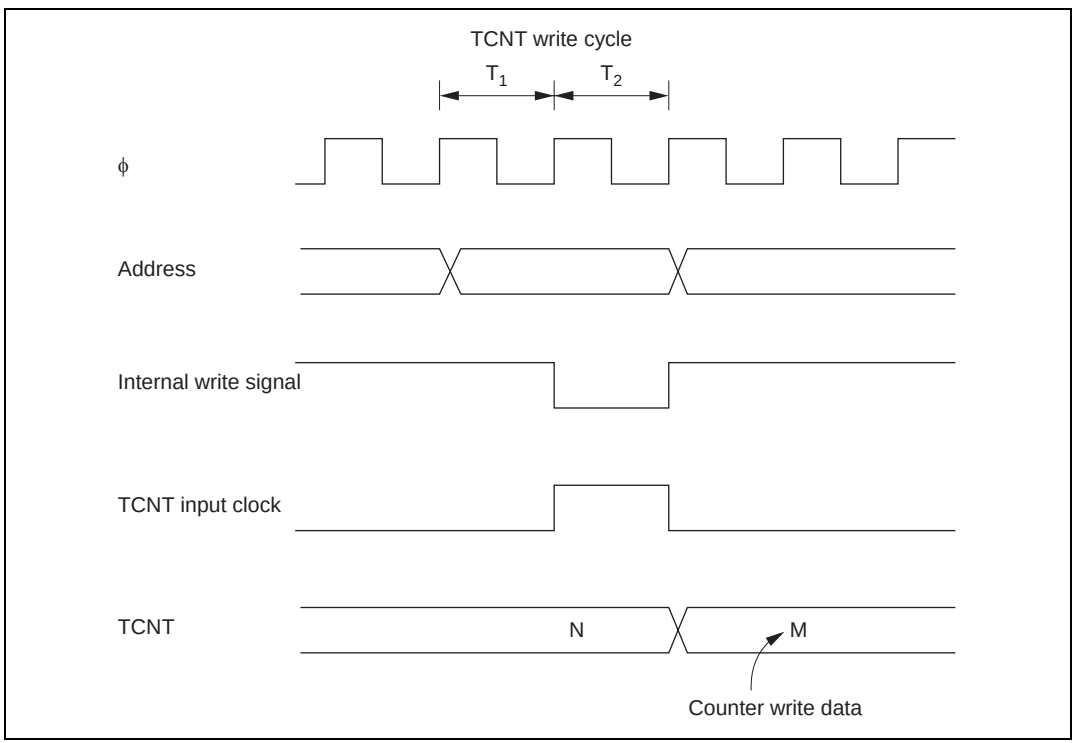

Figure 13.8 Contention between TCNT Write and Increment

Influences on Absolute Precision: Adding capacitance results in coupling with GND, and therefore noise in GND may adversely affect absolute precision. Be sure to make the connection to an electrically stable GND such as AV_{SS}.

Care is also required to insure that filter circuits do not communicate with digital signals on the mounting board, so acting as antennas.

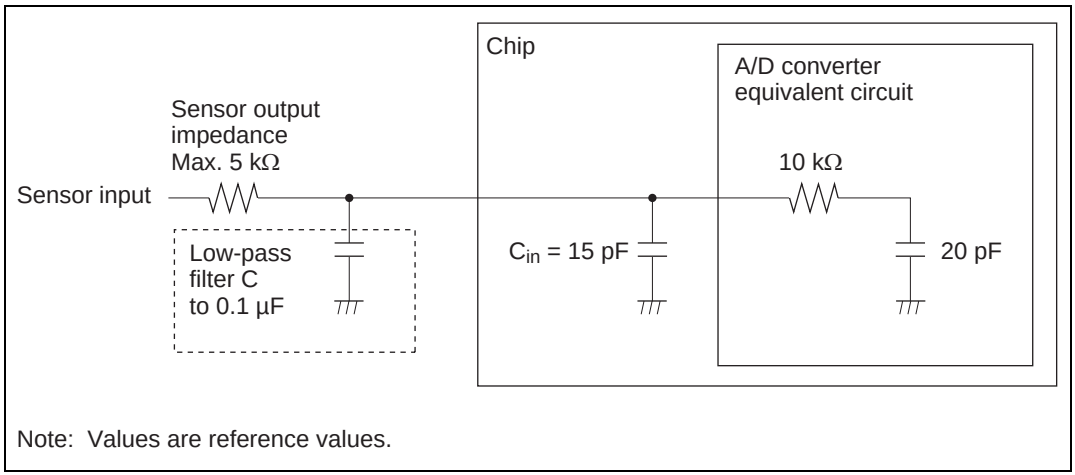

Figure 16.10 Example of Analog Input Circuit

19.2.2 Bus Control Register L (BCRL)

Bit	:	7	6	5	4	3	2	1	0
		BRLE	BREQOE	EAE	—	DDS	—	WDBE	WAITE
Initial value	:	0	0	1	1	1	1	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Enabling or disabling of part of the on-chip ROM area in the chip can be selected by means of the EAE bit in BCRL. For details of the other bits in BCRL, see section 6.2.5, Bus Control Register L (BCRL).

Bit 5—External Address Enable (EAE): Selects whether addresses H'010000 to H'03FFFF*2 are to be internal addresses or external addresses.

	Description		
Bit 5	**H8S/2329B, H8S/2328*3, H8S/2326**	**H8S/2327**	**H8S/2323**
0	On-chip ROM	Addresses H'010000 to H'01FFFF are on-chip ROM or address H'020000 to H'03FFFF are reserved area*1	Reserved area*1
1	Addresses H'010000 to H'03FFFF*2 are external addresses in external expanded mode or reserved area*1 in single-chip mode (Initial value)		

Notes: 1. Do not access a reserved area.
2. Addresses H'010000 to H'05FFFF in the H8S/2329B.
Addresses H'010000 to H'07FFFF in the H8S/2326.
3. H8S/2328B in flash memory version.

19.3 Operation

The on-chip ROM is connected to the CPU by a 16-bit data bus, and both byte and word data can be accessed in one state. Even addresses are connected to the upper 8 bits, and odd addresses to the lower 8 bits. Word data must start at an even address.

The on-chip ROM is enabled and disabled by setting the mode pins (MD2 to MD0) and the EAE bit in BCRL. These settings are shown in tables 19.2 and 19.3.

(3) Bus Timing

Table 22.7 Bus Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figures 22.6 to 22.13
Address setup time	t_{AS}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 15	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 10	—	0.5 × t_{cyc} – 8	—	ns	
Precharge time*	t_{PCH}	1.5 × t_{cyc}– 20	—	1.5 × t_{cyc}– 15	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{CS}$ delay time 2*	t_{CSD2}	—	20	—	15	ns	
$\overline{CS}$ delay time 3*	t_{CSD3}	—	25	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
$\overline{CAS}$ delay time*	t_{CASD}	—	20	—	15	ns	
Read data setup time	t_{RDS}	15	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	
Read data access time 2	t_{ACC2}	—	1.5 × t_{cyc} – 25	—	1.5 × t_{cyc} – 20	ns	
Read data access time 3	t_{ACC3}	—	2.0 × t_{cyc} – 25	—	2.0 × t_{cyc} – 20	ns	
Read data access time 4	t_{ACC4}	—	2.5 × t_{cyc} – 25	—	2.5 × t_{cyc} – 20	ns	
Read data access time 5	t_{ACC5}	—	3.0 × t_{cyc} – 25	—	3.0 × t_{cyc} – 20	ns	
Read data access time 6*	t_{ACC6}	—	1.0 × t_{cyc} – 25	—	1.0 × t_{cyc} – 20	ns	

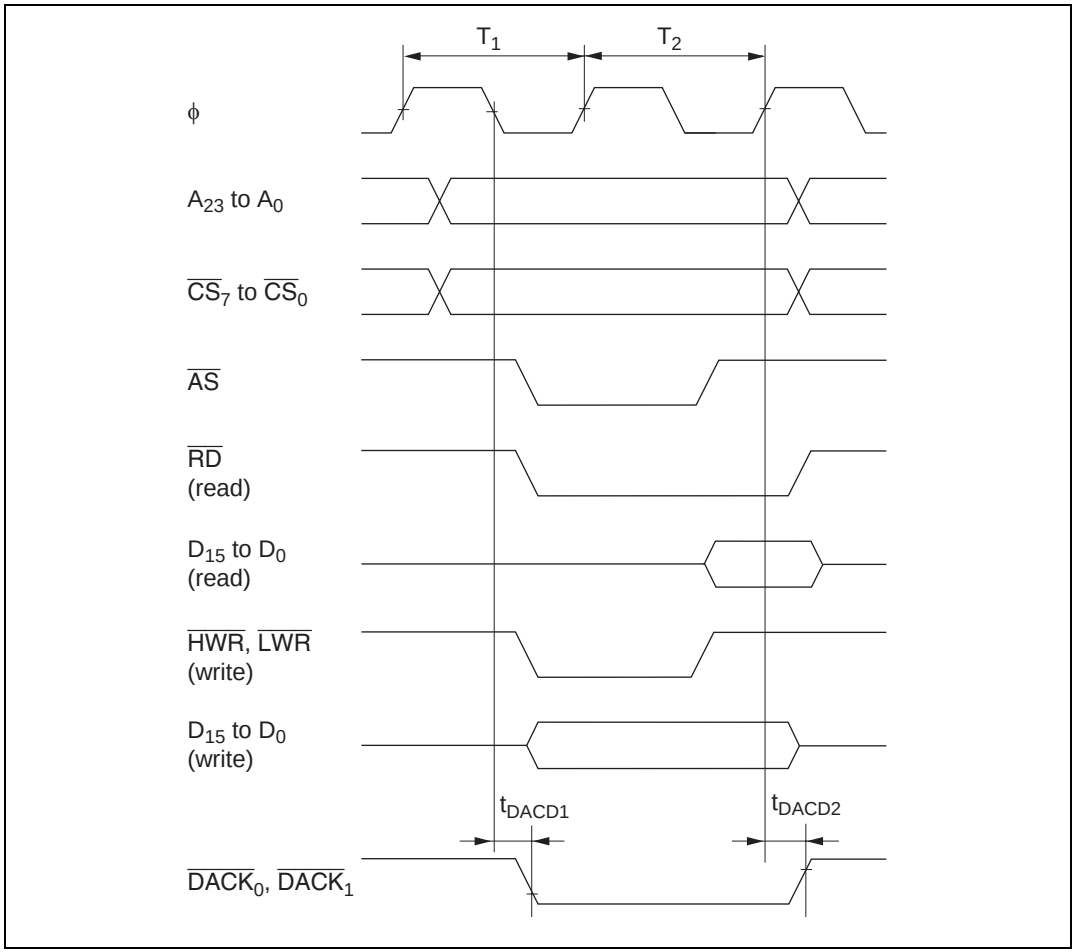

Figure 22.16 DMAC Single Address Transfer Timing (2-State Access)

DRAMCR—DRAM Control Register H'FED7 Bus Controller
(Not supported in H8S/2321)

Bit	7	6	5	4	3	2	1	0
	RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Refresh Counter Clock Select

0	0	0	Count operation disabled
		1	Count uses ϕ/2
	1	0	Count uses ϕ/8
		1	Count uses ϕ/32
1	0	0	Count uses ϕ/128
		1	Count uses ϕ/512
	1	0	Count uses ϕ/2048
		1	Count uses ϕ/4096

Compare Match Interrupt Enable

0	Interrupt request (CMI) by CMF flag disabled
1	Interrupt request (CMI) by CMF flag enabled

Compare Match Flag

0	[Clearing condition] When 0 is written to CMF after reading CMF = 1
1	[Setting condition] When RTCNT = RTCOR

Refresh Mode

0	Self-refreshing is not performed in software standby mode
1	Self-refreshing is performed in software standby mode

RAS-CAS Wait

0	Wait state insertion in CAS-before-RAS refreshing disabled $\overline{RAS}$ falls in T_r cycle
1	One wait state inserted in CAS-before-RAS refreshing $\overline{RAS}$ falls in T_{c1} cycle

Refresh Control

0	Refresh control is not performed
1	Refresh control is performed

SMR2—Serial Mode Register 2 **H'FF88** **SCI2**

Bit :	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ϕ clock
	1	ϕ/4 clock
1	0	ϕ/16 clock
	1	ϕ/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

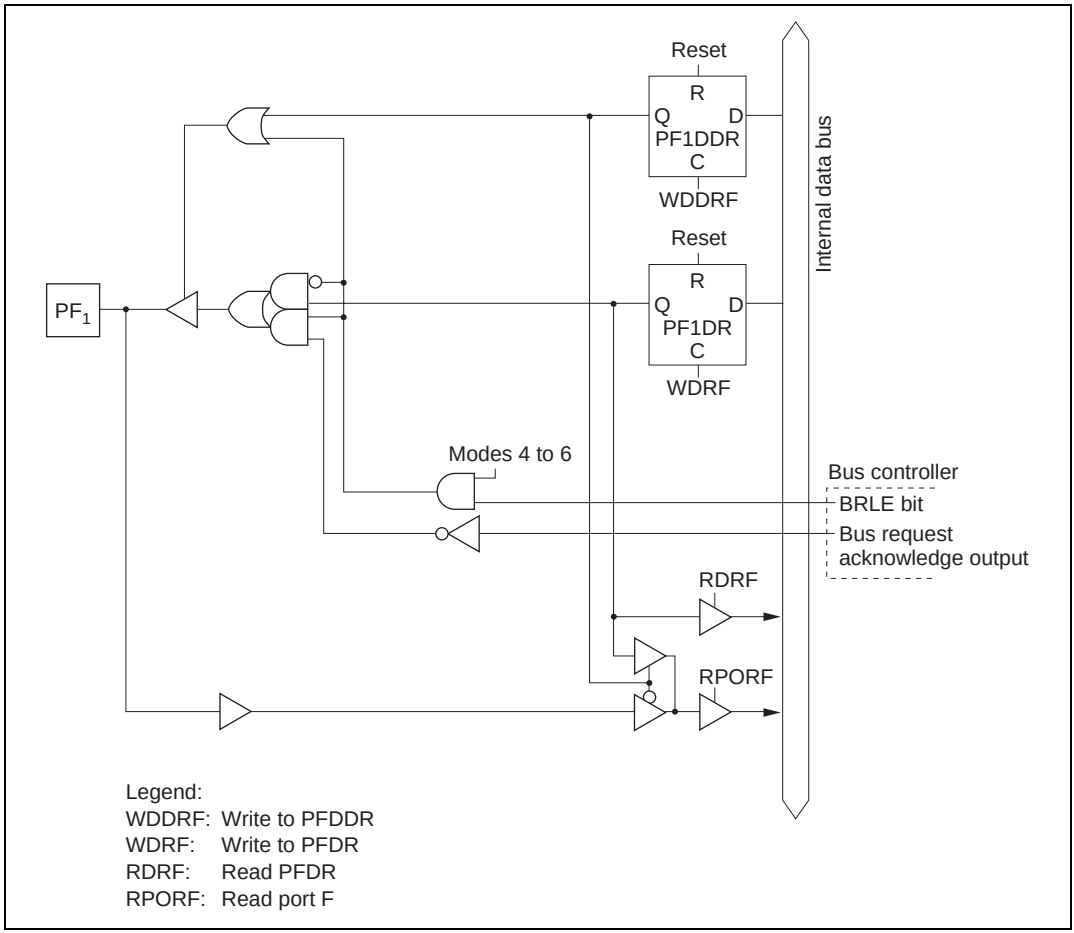

Figure C.12 (b) Port F Block Diagram (Pin PF_1)