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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2326vte25v

1.3.3 Pin Functions

Table 1.3 Pin Functions

Type	Symbol	Pin No. TFP-120	Pin No. FP-128B	I/O	Name and Function
Power	V_{CC}	1, 33, 52, 76, 81	5, 39, 58, 84, 89	Input	**Power supply:** For connection to the power supply. All V_{CC} pins should be connected to the system power supply.
	V_{SS}	6, 15, 24, 38, 47, 59, 79, 104	3, 10, 19, 28, 35, 36, 44, 53, 65, 67, 68, 87, 99, 100, 114	Input	**Ground:** For connection to ground (0 V). All V_{SS} pins should be connected to the system power supply (0 V).
Clock	XTAL	77	85	Input	Connects to a crystal resonator. See section 20, Clock Pulse Generator for typical connection diagrams for a crystal resonator and external clock input.
	EXTAL	78	86	Input	Connects to a crystal resonator. The EXTAL pin can also input an external clock. See section 20, Clock Pulse Generator for typical connection diagrams for a crystal resonator and external clock input.
	ϕ	80	88	Output	**System clock:** Supplies the system clock to an external device.

2.6 Instruction Set

2.6.1 Overview

The H8S/2000 CPU has 65 types of instructions. The instructions are classified by function in table 2.1.

Table 2.1 Instruction Classification

Function	Instructions	Size	Types
Data transfer	MOV	BWL	5
	POP*1, PUSH*1	WL	
	LDM, STM	L	
	MOVFPE, MOVTPE*3	B	
Arithmetic operations	ADD, SUB, CMP, NEG	BWL	19
	ADDX, SUBX, DAA, DAS	B	
	INC, DEC	BWL	
	ADDS, SUBS	L	
	MULXU, DIVXU, MULXS, DIVXS	BW	
	EXTU, EXTS	WL	
	TAS*4	B	
Logic operations	AND, OR, XOR, NOT	BWL	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	BWL	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BLD, BILD, BST, BIST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR	B	14
Branch	Bcc*2, JMP, BSR, JSR, RTS	—	5
System control	TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	—	9
Block data transfer	EEPMOV	—	1
		Total:	65

Legend:
B: Byte
W: Word
L: Longword

Notes: 1. POP.W Rn and PUSH.W Rn are identical to MOV.W @SP+, Rn and MOV.W Rn, @-SP. POP.L ERn and PUSH.L ERn are identical to MOV.L @SP+, ERn and MOV.L ERn, @-SP.
2. Bcc is the general name for conditional branch instructions.
3. Cannot be used in the H8S/2329 Group and H8S/2328 Group.
4. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.

Table 4.2 Exception Vector Table

Exception Source		Vector Number	Vector Address[*1] Advanced Mode
Reset		0	H'0000 to H'0003
Reserved		1	H'0004 to H'0007
Reserved for system use		2	H'0008 to H'000B
		3	H'000C to H'000F
		4	H'0010 to H'0013
Trace		5	H'0014 to H'0017
Reserved for system use		6	H'0018 to H'001B
External interrupt	NMI	7	H'001C to H'001F
Trap instruction (4 sources)		8	H'0020 to H'0023
		9	H'0024 to H'0027
		10	H'0028 to H'002B
		11	H'002C to H'002F
Reserved for system use		12	H'0030 to H'0033
		13	H'0034 to H'0037
		14	H'0038 to H'003B
		15	H'003C to H'003F
External interrupt	IRQ0	16	H'0040 to H'0043
	IRQ1	17	H'0044 to H'0047
	IRQ2	18	H'0048 to H'004B
	IRQ3	19	H'004C to H'004F
	IRQ4	20	H'0050 to H'0053
	IRQ5	21	H'0054 to H'0057
	IRQ6	22	H'0058 to H'005B
	IRQ7	23	H'005C to H'005F
Internal interrupt[*2]		24 | 91	H'0060 to H'0063 | H'016C to H'016F

Notes: 1. Lower 16 bits of the address.

2. For details of internal interrupt vectors, see section 5.3.3, Interrupt Exception Vector Table.

5.2.4 IRQ Sense Control Registers H and L (ISCRH, ISCRL)

ISCRH

Bit	:	15	14	13	12	11	10	9	8
		IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISCRL

Bit	:	7	6	5	4	3	2	1	0
		IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISCR (composed of ISCRH and ISCRL) is a 16-bit readable/writable register that selects rising edge, falling edge, or both edge detection, or level sensing, for the input at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.

ISCR is initialized to H'0000 by a reset and in hardware standby mode.

Bits 15 to 0—IRQ7 Sense Control A and B (IRQ7SCA, IRQ7SCB) to IRQ0 Sense Control A and B (IRQ0SCA, IRQ0SCB)

Bits 15 to 0

IRQ7SCB to IRQ0SCB	IRQ7SCA to IRQ0SCA	Description
0	0	Interrupt request generated at $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input low level (Initial value)
	1	Interrupt request generated at falling edge of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input
1	0	Interrupt request generated at rising edge of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input
	1	Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input

Bit 6—Data Transfer Enable 1A (DTE1A): Enables or disables data transfer on channel 1A.

Bit 6 DTE1A	Description	
0	Data transfer disabled	(Initial value)
1	Data transfer enabled	

Bit 5—Data Transfer Enable 0B (DTE0B): Enables or disables data transfer on channel 0B.

Bit 5 DTE0B	Description	
0	Data transfer disabled	(Initial value)
1	Data transfer enabled	

Bit 4—Data Transfer Enable 0A (DTE0A): Enables or disables data transfer on channel 0A.

Bit 4 DTE0A	Description	
0	Data transfer disabled	(Initial value)
1	Data transfer enabled	

Bits 3 to 0—Data Transfer End Interrupt Enable (DTIE): These bits enable or disable an interrupt to the CPU or DTC when transfer ends. If the DTIE bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC.

A transfer end interrupt can be canceled either by clearing the DTIE bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the transfer counter and address register again, and then setting the DTE bit to 1.

Bit 3—Data Transfer Interrupt Enable 1B (DTIE1B): Enables or disables the channel 1B transfer end interrupt.

Bit 3 DTIE1B	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

SYSCR is an 8-bit readable/writable register that selects the interrupt control mode, controls the $\overline{\text{LWR}}$ pin, switches the $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input pins, and selects the detected edge for NMI. SYSCR is initialized to H'01 by a reset, and in hardware standby mode. It is not initialized in software standby mode.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select either of two interrupt control modes for the interrupt controller. For details, see section 5, Interrupt Controller.

Bit 3—NMI Edge Select (NMIEG): Selects the input edge for the NMI pin. For details, see section 5, Interrupt Controller.

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output. For details, see section 9.13, Port F.

Bit 1—IRQ Port Switching Select (IRQPAS): Selects switching of input pins for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$. $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input is always performed from one of the ports.

Bit 1 IRQPAS	Description	
0	PA_4 to PA_7 used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	(Initial value)
1	$P5_0$ to $P5_3$ used for $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_7$ input	

Bit 0—RAM Enable (RAME): Enables or disables on-chip RAM. For details, see section 18, RAM.

9.11.2 Register Configuration

Table 9.20 shows the port D register configuration.

Table 9.20 Port D Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port D data direction register	PDDDR	W	H'00	H'FEBC
Port D data register	PDDR	R/W	H'00	H'FF6C
Port D register	PORTD	R	Undefined	H'FF5C
Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FF73

Note: * Lower 16 bits of the address.

Port D Data Direction Register (PDDDR)

Bit	:	7	6	5	4	3	2	1	0
		PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PDDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port D. PDDDR cannot be read; if it is, an undefined value will be read.

PDDDR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 4 to 6

  The input/output direction specification by PDDDR is ignored, and port D is automatically designated for data I/O.

- Mode 7

  Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Bit 3—Input Capture/Output Compare Flag D (TGFD): Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0 and 3.

In channels 1, 2, 4, and 5, bit 3 is reserved. It is always read as 0 and cannot be modified.

Bit 3 TGFD	Description
0	[Clearing conditions] (Initial value) • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Bit 2—Input Capture/Output Compare Flag C (TGFC): Status flag that indicates the occurrence of TGRC input capture or compare match in channels 0 and 3.

In channels 1, 2, 4, and 5, bit 2 is reserved. It is always read as 0 and cannot be modified.

Bit 2 TGFC	Description
0	[Clearing conditions] (Initial value) • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Examples of Cascaded Operation: Figure 10.22 illustrates the operation when counting upon TCNT2 overflow/underflow has been set for TCNT1, TGR1A, and TGR2A have been designated as input capture registers, and TIOC pin rising edge has been selected.

When a rising edge is input to the TIOCA1 and TIOCA2 pins simultaneously, the upper 16 bits of the 32-bit data are transferred to TGR1A, and the lower 16 bits to TGR2A.

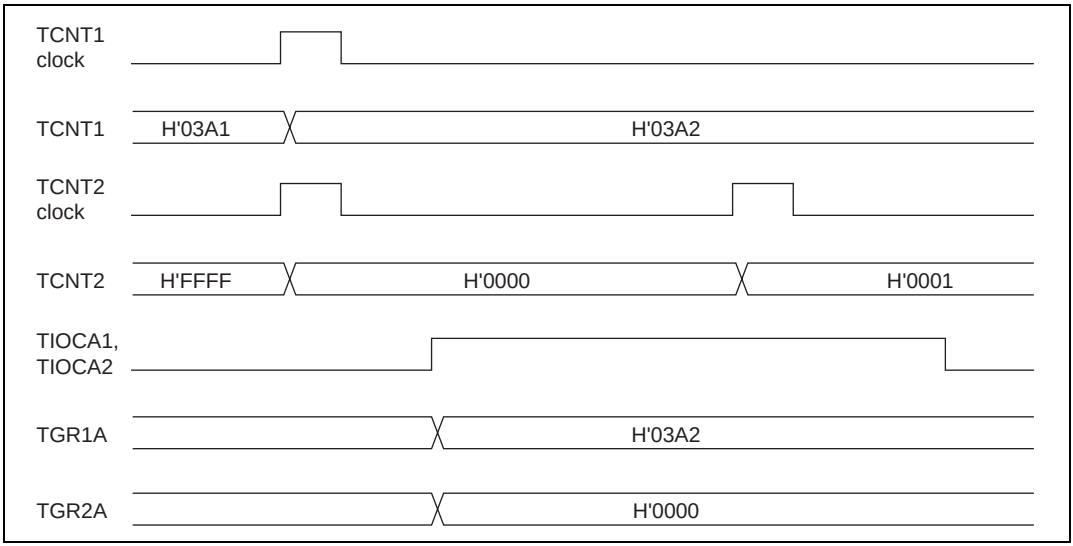


Figure 10.22 Example of Cascaded Operation (1)

Figure 10.23 illustrates the operation when counting upon TCNT2 overflow/underflow has been set for TCNT1, and phase counting mode has been designated for channel 2.

TCNT1 is incremented by TCNT2 overflow and decremented by TCNT2 underflow.

11.3.5 Inverted Pulse Output

If the G3INV, G2INV, G1INV, and G0INV bits in PMR are cleared to 0, values that are the inverse of the PODR contents can be output.

Figure 11.8 shows the outputs when G3INV and G2INV are cleared to 0, in addition to the settings of figure 11.7.

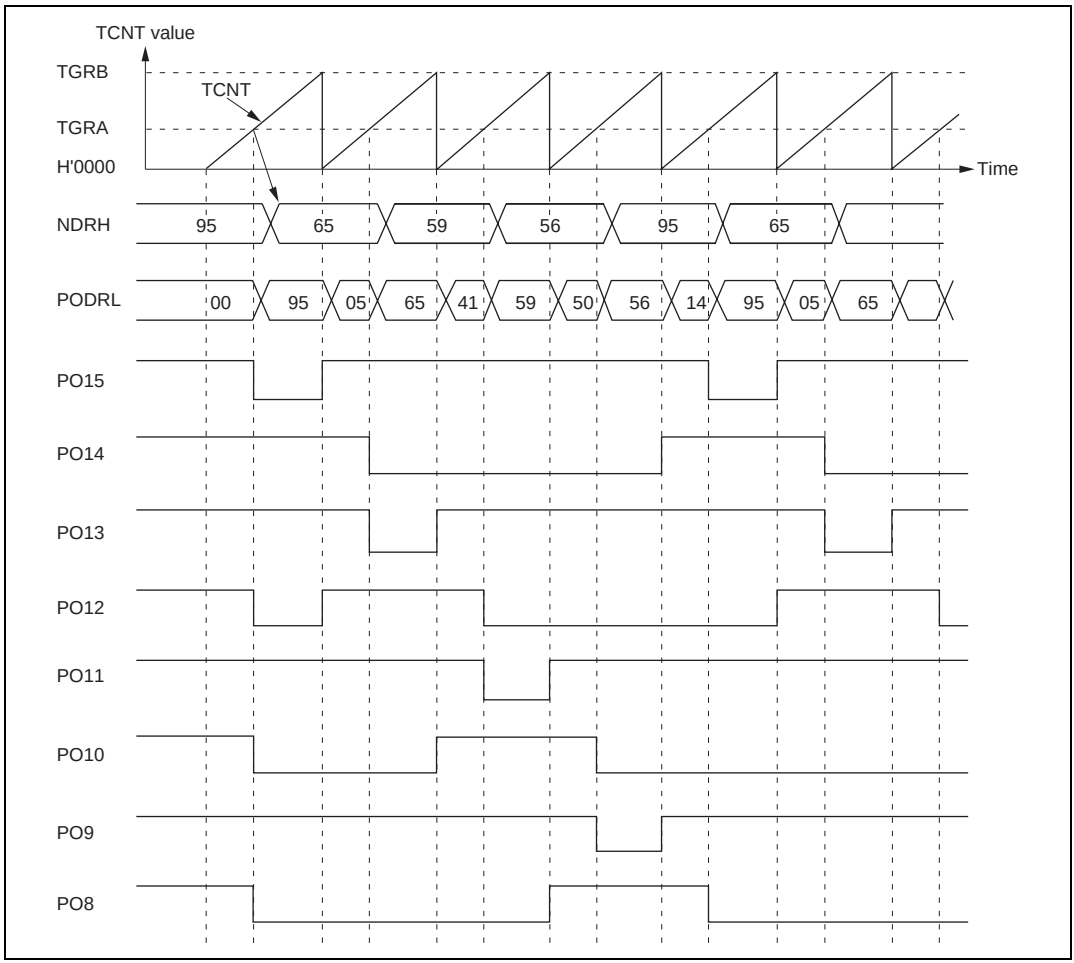


Figure 11.8 Inverted Pulse Output (Example)

13.2.3 Reset Control/Status Register (RSTCSR)

Bit	:	7	6	5	4	3	2	1	0
		WOVF	RSTE	—	—	—	—	—	—
Initial value	:	0	0	0	1	1	1	1	1
R/W	:	R/(W)*	R/W	R/W	—	—	—	—	—

Note: * Only 0 can be written, to clear the flag.

RSTCSR is an 8-bit readable/writable* register that controls the generation of the internal reset signal when TCNT overflows, and selects the type of internal reset signal.

RSTCSR is initialized to H'1F by a reset signal from the $\overline{\text{RES}}$ pin, but not by the WDT internal reset signal caused by overflows.

Note: * RSTCSR is write-protected by a password to prevent accidental overwriting. For details see section 13.2.4, Notes on Register Access.

Bit 7—Watchdog Timer Overflow Flag (WOVF): Indicates that TCNT has overflowed (changed from H'FF to H'00) during watchdog timer operation. This bit is not set in interval timer mode.

Bit 7 WOVF	Description	
0	[Clearing condition]	(Initial value)
	Cleared by reading RSTCSR when WOVF = 1, then writing 0 to WOVF	
1	[Setting condition]	
	Set when TCNT overflows (changes from H'FF to H'00) during watchdog timer operation	

Bit 6—Reset Enable (RSTE): Specifies whether or not a reset signal is generated in the chip if TCNT overflows during watchdog timer operation.

Bit 6 RSTE	Description	
0	Reset signal is not generated if TCNT overflows*	(Initial value)
1	Reset signal is generated if TCNT overflows	

Note: * The modules within the chip are not reset, but TCNT and TCSR within the WDT are reset.

16.2 Register Descriptions

16.2.1 A/D Data Registers A to D (ADDRA to ADDRD)

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

There are four 16-bit read-only ADDR registers, ADDRA to ADDRD, used to store the results of A/D conversion.

The 10-bit data resulting from A/D conversion is transferred to the ADDR register for the selected channel and stored there. The upper 8 bits of the converted data are transferred to the upper byte (bits 15 to 8) of ADDR, and the lower 2 bits are transferred to the lower byte (bits 7 and 6) and stored. Bits 5 to 0 are always read as 0.

The correspondence between the analog input channels and ADDR registers is shown in table 16.3.

The ADDR registers can always be read by the CPU. The upper byte can be read directly, but for the lower byte, data transfer is performed via a temporary register (TEMP). For details, see section 16.3, Interface to Bus Master.

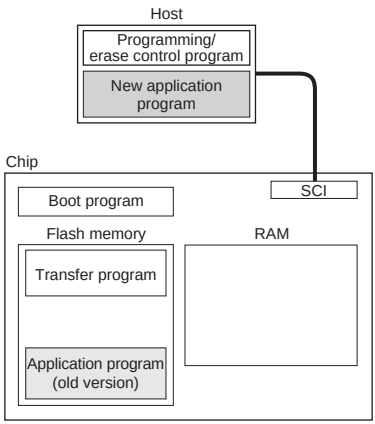
The ADDR registers are initialized to H'0000 by a reset, and in standby mode or module stop mode.

Table 16.3 Analog Input Channels and Corresponding ADDR Registers

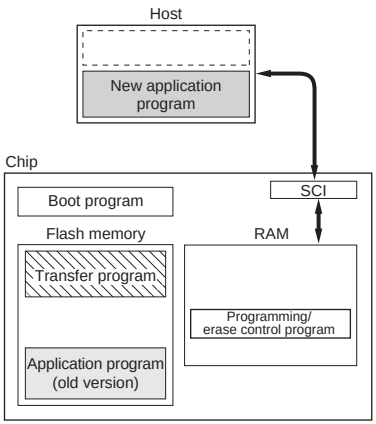
Analog Input Channel		
Group 0	**Group 1**	**A/D Data Register**
AN0	AN4	ADDRA
AN1	AN5	ADDRB
AN2	AN6	ADDRC
AN3	AN7	ADDRD

- User program mode

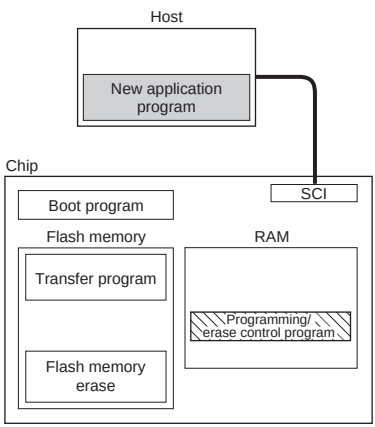
1. Initial state
   (1) The program that will transfer the programming/erase control program to on-chip RAM should be written into the flash memory by the user beforehand. (2) The programming/erase control program should be prepared in the host or in the flash memory.



2. Programming/erase control program transfer
   Executes the transfer program in the flash memory, and transfers the programming/erase control program to RAM.



3. Flash memory initialization
   The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.



4. Writing new application program
   Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.

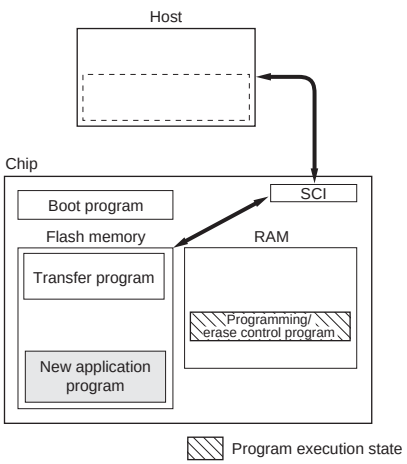


Figure 19.5 User Program Mode (Example)

Bit 2—Program-Verify 1 (PV1): Selects program-verify mode transition or clearing for addresses H'000000 to H'03FFFF. Do not set the SWE1, ESU1, PSU1, EV1, E1, or P1 bit at the same time.

Bit 2 PV1	Description	
0	Program-verify mode cleared	(Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1, SWE1 = 1	

Bit 1—Erase 1 (E1): Selects erase mode transition or clearing for addresses H'000000 to H'03FFFF. Do not set the SWE1, ESU1, PSU1, EV1, PV1, or P1 bit at the same time.

Bit 1 E1	Description	
0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE1 = 1, and ESU1 = 1	

Bit 0—Program 1 (P1): Selects program mode transition or clearing for addresses H'000000 to H'03FFFF. Do not set the SWE1, PSU1, ESU1, EV1, PV1, or E1 bit at the same time.

Bit 0 P1	Description	
0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE1 = 1, and PSU1 = 1	

(2) Control Signal Timing

Table 22.6 Control Signal Timing

Condition A: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 20 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition A		Condition B			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 22.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 22.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

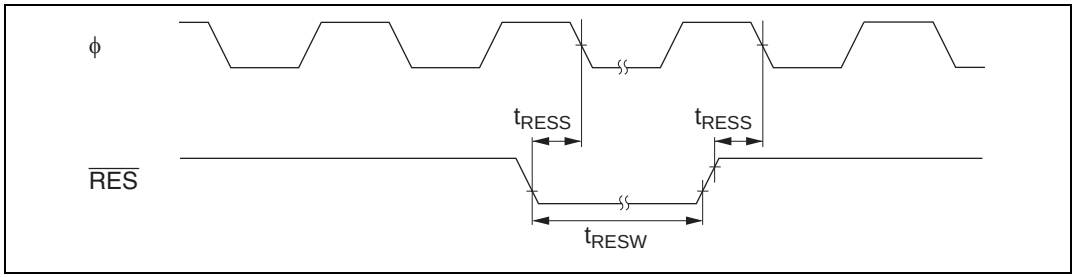


Figure 22.4 Reset Input Timing

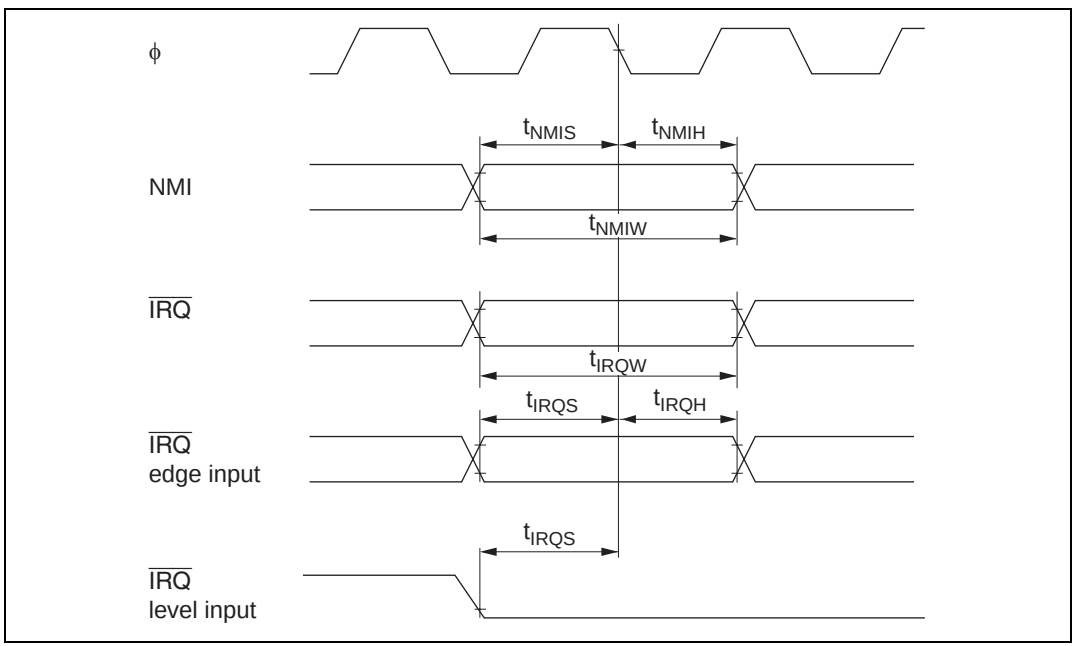


Figure 22.5 Interrupt Input Timing

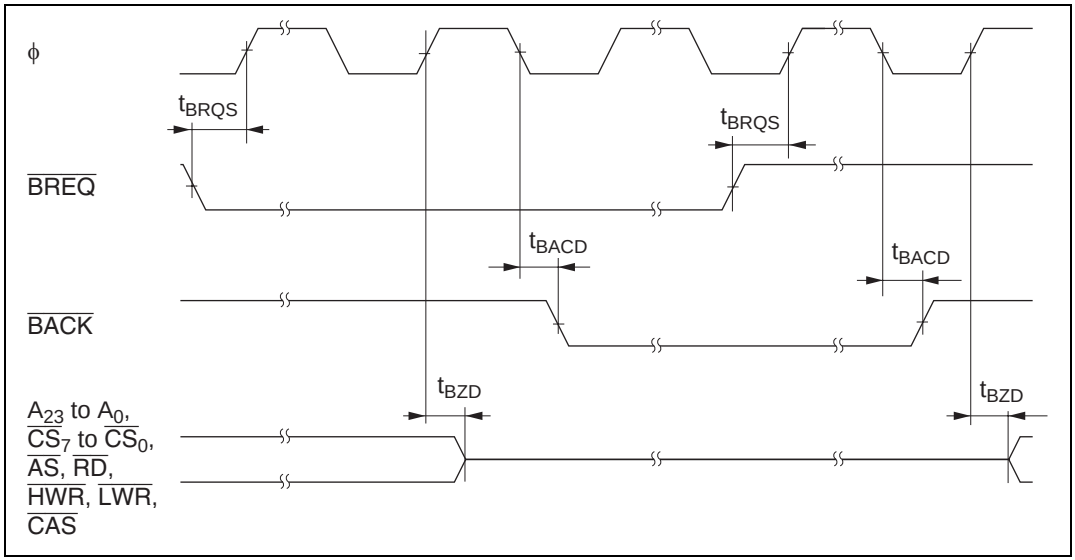


Figure 22.14 External Bus Release Timing

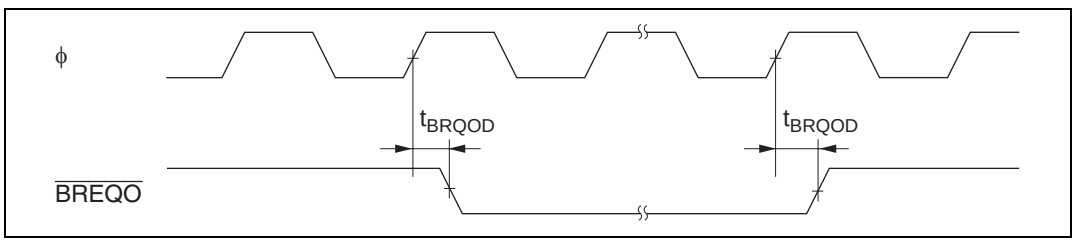


Figure 22.15 External Bus Request Output Timing

(2) Control Signal Timing

Table 22.16 Control Signal Timing

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

		Condition B			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	ns	Figure 22.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	ns	Figure 22.5
NMI hold time	t_{NMIH}	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—		

Mnemonic	Operand Size	Addressing Mode/ Instruction Length (Bytes)								Operation	Condition Code						No. of States*1
		#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa		I	H	N	Z	V	C	Advanced
BCLR	BCLR Rn,@aa:32	B					8			(Rn8 of @aa:32)←0	—	—	—	↕	—	—	6
BNOT	BNOT #xx:3,Rd	B	2							(#xx:3 of Rd8)←[¬ (#xx:3 of Rd8)]	—	—	—	↕	—	—	1
	BNOT #xx:3,@ERd	B		4						(#xx:3 of @ERd)←[¬ (#xx:3 of @ERd)]	—	—	—	↕	—	—	4
	BNOT #xx:3,@aa:8	B					4			(#xx:3 of @aa:8)←[¬ (#xx:3 of @aa:8)]	—	—	—	↕	—	—	4
	BNOT #xx:3,@aa:16	B					6			(#xx:3 of @aa:16)←[¬ (#xx:3 of @aa:16)]	—	—	—	↕	—	—	5
	BNOT #xx:3,@aa:32	B					8			(#xx:3 of @aa:32)←[¬ (#xx:3 of @aa:32)]	—	—	—	↕	—	—	6
	BNOT Rn,Rd	B	2							(Rn8 of Rd8)←[¬ (Rn8 of Rd8)]	—	—	—	↕	—	—	1
	BNOT Rn,@ERd	B		4						(Rn8 of @ERd)←[¬ (Rn8 of @ERd)]	—	—	—	↕	—	—	4
	BNOT Rn,@aa:8	B					4			(Rn8 of @aa:8)←[¬ (Rn8 of @aa:8)]	—	—	—	↕	—	—	4
	BNOT Rn,@aa:16	B					6			(Rn8 of @aa:16)←[¬ (Rn8 of @aa:16)]	—	—	—	↕	—	—	5
	BNOT Rn,@aa:32	B					8			(Rn8 of @aa:32)←[¬ (Rn8 of @aa:32)]	—	—	—	↕	—	—	6
BTST	BTST #xx:3,Rd	B	2							¬ (#xx:3 of Rd8)→Z	—	—	—	↕	—	—	1
	BTST #xx:3,@ERd	B		4						¬ (#xx:3 of @ERd)→Z	—	—	—	↕	—	—	3
	BTST #xx:3,@aa:8	B					4			¬ (#xx:3 of @aa:8)→Z	—	—	—	↕	—	—	3
	BTST #xx:3,@aa:16	B					6			¬ (#xx:3 of @aa:16)→Z	—	—	—	↕	—	—	4