Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2328bvf25wvtr

Type	Instruction	Size[*1]	Function
Arithmetic operations	DIVXS	B/W	Rd ÷ Rs → Rd Performs signed division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.
	CMP	B/W/L	Rd – Rs, Rd – #IMM Compares data in a general register with data in another general register or with immediate data, and sets CCR bits according to the result.
	NEG	B/W/L	0 – Rd → Rd Takes the two's complement (arithmetic complement) of data in a general register.
	EXTU	W/L	Rd (zero extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by padding with zeros on the left.
	EXTS	W/L	Rd (sign extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by extending the sign bit.
	TAS	B	@ERd – 0, 1 → (<bit 7> of @Erd)[*2] Tests memory contents, and sets the most significant bit (bit 7) to 1.

Table 4.2 Exception Vector Table

			Vector Address*1
Exception Source		**Vector Number**	**Advanced Mode**
Reset		0	H'0000 to H'0003
Reserved		1	H'0004 to H'0007
Reserved for system use		2	H'0008 to H'000B
		3	H'000C to H'000F
		4	H'0010 to H'0013
Trace		5	H'0014 to H'0017
Reserved for system use		6	H'0018 to H'001B
External interrupt	NMI	7	H'001C to H'001F
Trap instruction (4 sources)		8	H'0020 to H'0023
		9	H'0024 to H'0027
		10	H'0028 to H'002B
		11	H'002C to H'002F
Reserved for system use		12	H'0030 to H'0033
		13	H'0034 to H'0037
		14	H'0038 to H'003B
		15	H'003C to H'003F
External interrupt	IRQ0	16	H'0040 to H'0043
	IRQ1	17	H'0044 to H'0047
	IRQ2	18	H'0048 to H'004B
	IRQ3	19	H'004C to H'004F
	IRQ4	20	H'0050 to H'0053
	IRQ5	21	H'0054 to H'0057
	IRQ6	22	H'0058 to H'005B
	IRQ7	23	H'005C to H'005F
Internal interrupt*2		24	H'0060 to H'0063
		|	|
		91	H'016C to H'016F

Notes: 1. Lower 16 bits of the address.

2. For details of internal interrupt vectors, see section 5.3.3, Interrupt Exception Vector Table.

5.4.2 Interrupt Control Mode 0

Enabling and disabling of IRQ interrupts and on-chip supporting module interrupts can be set by means of the I bit in the CPU's CCR. Interrupts are enabled when the I bit is cleared to 0, and disabled when set to 1.

Figure 5.5 shows a flowchart of the interrupt acceptance operation in this case.

[1] If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.

[2] The I bit is then referenced. If the I bit is cleared to 0, the interrupt request is accepted. If the I bit is set to 1, only an NMI interrupt is accepted, and other interrupt requests are held pending.

[3] Interrupt requests are sent to the interrupt controller, the highest-ranked interrupt according to the priority system is accepted, and other interrupt requests are held pending.

[4] When an interrupt request is accepted, interrupt exception handling starts after execution of the current instruction has been completed.

[5] The PC and CCR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.

[6] Next, the I bit in CCR is set to 1. This masks all interrupts except NMI.

[7] A vector address is generated for the accepted interrupt, and execution of the interrupt handling routine starts at the address indicated by the contents of that vector address.

Section 6 Bus Controller

6.1 Overview

The chip has an on-chip bus controller (BSC) that manages the external address space divided into eight areas. The bus specifications, such as bus width and number of access states, can be set independently for each area, enabling multiple memories to be connected easily.

The bus controller also has a bus arbitration function, and controls the operation of the internal bus masters: the CPU, DMA controller (DMAC)*, and data transfer controller (DTC).

Note: * The DMAC is not supported in the H8S/2321.

6.1.1 Features

The features of the bus controller are listed below.

- Manages external address space in area units
  - In advanced mode, manages the external space as 8 areas of 2 Mbytes
  - Bus specifications can be set independently for each area
  - DRAM*/burst ROM interfaces can be set
- Basic bus interface
  - Chip select ($\overline{\text{CS0}}$ to $\overline{\text{CS7}}$) can be output for areas 0 to 7
  - 8-bit access or 16-bit access can be selected for each area
  - 2-state access or 3-state access can be selected for each area
  - Program wait states can be inserted for each area
- DRAM interface*
  - DRAM interface can be set for areas 2 to 5 (in advanced mode)
  - Row address/column address multiplexed output (8/9/10 bits)
  - 2-CAS access method
  - Burst operation (fast page mode)
  - T_P cycle insertion to secure RAS precharging time
  - Choice of CAS-before-RAS refreshing or self-refreshing
- Burst ROM interface
  - Burst ROM interface can be set for area 0
  - Choice of 1- or 2-state burst access

Bit 7—TP Cycle Control (TPC): Selects whether a 1-state or 2-state precharge cycle (T_P) is to be used when areas 2 to 5 designated as DRAM space are accessed.

Bit 7 TPC	Description	
0	1-state precharge cycle is inserted	(Initial value)
1	2-state precharge cycle is inserted	

Bit 6—Burst Access Enable (BE): Selects enabling or disabling of burst access to areas 2 to 5 designated as DRAM space. DRAM space burst access is performed in fast page mode.

Bit 6 BE	Description	
0	Burst disabled (always full access)	(Initial value)
1	For DRAM space access, access in fast page mode	

Bit 5—RAS Down Mode (RCDM): When areas 2 to 5 are designated as DRAM space and access to DRAM is interrupted, RCDM selects whether the next DRAM access is waited for with the $\overline{\text{RAS}}$ signal held low (RAS down mode), or the $\overline{\text{RAS}}$ signal is driven high again (RAS up mode).

Bit 5 RCDM	Description	
0	DRAM interface: RAS up mode selected	(Initial value)
1	DRAM interface: RAS down mode selected	

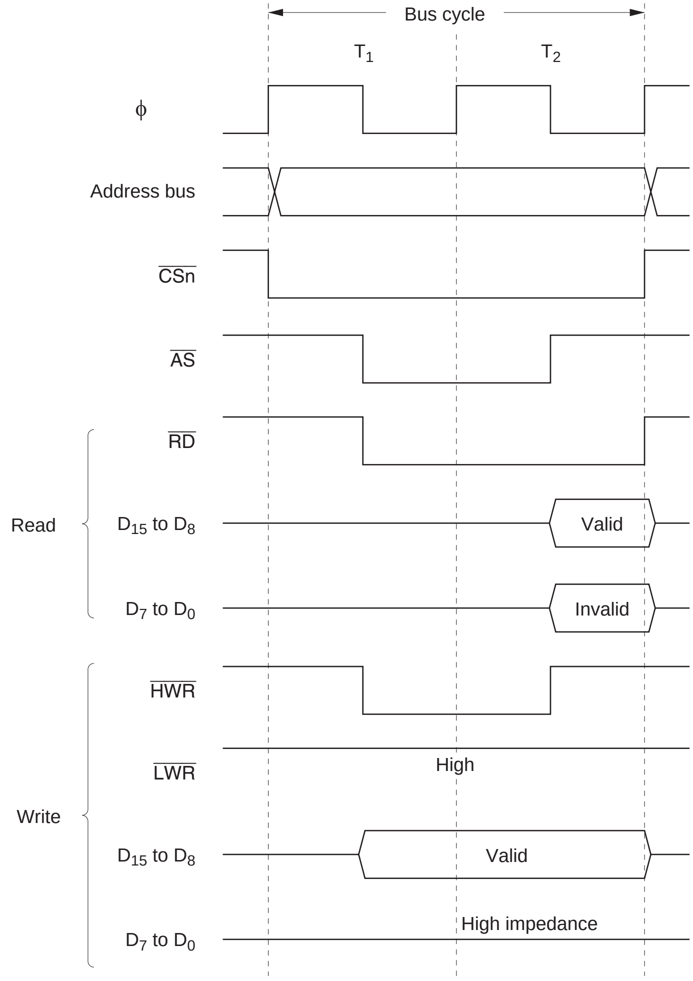
Bit 4—Reserved: Only 0 should be written to this bit.

Bits 3 and 2—Multiplex Shift Count 1 and 0 (MXC1, MXC0): These bits select the size of the shift to the lower half of the row address in row address/column address multiplexing for the DRAM interface. In burst operation on the DRAM interface, these bits also select the row address to be used for comparison.

6.4.4 Basic Timing

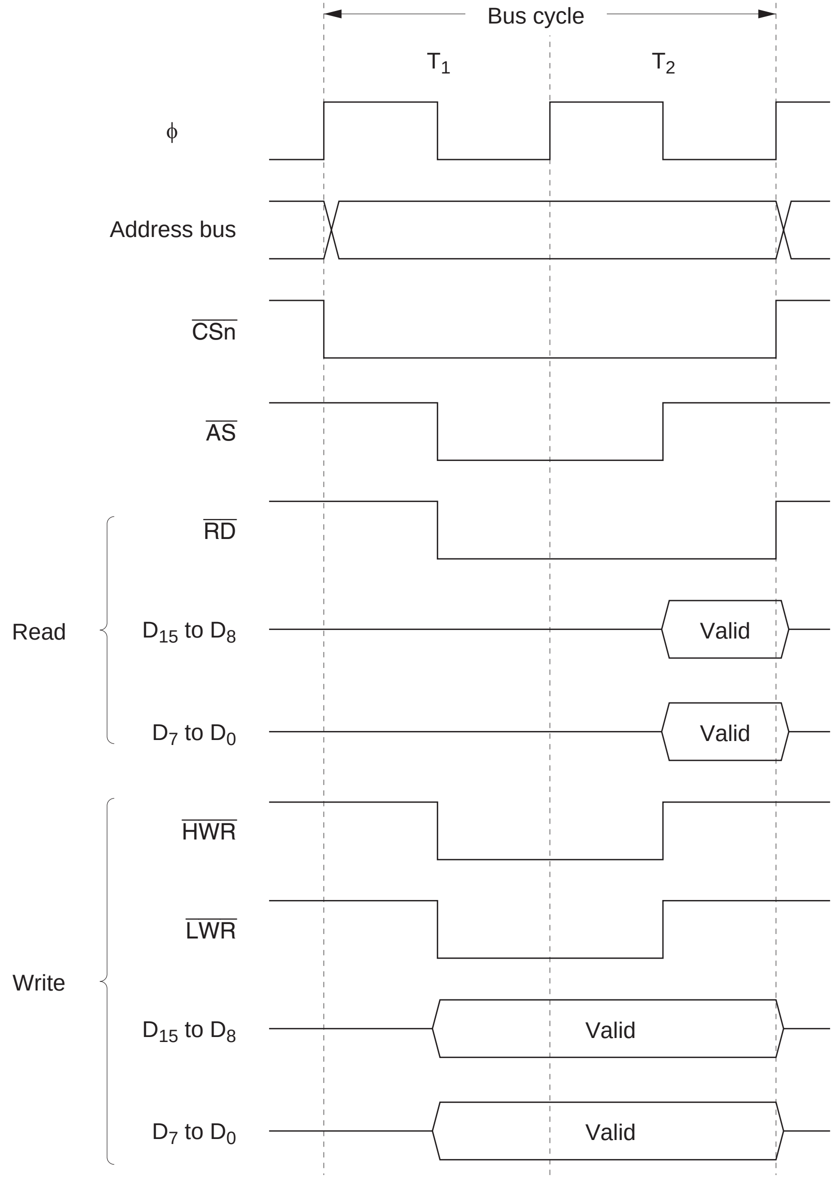
8-Bit 2-State Access Space: Figure 6.6 shows the bus timing for an 8-bit 2-state access space. When an 8-bit access space is accessed, the upper half (D_{15} to D_8) of the data bus is used.

The $\overline{\text{LWR}}$ pin is fixed high. Wait states cannot be inserted.



Note: n = 0 to 7

Figure 6.6 Bus Timing for 8-Bit 2-State Access Space



Note: n = 0 to 7

Figure 6.10 Bus Timing for 16-Bit 2-State Access Space (3) (Word Access)

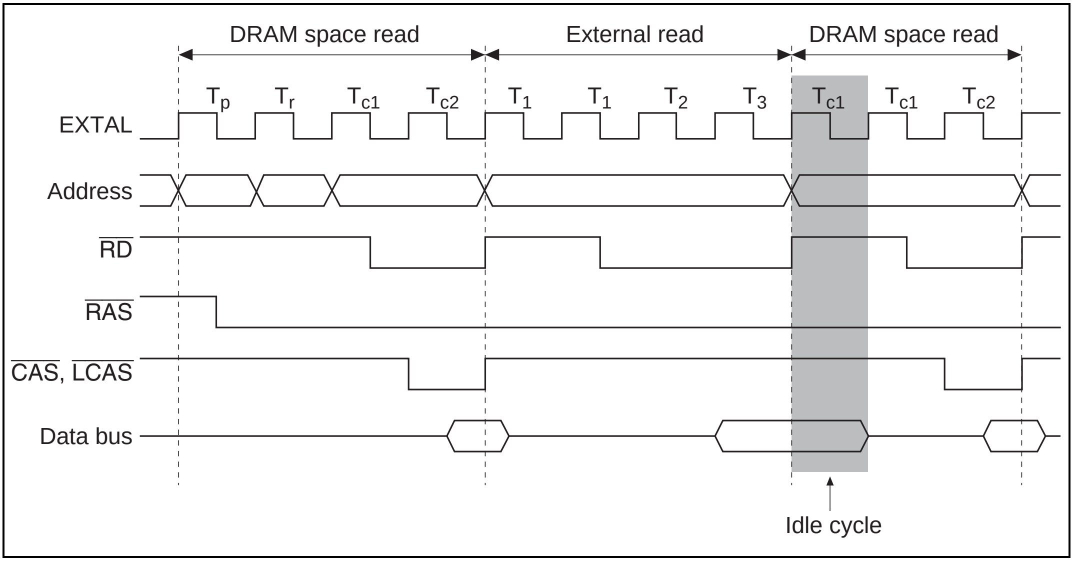


Figure 6.35 (a) Example of Idle Cycle Operation in RAS Down Mode (ICIS1 = 1)

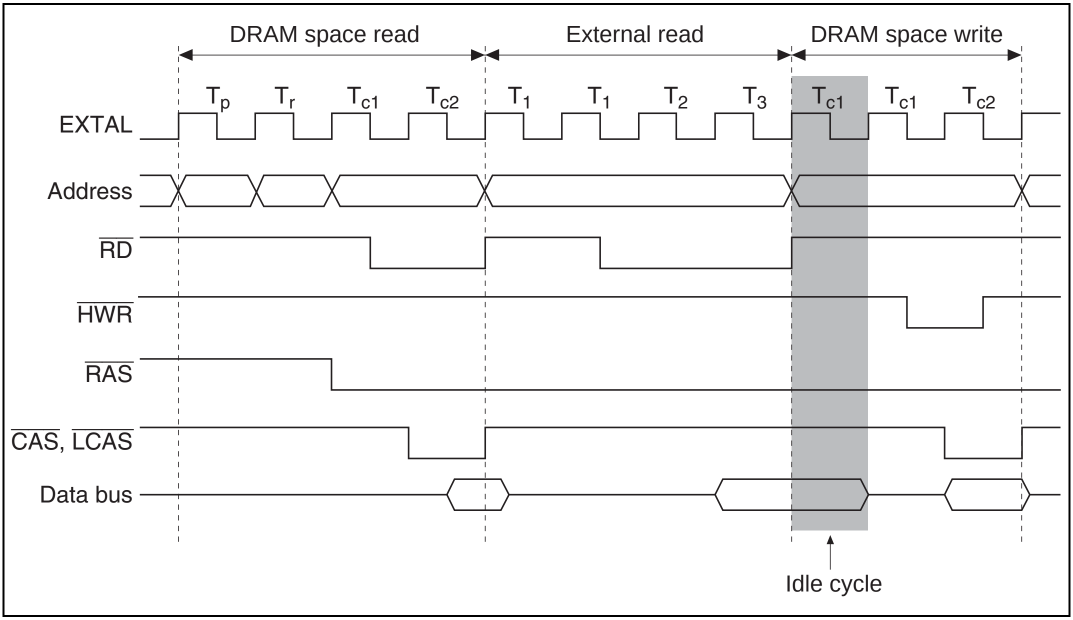


Figure 6.35 (b) Example of Idle Cycle Operation in RAS Down Mode (ICIS0 = 1)

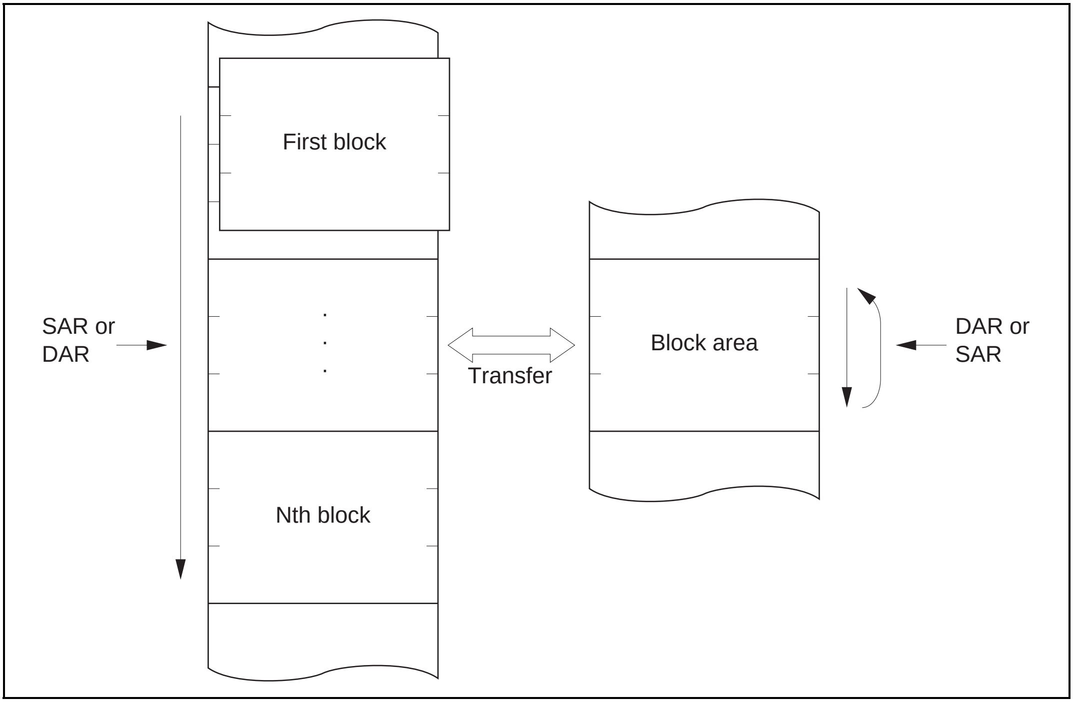


Figure 8.8 Memory Map in Block Transfer Mode

Pin	Selection Method and Pin Functions
P2$_1$/PO$_1$/TIOCB$_3$	The pin function is switched as shown below according to the combination of the TPU channel 3 setting (by bits MD3 to MD0 in TMDR3, bits IOB3 to IOB0 in TIOR3H, and bits CCLR2 to CCLR0 in TCR3), bit NDER1 in NDERL, and bit P21DDR.

TPU Channel 3 Setting	Table Below (1)	Table Below (2)		
P21DDR	—	0	1	1
NDER1	—	—	0	1
Pin function	TIOCB$_3$ output	P2$_1$ input	P2$_1$ output	PO$_1$ output
		TIOCB$_3$ input*		

Note: * TIOCB$_3$ input when MD3 to MD0 = B'0000, and IOB3 to IOB0 = B'10xx.

TPU Channel 3 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin **Selection Method and Pin Functions**

P3$_3$/RxD$_1$

The pin function is switched as shown below according to the combination of bit RE in the SCI1 SCR, and bit P33DDR.

RE	0		1
P33DDR	0	1	—
Pin function	P3$_3$ input pin	P3$_3$ output pin*	RxD$_1$ input pin

Note: * When P33ODR = 1, the pin becomes an NMOS open-drain output.

P3$_2$/RxD$_0$

The pin function is switched as shown below according to the combination of bit RE in the SCI0 SCR, and bit P32DDR.

RE	0		1
P32DDR	0	1	—
Pin function	P3$_2$ input pin	P3$_2$ output pin*	RxD$_0$ input pin

Note: * When P32ODR = 1, the pin becomes an NMOS open-drain output.

P3$_1$/TxD$_1$

The pin function is switched as shown below according to the combination of bit TE in the SCI1 SCR, and bit P31DDR.

TE	0		1
P31DDR	0	1	—
Pin function	P3$_1$ input pin	P3$_1$ output pin*	TxD$_1$ output pin

Note: * When P31ODR = 1, the pin becomes an NMOS open-drain output.

P3$_0$/TxD$_0$

The pin function is switched as shown below according to the combination of bit TE in the SCI0 SCR, and bit P30DDR.

TE	0		1
P30DDR	0	1	—
Pin function	P3$_0$ input pin	P3$_0$ output pin*	TxD$_0$ output pin

Note: * When P30ODR = 1, the pin becomes an NMOS open-drain output.

11.1.3 Pin Configuration

Table 11.1 summarizes the PPG pins.

Table 11.1 PPG Pins

Name	Symbol	I/O	Function
Pulse output 0	PO0	Output	Group 0 pulse output
Pulse output 1	PO1	Output	
Pulse output 2	PO2	Output	
Pulse output 3	PO3	Output	
Pulse output 4	PO4	Output	Group 1 pulse output
Pulse output 5	PO5	Output	
Pulse output 6	PO6	Output	
Pulse output 7	PO7	Output	
Pulse output 8	PO8	Output	Group 2 pulse output
Pulse output 9	PO9	Output	
Pulse output 10	PO10	Output	
Pulse output 11	PO11	Output	
Pulse output 12	PO12	Output	Group 3 pulse output
Pulse output 13	PO13	Output	
Pulse output 14	PO14	Output	
Pulse output 15	PO15	Output	

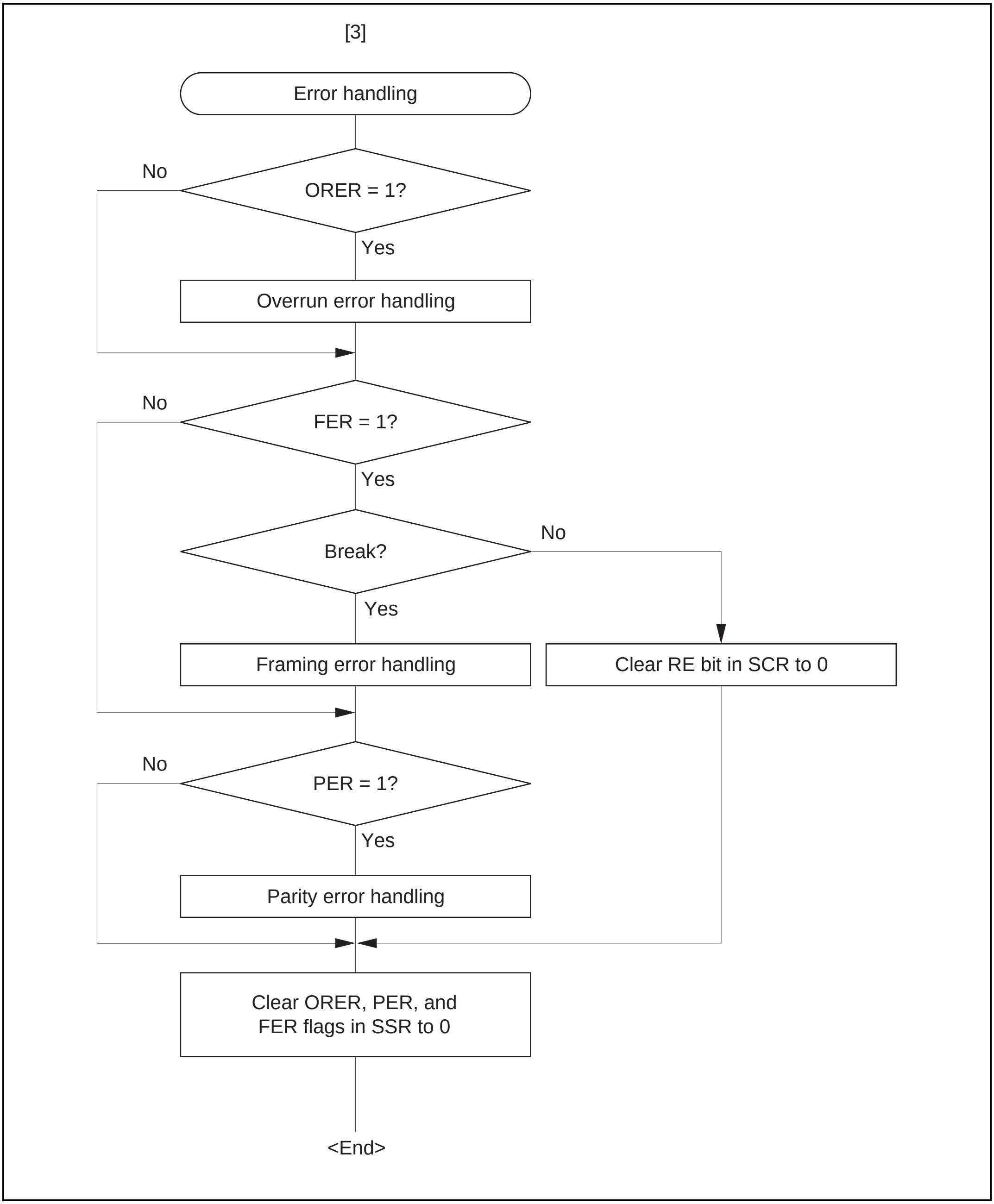
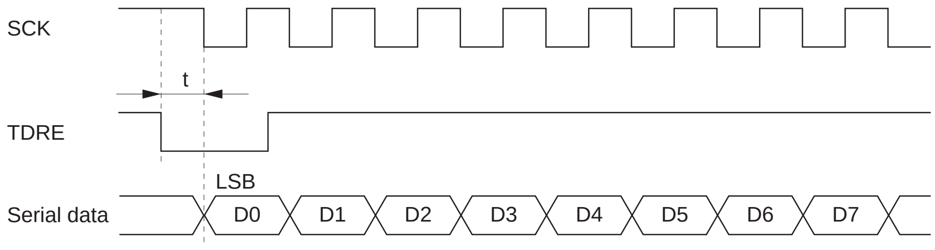


Figure 14.7 Sample Serial Reception Flowchart (cont)

Restrictions on Use of DMAC* or DTC

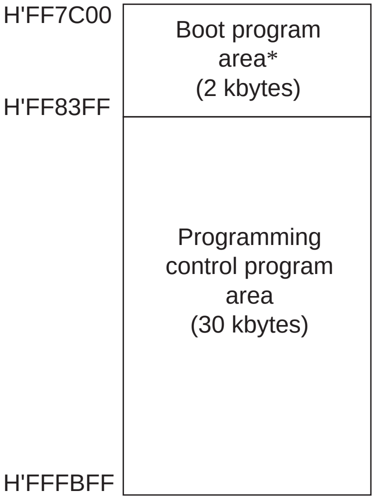
- When an external clock source is used as the serial clock, the transmit clock should not be input until at least 5 ϕ clock cycles after TDR is updated by the DMAC* or DTC. Misoperation may occur if the transmit clock is input within 4 ϕ clocks after TDR is updated. (Figure 14.22)
- When RDR is read by the DMAC* or DTC, be sure to set the activation source to the relevant SCI receive-data-full interrupt (RXI).

Note: * The DMAC is not supported in the H8S/2321.



Note: When operating on an external clock, set t > 4 clocks.

Figure 14.22 Example of Synchronous Transmission Using DTC



Note: * The boot program area cannot be used until a transition is made to the execution state for the programming control program transferred to RAM. Note that the boot program remains stored in this area after a branch is made to the programming control program.

Figure 19.12 RAM Areas in Boot Mode

Notes on Use of Boot Mode

- When the chip comes out of reset in boot mode, it measures the low-level period of the input at the SCI’s RxD1 pin. The reset should end with RxD1 high. After the reset ends, it takes approximately 100 states before the chip is ready to measure the low-level period of the RxD1 pin.

- In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.

- Interrupts cannot be used while the flash memory is being programmed or erased.

- The RxD1 and TxD1 pins should be pulled up on the board.

- Before branching to the programming control program (RAM area H'FF8400 to H'FFFBFF), the chip terminates transmit and receive operations by the on-chip SCI (channel 1) (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. The transmit data output pin, TxD1, goes to the high-level output state (P31DDR = 1, P31DR = 1).

19.20.2 Socket Adapters and Memory Map

In PROM mode, a socket adapter is connected to the chip as shown in figure 19.47. Figure 19.46 shows the on-chip ROM memory map and figure 19.47 shows the socket adapter pin assignments.

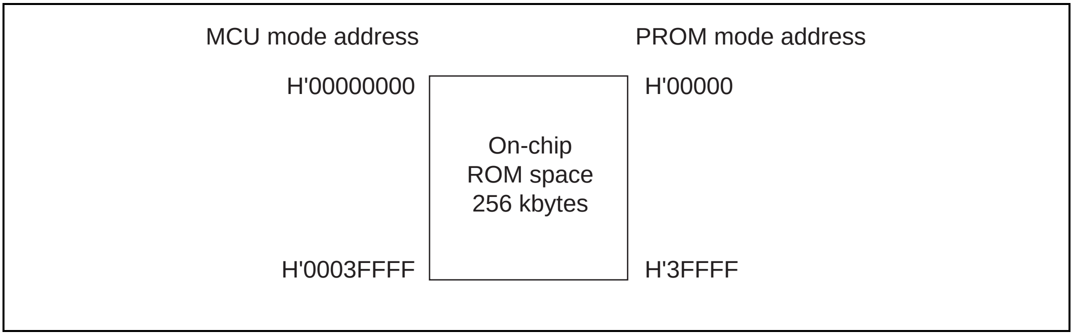


Figure 19.46 Memory Map in PROM Mode

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). Writing 1 to the FLSHE bit enables the flash memory control registers to be read and written to. Clearing FLSHE to 0 designates these registers as unselected (the register contents are retained).

Bit 3 FLSHE	Description
0	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB (Initial value)
1	Flash control registers are selected for addresses H'FFFFC8 to H'FFFFCB

Bits 2 to 0—Reserved: These bits cannot be modified and are always read as 0.

19.23.6 RAM Emulation Register (RAMER)

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value :	0	0	0	0	0	0	0	0
R/W :	—	—	—	—	R/W	R/W	R/W	R/W

RAMER specifies the area of flash memory to be overlapped with part of RAM when emulating real-time flash memory programming. RAMER is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode. RAMER settings should be made in user mode or user program mode.

Flash memory area divisions are shown in table 19.50. To ensure correct operation of the emulation function, the ROM for which RAM emulation is performed should not be accessed immediately after this register has been modified. Normal execution of an access immediately after register modification is not guaranteed.

Bits 7 to 4—Reserved: These bits cannot be modified and are always read as 0.

BCRH—Bus Control Register H H'FED4 Bus Controller

Bit :	7	6	5	4	3	2	1	0
	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMTS0
Initial value :	1	1	0	1	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RAM Type Select

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	0	Normal space			
		1	Normal space			DRAM space
	1	0	Normal space		DRAM space	
		1	DRAM space			
1	—	—	—			

Notes: 1. When areas selected in DRAM space are all 8-bit space, the PF2 pin can be used as an I/O port, $\overline{\text{BREQO}}$, or $\overline{\text{WAIT}}$. When PF2 is used as the $\overline{\text{WAIT}}$ pin in the H8S/2323, normal space other than DRAM space should be designated as 16-bit-bus space. RAS down mode cannot be used when this setting is made. Sample settings are shown below.

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	0	Normal space			
		1	Normal space (16-bit bus)			DRAM space (8-bit bus)
	1	0	Normal space (16-bit bus)		DRAM space (8-bit bus)	
		1	DRAM space (8-bit bus)			

2. In the H8S/2321 these bits are reserved and should only be written with 0.

Burst Cycle Select 0

0	Max. 4 words in burst access
1	Max. 8 words in burst access

Burst Cycle Select 1

0	Burst cycle comprises 1 state
1	Burst cycle comprises 2 states

Area 0 Burst ROM Enable

0	Basic bus interface
1	Burst ROM interface

Idle Cycle Insert 0

0	Idle cycle not inserted in case of successive external read and external write cycles
1	Idle cycle inserted in case of successive external read and external write cycles

Idle Cycle Insert 1

0	Idle cycle not inserted in case of successive external read cycles in different areas
1	Idle cycle inserted in case of successive external read cycles in different areas

NDRH—Next Data Register H H'FF4C (FF4E) PPG

(1) When pulse output group output triggers are the same

(a) Address: H'FF4C

Bit :	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores the next data for pulse output groups 3 and 2

(b) Address: H'FF4E

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value :	1	1	1	1	1	1	1	1
Read/Write :	—	—	—	—	—	—	—	—

(2) When pulse output group output triggers are different

(a) Address: H'FF4C

Bit :	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	—	—	—	—
Initial value :	0	0	0	0	1	1	1	1
Read/Write :	R/W	R/W	R/W	R/W	—	—	—	—

Stores the next data for pulse output group 3

(b) Address: H'FF4E

Bit :	7	6	5	4	3	2	1	0
	—	—	—	—	NDR11	NDR10	NDR9	NDR8
Initial value :	1	1	1	1	0	0	0	0
Read/Write :	—	—	—	—	R/W	R/W	R/W	R/W

Stores the next data for pulse output group 2