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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2329bvf25v

Section 1 Overview

1.1 Overview

The H8S/2329 Group and H8S/2328 Group are series of microcomputers (MCUs: microcomputer units), built around the H8S/2000 CPU, employing Renesas' proprietary architecture, and equipped with supporting functions on-chip.

The H8S/2000 CPU has an internal 32-bit architecture, is provided with sixteen 16-bit general registers and a concise, optimized instruction set designed for high-speed operation, and can address a 16-Mbyte linear address space. The instruction set is upward-compatible with H8/300 and H8/300H CPU instructions at the object-code level, facilitating migration from the H8/300, H8/300L, or H8/300H Series.

On-chip supporting functions required for system configuration include DMA controller (DMAC)*1 and data transfer controller (DTC) bus masters, ROM and RAM, a 16-bit timer-pulse unit (TPU), programmable pulse generator (PPG), 8-bit timer, watchdog timer (WDT), serial communication interface (SCI), A/D converter, D/A converter, and I/O ports.

A high-functionality bus controller is also provided, enabling fast and easy connection of DRAM and other kinds of memory.

Single-power-supply flash memory (F-ZTAT™*2) and mask ROM versions are available, providing a quick and flexible response to conditions from ramp-up through full-scale volume production, even for applications with frequently changing specifications. ROM is connected to the CPU via a 16-bit data bus, enabling both byte and word data to be accessed in one state. Instruction fetching is thus speeded up, and processing speed increased.

The features of the H8S/2329 Group is shown in table 1.1.

Notes: 1. The DMAC is not supported in the H8S/2321.
2. F-ZTAT is a trademark of Renesas Technology Corp.

2.4 Register Configuration

2.4.1 Overview

The CPU has the internal registers shown in figure 2.4. There are two types of registers: general registers and control registers.

General Registers (Rn) and Extended Registers (En)

	15	07	07	0
ER0	E0	R0H	R0L	
ER1	E1	R1H	R1L	
ER2	E2	R2H	R2L	
ER3	E3	R3H	R3L	
ER4	E4	R4H	R4L	
ER5	E5	R5H	R5L	
ER6	E6	R6H	R6L	
ER7 (SP)	E7	R7H	R7L	

Control Registers (CR)

23	0
PC	

	7	6	5	4	3	2	1	0
EXR	T	—	—	—	—	I2	I1	I0

	7	6	5	4	3	2	1	0
CCR	I	UI	H	U	N	Z	V	C

Legend:

SP:	Stack pointer	H:	Half-carry flag
PC:	Program counter	U:	User bit
EXR:	Extended control register	N:	Negative flag
T:	Trace bit	Z:	Zero flag
I2 to I0:	Interrupt mask bits	V:	Overflow flag
CCR:	Condition-code register	C:	Carry flag
I:	Interrupt mask bit		
UI:	User bit or interrupt mask bit*		

Note: * In the H8S/2329 Group and H8S/2328 Group, this bit cannot be used as an interrupt mask.

Figure 2.4 CPU Registers

Type	Instruction	Size*1	Function		
Branch instructions	Bcc	—	Branches to a specified address if a specified condition is true. The branching conditions are listed below.		
			Mnemonic	**Description**	**Condition**
			BRA(BT)	Always (true)	Always
			BRN(BF)	Never (false)	Never
			BHI	High	$C \vee Z = 0$
			BLS	Low or same	$C \vee Z = 1$
			BCC(BHS)	Carry clear (high or same)	$C = 0$
			BCS(BLO)	Carry set (low)	$C = 1$
			BNE	Not equal	$Z = 0$
			BEQ	Equal	$Z = 1$
			BVC	Overflow clear	$V = 0$
			BVS	Overflow set	$V = 1$
			BPL	Plus	$N = 0$
			BMI	Minus	$N = 1$
			BGE	Greater or equal	$N \oplus V = 0$
			BLT	Less than	$N \oplus V = 1$
			BGT	Greater than	$Z \vee (N \oplus V) = 0$
			BLE	Less or equal	$Z \vee (N \oplus V) = 1$
	JMP	—	Branches unconditionally to a specified address.		
	BSR	—	Branches to a subroutine at a specified address.		
	JSR	—	Branches to a subroutine at a specified address.		
	RTS	—	Returns from a subroutine.		

If an odd address is specified in word or longword memory access, or as a branch address, the least significant bit is regarded as 0, causing data to be accessed or instruction code to be fetched at the address preceding the specified address. (For further information, see section 2.5.2, Memory Data Formats.)

2.7.2 Effective Address Calculation

Table 2.6 indicates how effective addresses are calculated in each addressing mode.

As a refresh* and an external access by an internal bus master can be executed simultaneously, there is no relative order of priority for these two operations.

Note: * The DMAC and DRAM interface are not supported in the H8S/2321.

6.11.3 Bus Transfer Timing

Even if a bus request is received from a bus master with a higher priority than that of the bus master that has acquired the bus and is currently operating, the bus is not necessarily transferred immediately. There are specific times at which each bus master can relinquish the bus.

CPU: The CPU is the lowest-priority bus master, and if a bus request is received from the DTC or DMAC*, the bus arbiter transfers the bus to the bus master that issued the request. The timing for transfer of the bus is as follows:

- The bus is transferred at a break between bus cycles. However, if a bus cycle is executed in discrete operations, as in the case of a longword-size access, the bus is not transferred between the operations. See appendix A.5, Bus States during Instruction Execution, for timings at which the bus is not transferred.
- If the CPU is in sleep mode, it transfers the bus immediately.

DTC: The DTC sends the bus arbiter a request for the bus when an activation request is generated.

The DTC can release the bus after a vector read, a register information read (3 states), a single data transfer, or a register information write (3 states). It does not release the bus during a register information read (3 states), a single data transfer, or a register information write (3 states).

DMAC*: The DMAC sends the bus arbiter a request for the bus when an activation request is generated.

In the case of an external request in short address mode or normal mode, and in cycle steal mode, the DMAC releases the bus after a single transfer.

In block transfer mode, it releases the bus after transfer of one block, and in burst mode, after completion of a transfer.

Note: * The DMAC is not supported in the H8S/2321.

Bit 7—DTC Chain Transfer Enable (CHNE): Specifies chain transfer. With chain transfer, a number of data transfers can be performed consecutively in response to a single transfer request.

In data transfer with CHNE set to 1, determination of the end of the specified number of transfers, clearing of the interrupt source flag, and clearing of DTCER are not performed.

When CHNE is set to 1, the chain transfer condition can be selected with the CHNS bit.

Bit 7 CHNE	Description
0	End of DTC data transfer (activation waiting state)
1	DTC chain transfer (new register information is read, then data is transferred)

Bit 6—DTC Interrupt Select (DISEL): Specifies whether interrupt requests to the CPU are disabled or enabled after a data transfer.

Bit 6 DISEL	Description
0	After a data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0 (the DTC clears the interrupt source flag of the activating interrupt to 0)
1	After a data transfer ends, the CPU interrupt is enabled (the DTC does not clear the interrupt source flag of the activating interrupt to 0)

Bit 5—DTC Chain Transfer Select (CHNS): Specifies the chain transfer condition when CHNE is 1.

Bit 7 CHNE	Bit 5 CHNS	Description
0	–	No chain transfer (DTC data transfer end, activation waiting state entered)
1	0	DTC chain transfer
1	1	Chain transfer only when transfer counter = 0

Bits 4 to 0—Reserved: These bits have no effect on DTC operation in the chip and should always be written with 0.

Section 9 I/O Ports

9.1 Overview

The chip has 12 I/O ports (ports 1, 2, 3, 5, 6, and A to G), and one input-only port (port 4).

Table 9.1 summarizes the port functions. The pins of each port also have other functions.

Each port includes a data direction register (DDR) that controls input/output (not provided for the input-only port), a data register (DR) that stores output data, and a port register (PORT) used to read the pin states.

Ports A to E have a built-in MOS pull-up function, and in addition to DR and DDR, have a MOS input pull-up control register (PCR) to control the on/off state of MOS input pull-up.

Port 3 and port A include an open drain control register (ODR) that controls the on/off state of the output buffer PMOS.

Ports 1 and A to F can drive a single TTL load and 50 pF capacitive load, and ports 2, 3, 5, 6, and G can drive a single TTL load and 30 pF capacitive load.

Ports 1, 2, and 5 (only when used for IRQ input), and pins 6_4 to 6_7 and A_4 to A_7, are Schmitt-triggered inputs.

	φ = 9.8304 MHz			φ = 10 MHz			φ = 12 MHz			φ = 12.288 MHz		
Bit Rate (bits/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

	φ = 14 MHz			φ = 14.7456 MHz			φ = 16 MHz			φ = 17.2032 MHz		
Bit Rate (bits/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	248	–0.17	3	64	0.70	3	70	0.03	3	75	0.48
150	2	181	0.16	2	191	0.00	2	207	0.16	2	223	0.00
300	2	90	0.16	2	95	0.00	2	103	0.16	2	111	0.00
600	1	181	0.16	1	191	0.00	1	207	0.16	1	223	0.00
1200	1	90	0.16	1	95	0.00	1	103	0.16	1	111	0.00
2400	0	181	0.16	0	191	0.00	0	207	0.16	0	223	0.00
4800	0	90	0.16	0	95	0.00	0	103	0.16	0	111	0.00
9600	0	45	–0.93	0	47	0.00	0	51	0.16	0	55	0.00
19200	0	22	–0.93	0	23	0.00	0	25	0.16	0	27	0.00
31250	0	13	0.00	0	14	–1.70	0	15	0.00	0	16	1.20
38400	0	10	—	0	11	0.00	0	12	0.16	0	13	0.00

14.2.10 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR is a 16-bit readable/writable register that performs module stop mode control.

When the corresponding bit of bits MSTP7 to MSTP5 is set to 1, SCI operation stops at the end of the bus cycle and a transition is made to module stop mode. Registers cannot be read or written to in module stop mode. For details, see section 21.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Module Stop (MSTP7): Specifies the SCI channel 2 module stop mode.

Bit 7 MSTP7	Description	
0	SCI channel 2 module stop mode cleared	
1	SCI channel 2 module stop mode set	(Initial value)

Bit 6—Module Stop (MSTP6): Specifies the SCI channel 1 module stop mode.

Bit 6 MSTP6	Description	
0	SCI channel 1 module stop mode cleared	
1	SCI channel 1 module stop mode set	(Initial value)

Bit 5—Module Stop (MSTP5): Specifies the SCI channel 0 module stop mode.

Bit 5 MSTP5	Description	
0	SCI channel 0 module stop mode cleared	
1	SCI channel 0 module stop mode set	(Initial value)

Section 15 Smart Card Interface

15.1 Overview

The SCI supports an IC card (smart card) interface conforming to ISO/IEC 7816-3 (identification card) as a serial communication interface extension function.

Switching between the normal serial communication interface and the smart card interface is carried out by means of a register setting.

15.1.1 Features

Features of the smart card interface supported by the chip is as follows.

- Asynchronous mode
  - Data length: 8 bits
  - Parity bit generation and checking
  - Transmission of error signal (parity error) in receive mode
  - Error signal detection and automatic data retransmission in transmit mode
  - Direct convention and inverse convention both supported
- Built-in baud rate generator allows any bit rate to be selected
- Three interrupt sources
  - Three interrupt sources (transmit-data-empty, receive-data-full, and transmit/receive-error) that can issue requests independently
  - The transmit-data-empty and receive-data-full interrupts can activate the DMA controller (DMAC)* or data transfer controller (DTC) to execute data transfer

Note: * The DMAC is not supported in the H8S/2321.

- Retransfer operation when SCI is in transmit mode

  Figure 15.12 illustrates the retransfer operation when the SCI is in transmit mode.

[6] If an error signal is sent back from the receiving end after transmission of one frame is completed, the ERS bit in SSR is set to 1. If the RIE bit in SCR is enabled at this time, an ERI interrupt request is generated. The ERS bit in SSR should be kept cleared to 0 until the next parity bit is sampled.

[7] The TEND bit in SSR is not set for a frame for which an error signal indicating an abnormality is received.

[8] If an error signal is not sent back from the receiving end, the ERS bit in SSR is not set.

[9] If an error signal is not sent back from the receiving end, transmission of one frame, including a retransfer, is judged to have been completed, and the TEND bit in SSR is set to 1. If the TIE bit in SCR is enabled at this time, a TXI interrupt request is generated.

If data transfer by the DMAC* or DTC by means of the TXI source is enabled, the next data can be written to TDR automatically. When data is written to TDR by the DMAC* or DTC, the TDRE bit is automatically cleared to 0.

Note: * The DMAC is not supported in the H8S/2321.

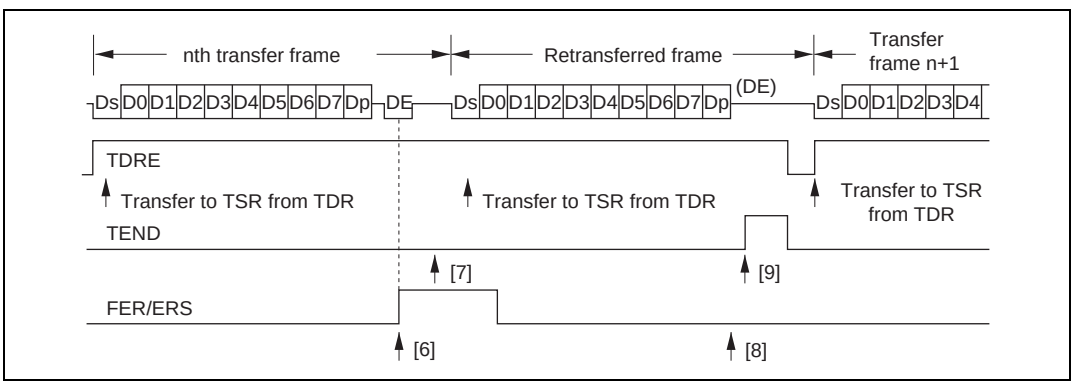

Figure 15.12 Retransfer Operation in SCI Transmit Mode

16.4 Operation

The A/D converter operates by successive approximations with 10-bit resolution. It has two operating modes: single mode and scan mode.

16.4.1 Single Mode (SCAN = 0)

Single mode is selected when A/D conversion is to be performed on a single channel only. A/D conversion is started when the ADST bit is set to 1 by software or by external trigger input. The ADST bit remains set to 1 during A/D conversion, and is automatically cleared to 0 when conversion ends.

On completion of conversion, the ADF flag is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated. The ADF flag is cleared by writing 0 to it after reading ADCSR.

When the operating mode or analog input channel must be changed during analog conversion, to prevent incorrect operation, first clear the ADST bit to 0 in ADCSR to halt A/D conversion. After making the necessary changes, set the ADST bit to 1 to start A/D conversion again. The ADST bit can be set at the same time as the operating mode or input channel is changed.

Typical operations when channel 1 (AN1) is selected in single mode are described next. Figure 16.3 shows a timing diagram for this example.

[1] Single mode is selected (SCAN = 0), input channel AN1 is selected (CH2 = 0, CH1 = 0, CH0 = 1), the A/D interrupt is enabled (ADIE = 1), and A/D conversion is started (ADST = 1).

[2] When A/D conversion is completed, the result is transferred to ADDRB. At the same time the ADF flag is set to 1, the ADST bit is cleared to 0, and the A/D converter becomes idle.

[3] Since ADF = 1 and ADIE = 1, an ADI interrupt is requested.

[4] The A/D interrupt handling routine starts.

[5] The routine reads ADCSR, then writes 0 to the ADF flag.

[6] The routine reads and processes the conversion result (ADDRB).

[7] Execution of the A/D interrupt handling routine ends. After that, if the ADST bit is set to 1, A/D conversion starts again and steps [2] to [7] are repeated.

Writing Overlap RAM Data in User Program Mode: When overlap RAM data is confirmed, the RAMS bit is cleared, RAM overlap is released, and writes should actually be performed to the flash memory.

When the programming control program is transferred to RAM, ensure that the transfer destination and the overlap RAM do not overlap, as this will cause data in the overlap RAM to be rewritten.

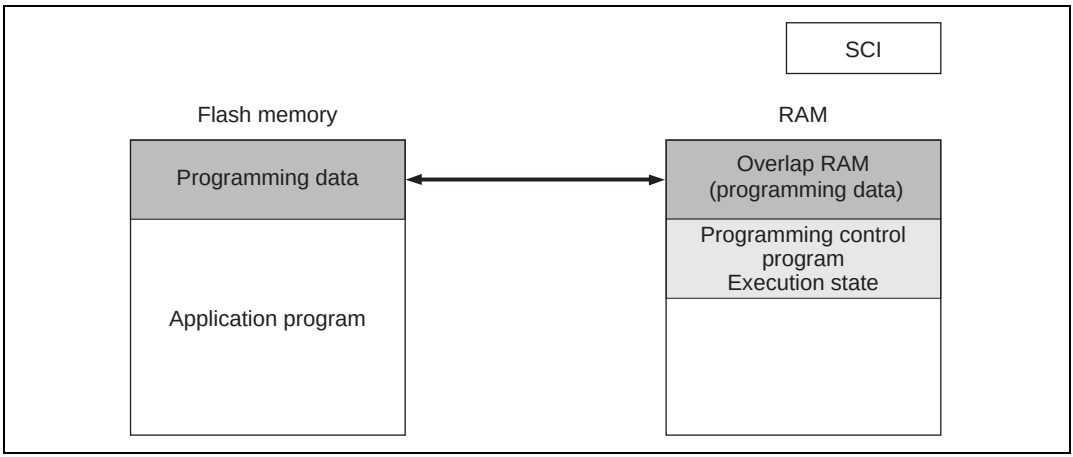

Figure 19.64 Writing Overlap RAM Data in User Program Mode

19.22.6 Differences between Boot Mode and User Program Mode

Table 19.46 Differnces between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Entire memory erase	Yes	Yes
Block erase	No	Yes
Programming control program*	Program/program-verify	Erase/erase-verify/program/ program-verify/emulation

Note: * To be provided by the user, in accordance with the recommended algorithm.

19.29.2 Socket Adapters and Memory Map

In PROM mode, a socket adapter is connected to the chip as shown in figure 19.77. Figure 19.76 shows the on-chip ROM memory map and figure 19.77 shows the socket adapter pin assignments.

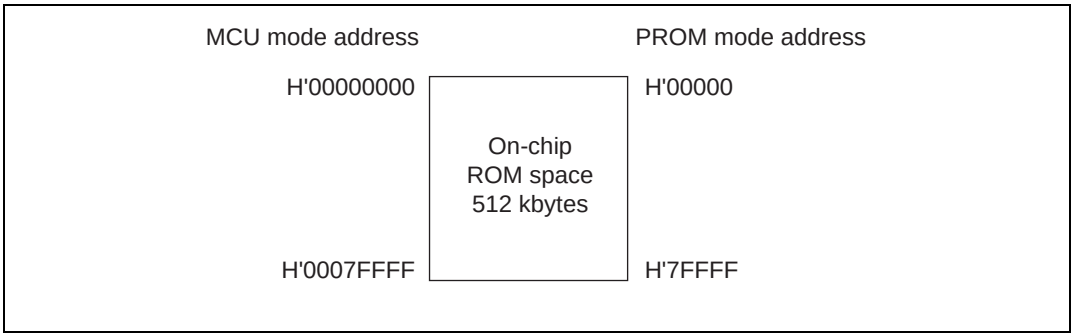

Figure 19.76 Memory Map in PROM Mode

22.1.2 DC Characteristics

Table 22.2 DC Characteristics (H8S/2328, H8S/2327, H8S/2323)

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $P6_4$ to $P6_7$, PA_4 to PA_7, Port 5 (when using $\overline{IRQ}$)	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Ports 3, 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		2.2	—	V_{CC} + 0.3	V	
	Port 4		2.2	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, Ports 3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 μA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	| I_{in} |	—	—	10.0	μA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2 to MD_0		—	—	1.0	μA	
	Port 4		—	—	1.0	μA	V_{in} = 0.5 V to AV_{CC} – 0.5 V

Mnemonic	Operand Size	Addressing Mode/ Instruction Length (Bytes)								Operation	Condition Code						No. of States*1
		#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa		I	H	N	Z	V	C	Advanced
JMP	JMP @ERn	—		2						PC←ERn	—	—	—	—	—	—	2
	JMP @aa:24	—					4			PC←aa:24	—	—	—	—	—	—	3
	JMP @@aa:8	—							2	PC←@aa:8	—	—	—	—	—	—	5
BSR	BSR d:8	—						2		PC→@-SP,PC←PC+d:8	—	—	—	—	—	—	4
	BSR d:16	—						4		PC→@-SP,PC←PC+d:16	—	—	—	—	—	—	5
JSR	JSR @ERn	—		2						PC→@-SP,PC←ERn	—	—	—	—	—	—	4
	JSR @aa:24	—					4			PC→@-SP,PC←aa:24	—	—	—	—	—	—	5
	JSR @@aa:8	—							2	PC→@-SP,PC←@aa:8	—	—	—	—	—	—	6
RTS	RTS	—							2	PC←@SP+	—	—	—	—	—	—	5

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte		10th byte	
EXTS	EXTS.W Rd	W	1	7	D	rd														
	EXTS.L ERd	L	1	7	F	0 erd														
EXTU	EXTU.W Rd	W	1	7	5	rd														
	EXTU.L ERd	L	1	7	7	0 erd														
INC	INC.B Rd	B	0	A	0	rd														
	INC.W #1,Rd	W	0	B	5	rd														
	INC.W #2,Rd	W	0	B	D	rd														
	INC.L #1,ERd	L	0	B	7	0 erd														
	INC.L #2,ERd	L	0	B	F	0 erd														
JMP	JMP @ERn	—	5	9	0 ern	0														
	JMP @aa:24	—	5	A	abs															
	JMP @@aa:8	—	5	B	abs															
JSR	JSR @ERn	—	5	D	0 ern	0														
	JSR @aa:24	—	5	E	abs															
	JSR @@aa:8	—	5	F	abs															
LDC	LDC #xx:8,CCR	B	0	7	IMM															
	LDC #xx:8,EXR	B	0	1	4	1	0	7	IMM											
	LDC Rs,CCR	B	0	3	0	rs														
	LDC Rs,EXR	B	0	3	1	rs														
	LDC @ERs,CCR	W	0	1	4	0	6	9	0 ers	0										
	LDC @ERs,EXR	W	0	1	4	1	6	9	0 ers	0										
	LDC @(d:16,ERs),CCR	W	0	1	4	0	6	F	0 ers	0	disp									
	LDC @(d:16,ERs),EXR	W	0	1	4	1	6	F	0 ers	0	disp									
	LDC @(d:32,ERs),CCR	W	0	1	4	0	7	8	0 ers	0	6	B	2	0	disp					
	LDC @(d:32,ERs),EXR	W	0	1	4	1	7	8	0 ers	0	6	B	2	0	disp					
	LDC @ERs+,CCR	W	0	1	4	0	6	D	0 ers	0										
	LDC @ERs+,EXR	W	0	1	4	1	6	D	0 ers	0										
	LDC @aa:16,CCR	W	0	1	4	0	6	B	0	0	abs									
	LDC @aa:16,EXR	W	0	1	4	1	6	B	0	0	abs									

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FEC4	IPRA	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	Interrupt controller	8 bits
H'FEC5	IPRB	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC6	IPRC	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC7	IPRD	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FEC8	IPRE	—	IPR6	IPR5	I PR4	—	IPR2	IPR1	IPR0		
H'FEC9	IPRF	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECA	IPRG	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECB	IPRH	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECC	IPRI	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECD	IPRJ	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FECE	IPRK	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0		
H'FED0	ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	Bus controller	8 bits
H'FED1	ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0		
H'FED2	WCRH	W71	W70	W61	W60	W51	W50	W41	W40		
H'FED3	WCRL	W31	W30	W21	W20	W11	W10	W01	W00		
H'FED4	BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2*2	RMTS1*2	RMTS0*2		
H'FED5	BCRL	BRLE	BREQOE	EAE	—	DDS*2	—	WDBE*2	WAITE		
H'FED6	MCR*3	TPC	BE	RCDM	—	MXC1	MXC0	RLW1	RLW0		
H'FED7	DRAMCR *3	RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0		
H'FED8	RTCNT*3										
H'FED9	RTCOR										
H'FEDB	RAMER*4	—	—	—	—	RAMS	RAM2	RAM1	RAM0	Flash memory	8 bits
H'FEE0	MAR0AH	—	—	—	—	—	—	—	—	DMAC*5	16 bits
H'FEE1											
H'FEE2	MAR0AL										
H'FEE3											
H'FEE4	IOAR0A										
H'FEE5											
H'FEE6	ETCR0A										
H'FEE7											
H'FEE8	MAR0BH	—	—	—	—	—	—	—	—		
H'FEE9											
H'FEEA	MAR0BL										
H'FEEB											
H'FEEC	IOAR0B										
H'FEED											
H'FEEE	ETCR0B										
H'FEEF											

Module	Register	Abbreviation	R/W	Initial Value	Address[*1]
ADC	A/D data register AH	ADDRAH	R	H'00	H'FF90
	A/D data register AL	ADDRAL	R	H'00	H'FF91
	A/D data register BH	ADDRBH	R	H'00	H'FF92
	A/D data register BL	ADDRBL	R	H'00	H'FF93
	A/D data register CH	ADDRCH	R	H'00	H'FF94
	A/D data register CL	ADDRCL	R	H'00	H'FF95
	A/D data register DH	ADDRDH	R	H'00	H'FF96
	A/D data register DL	ADDRDL	R	H'00	H'FF97
	A/D control/status register	ADCSR	R/(W)[*12]	H'00	H'FF98
	A/D control register	ADCR	R/W	H'3F	H'FF99
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
DAC	D/A data register 0	DADR0	R/W	H'00	H'FFA4
	D/A data register 1	DADR1	R/W	H'00	H'FFA5
	D/A control register 01	DACR01	R/W	H'1F	H'FFA6
	Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C
On-chip RAM	System control register	SYSCR	R/W	H'01	H'FF39
Flash memory	Flash memory control register 1	FLMCR1[*17]	R/W[*14]	H'00/H'80[*15]	H'FFC8[*13]
	Flash memory control register 2	FLMCR2[*17]	R/W[*14]	H'00	H'FFC9[*13]
	Erase block register 1	EBR1[*17]	R/W[*14]	H'00[*16]	H'FFCA[*13]
	Erase block register 2	EBR2[*17]	R/W[*14]	H'00[*16]	H'FFCB[*13]
	RAM emulation register	RAMER[*22]	R/W	H'00	H'FEDB
	System control register 2	SYSCR2[*18]	R/W	H'00	H'FF42
Clock pulse generator	System clock control register	SCKCR	R/W	H'00	H'FF3A
Power-down mode	Standby control register	SBYCR	R/W	H'08	H'FF38
	System clock control register	SCKCR	R/W	H'00	H'FF3A
	Module stop control register H	MSTPCRH	R/W	H'3F	H'FF3C
	Module stop control register L	MSTPCRL	R/W	H'FF	H'FF3D

C.8 Port B

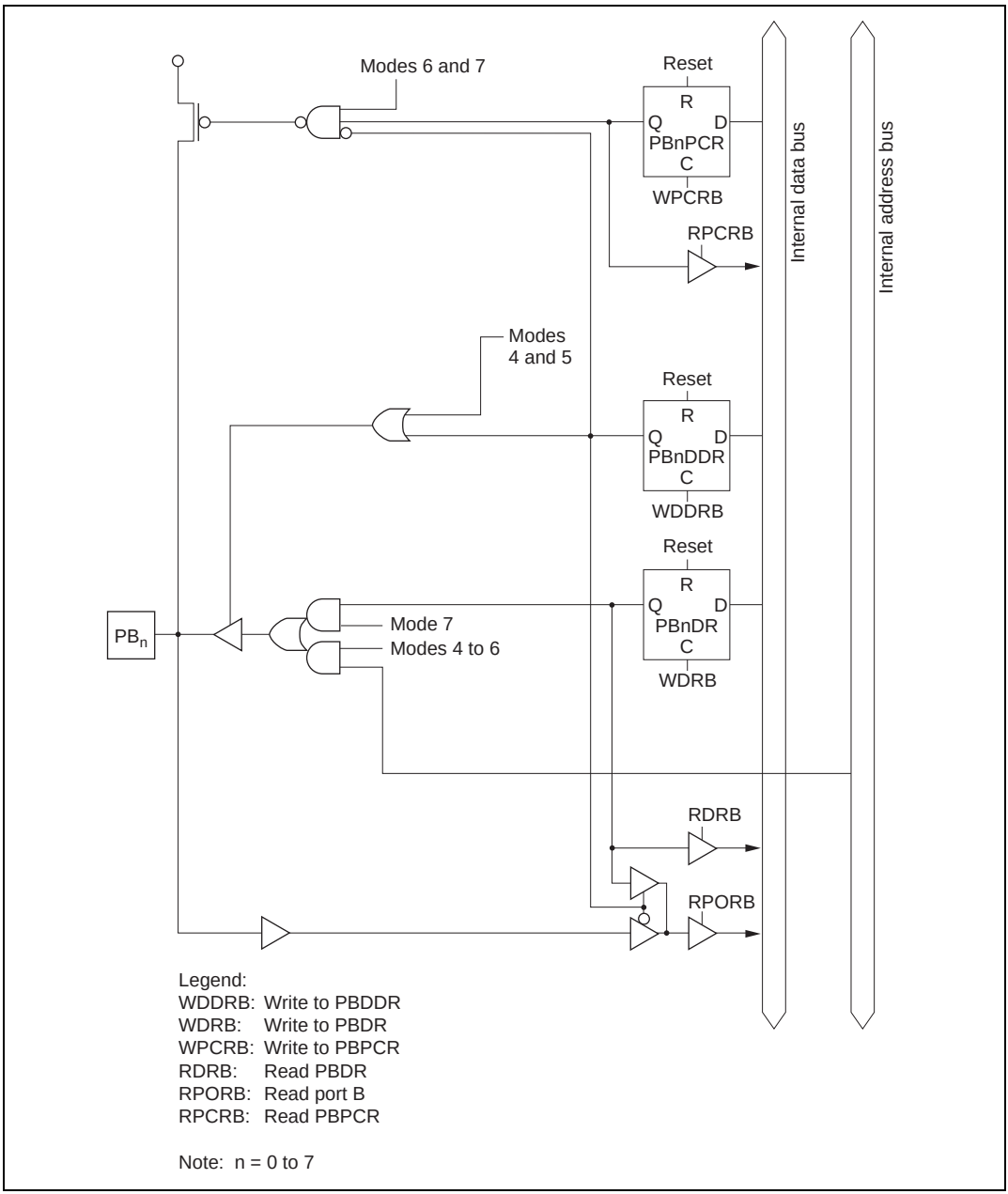

Figure C.8 Port B Block Diagram (Pins PB_0 to PB_7)