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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2329bvf25wv

2.6 Instruction Set

2.6.1 Overview

The H8S/2000 CPU has 65 types of instructions. The instructions are classified by function in table 2.1.

Table 2.1 Instruction Classification

Function	Instructions	Size	Types
Data transfer	MOV	BWL	5
	POP*1, PUSH*1	WL	
	LDM, STM	L	
	MOVFPE, MOVTPE*3	B	
Arithmetic operations	ADD, SUB, CMP, NEG	BWL	19
	ADDX, SUBX, DAA, DAS	B	
	INC, DEC	BWL	
	ADDS, SUBS	L	
	MULXU, DIVXU, MULXS, DIVXS	BW	
	EXTU, EXTS	WL	
	TAS*4	B	
Logic operations	AND, OR, XOR, NOT	BWL	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	BWL	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BLD, BILD, BST, BIST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR	B	14
Branch	Bcc*2, JMP, BSR, JSR, RTS	—	5
System control	TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	—	9
Block data transfer	EEPMOV	—	1
		Total:	65

Legend:
B: Byte
W: Word
L: Longword

Notes: 1. POP.W Rn and PUSH.W Rn are identical to MOV.W @SP+, Rn and MOV.W Rn, @-SP. POP.L ERn and PUSH.L ERn are identical to MOV.L @SP+, ERn and MOV.L ERn, @-SP.
2. Bcc is the general name for conditional branch instructions.
3. Cannot be used in the H8S/2329 Group and H8S/2328 Group.
4. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.

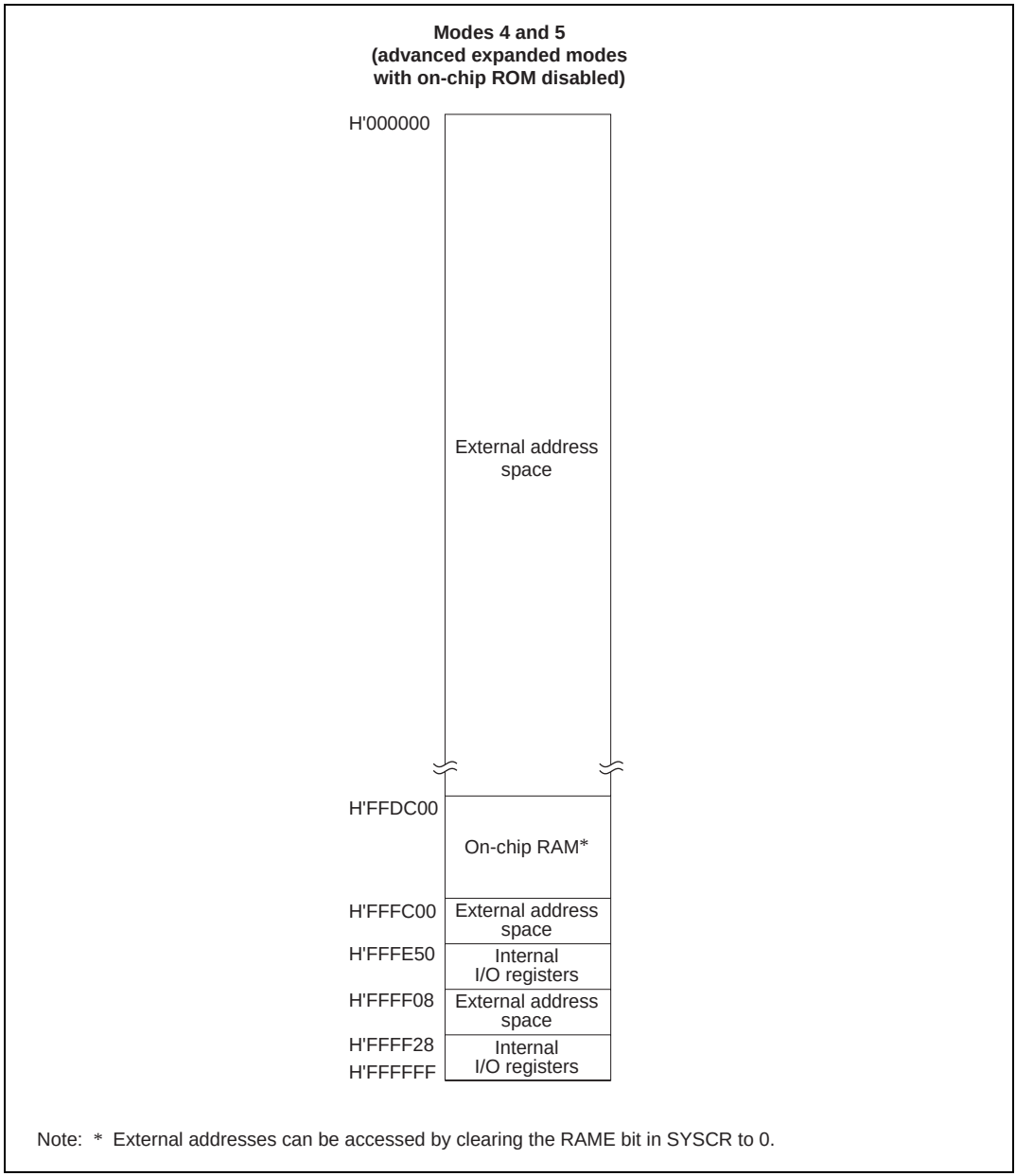

Figure 3.7 H8S/2322R Memory Map in Each Operating Mode

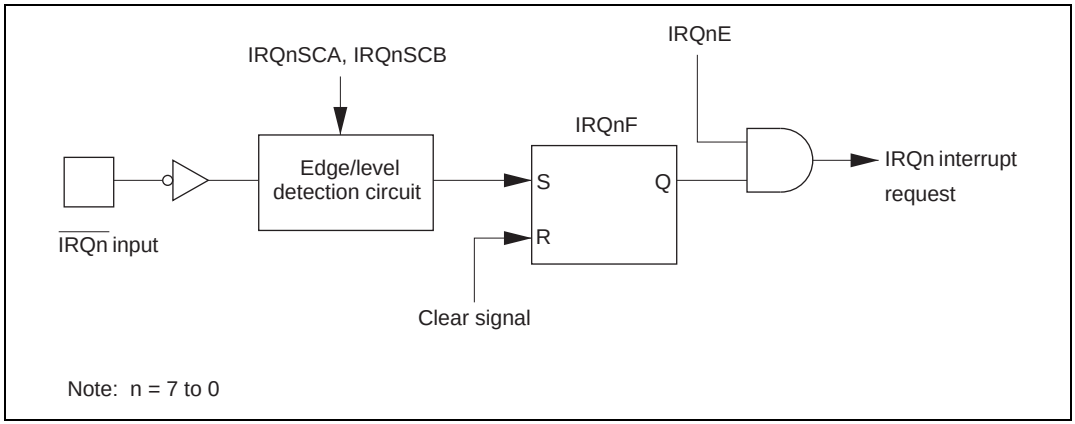

Figure 5.2 Block Diagram of Interrupts IRQ7 to IRQ0

Figure 5.3 shows the timing of setting IRQnF.

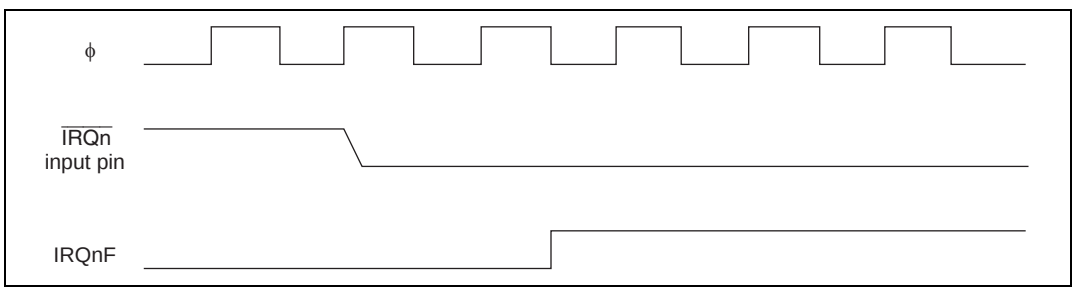

Figure 5.3 Timing of Setting IRQnF

The vector numbers for IRQ7 to IRQ0 interrupt exception handling are 23 to 16.

Detection of IRQ7 to IRQ0 interrupts does not depend on whether the relevant pin has been set for input or output. Therefore, when a pin is used as an external interrupt input pin, do not clear the corresponding DDR bit to 0 and use the pin as an I/O pin for another function. The pins that can be used for IRQ4 to IRQ7 interrupt input can be switched by means of the IRQPAS bit in SYSCR.

5.4.3 Interrupt Control Mode 2

Eight-level masking is implemented for IRQ interrupts and on-chip supporting module interrupts by comparing the interrupt mask level set by bits I2 to I0 of EXR in the CPU with IPR.

Figure 5.6 shows a flowchart of the interrupt acceptance operation in this case.

[1] If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.

[2] When interrupt requests are sent to the interrupt controller, the interrupt with the highest priority according to the interrupt priority levels set in IPR is selected, and lower-priority interrupt requests are held pending. If a number of interrupt requests with the same priority are generated at the same time, the interrupt request with the highest priority according to the priority system shown in table 5.4 is selected.

[3] Next, the priority of the selected interrupt request is compared with the interrupt mask level set in EXR. An interrupt request with a priority no higher than the mask level set at that time is held pending, and only an interrupt request with a priority higher than the interrupt mask level is accepted.

[4] When an interrupt request is accepted, interrupt exception handling starts after execution of the current instruction has been completed.

[5] The PC, CCR, and EXR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.

[6] The T bit in EXR is cleared to 0. The interrupt mask level is rewritten with the priority level of the accepted interrupt.

If the accepted interrupt is NMI, the interrupt mask level is set to H'7.

[7] A vector address is generated for the accepted interrupt, and execution of the interrupt handling routine starts at the address indicated by the contents of that vector address.

Bits 3 to 0—Data Transfer Factor (DTF3 to DTF0): These bits select the data transfer factor (activation source). There are some differences in activation sources for channel A and for channel B.

Channel A

Bit 3 DTF3	Bit 2 DTF2	Bit 1 DTF1	Bit 0 DTF0	Description
0	0	0	0	— (Initial value)
			1	Activated by A/D converter conversion end interrupt
		1	0	—
			1	—
	1	0	0	Activated by SCI channel 0 transmit-data-empty interrupt
			1	Activated by SCI channel 0 receive-data-full interrupt
		1	0	Activated by SCI channel 1 transmit-data-empty interrupt
			1	Activated by SCI channel 1 receive-data-full interrupt
1	0	0	0	Activated by TPU channel 0 compare match/input capture A interrupt
			1	Activated by TPU channel 1 compare match/input capture A interrupt
		1	0	Activated by TPU channel 2 compare match/input capture A interrupt
			1	Activated by TPU channel 3 compare match/input capture A interrupt
	1	0	0	Activated by TPU channel 4 compare match/input capture A interrupt
			1	Activated by TPU channel 5 compare match/input capture A interrupt
		1	0	—
			1	—

7.5.14 Relation Between the DMAC and External Bus Requests, Refresh Cycles, and the DTC

There can be no break between a DMA cycle read and a DMA cycle write. This means that a refresh cycle, external bus release cycle, or DTC cycle is not generated between the external read and external write in a DMA cycle.

In the case of successive read and write cycles, such as in burst transfer or block transfer, a refresh or external bus released state may be inserted after a write cycle. Since the DTC has a lower priority than the DMAC, the DTC does not operate until the DMAC releases the bus.

When DMA cycle reads or writes are accesses to on-chip memory or internal I/O registers, these DMA cycles can be executed at the same time as refresh cycles or external bus release. However, simultaneous operation may not be possible when a write buffer is used.

7.6 Interrupts

The sources of interrupts generated by the DMAC are transfer end and transfer break. Table 7.14 shows the interrupt sources and their priority order.

Table 7.14 Interrupt Source Priority Order

Interrupt Name	Interrupt Source		Interrupt Priority Order
	Short Address Mode	Full Address Mode	
DEND0A	Interrupt due to end of transfer on channel 0A	Interrupt due to end of transfer on channel 0	High
DEND0B	Interrupt due to end of transfer on channel 0B	Interrupt due to break in transfer on channel 0	
DEND1A	Interrupt due to end of transfer on channel 1A	Interrupt due to end of transfer on channel 1	
DEND1B	Interrupt due to end of transfer on channel 1B	Interrupt due to break in transfer on channel 1	Low

Enabling or disabling of each interrupt source is set by means of the DTIE bit for the corresponding channel in DMABCR, and interrupts from each source are sent to the interrupt controller independently.

The relative priority of transfer end interrupts on each channel is decided by the interrupt controller, as shown in table 7.14.

Figure 7.39 shows a block diagram of a transfer end/transfer break interrupt. An interrupt is always generated when the DTIE bit is set to 1 while the DTE bit is cleared to 0.

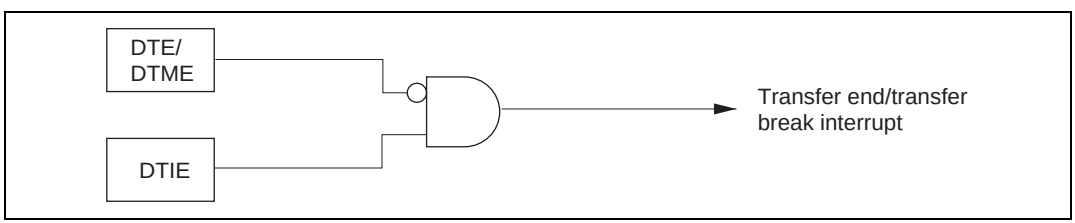

Figure 7.39 Block Diagram of Transfer End/Transfer Break Interrupt

In full address mode, a transfer break interrupt is generated when the DTME bit is cleared to 0 while the DTIEB bit is set to 1.

In both short address mode and full address mode, DMABCR should be set so as to prevent the occurrence of a combination that constitutes a condition for interrupt generation during setting.

Port	Description	Pins	Mode 4[*1]	Mode 5[*1]	Mode 6	Mode 7
Port F	• 8-bit I/O port	$PF_1/\overline{BACK}$	When BRLE = 0 (after reset): I/O port When BRLE = 1: $\overline{BREQ}$ input, $\overline{BACK}$ output			I/O ports
		$PF_0/\overline{BREQ}$				
Port G	• 5-bit I/O port	$PG_4/\overline{CS_0}$	When DDR = 0[*3]: input port When DDR = 1[*4]: $\overline{CS0}$ output			I/O ports
		$PG_3/\overline{CS_1}$	When DDR = 0 (after reset): input port When CS167E = 0 and DDR = 1: output port When CS167E = 1 and DDR = 1: $\overline{CS1}$ output			
		$PG_2/\overline{CS_2}$	When DDR = 0 (after reset): input port When CS25E = 0 and DDR = 1: output port When CS25E = 1 and DDR = 1: $\overline{CS2}$ output			
		$PG_1/\overline{CS_3}$	When DDR = 0 (after reset): input port When CS25E = 0 and DDR = 1: output port When CS25E = 1 and DDR = 1: $\overline{CS3}$ output			
		$PG_0/\overline{CAS}$[*2]	DRAM space set: $\overline{CAS}$ output Otherwise (after reset): I/O port			

Notes: 1. Only modes 4 and 5 are provided in the ROMless version.
2. The $\overline{DACK1}$, $\overline{DACK0}$, $\overline{TEND1}$, $\overline{DREQ1}$, $\overline{TEND0}$, $\overline{DREQ0}$ and $\overline{LCAS}$ are not supported in the H8S/2321.
3. After a reset in mode 6.
4. After a reset in mode 4 or 5.

Pin	Selection Method and Pin Functions
$P1_6/PO_{14}/TIOCA_2$	The pin function is switched as shown below according to the combination of the TPU channel 2 setting (by bits MD3 to MD0 in TMDR2, bits IOA3 to IOA0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bit NDER14 in NDERH, and bit P16DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)		
P16DDR	—	0	1	1
NDER14	—	—	0	1
Pin function	$TIOCA_2$ output	$P1_6$ input	$P1_6$ output	PO_{14} output
		$TIOCA_2$ input*1		

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0011	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. $TIOCA_2$ input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 = 1.
2. $TIOCB_2$ output is disabled.

Channel	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	Description		
0	0	0	0	0	TGR0C is output compare register*[1]	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR0C is input capture register*[1]	Capture input source is TIOCC0 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges
		1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/count-down

*: Don't care

Note: 1. When the BFA bit in TMDR0 is set to 1 and TGR0C is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Example of Non-Overlapping Pulse Output (Example of Four-Phase Complementary Non-Overlapping Output): Figure 11.7 shows an example in which pulse output is used for four-phase complementary non-overlapping pulse output.

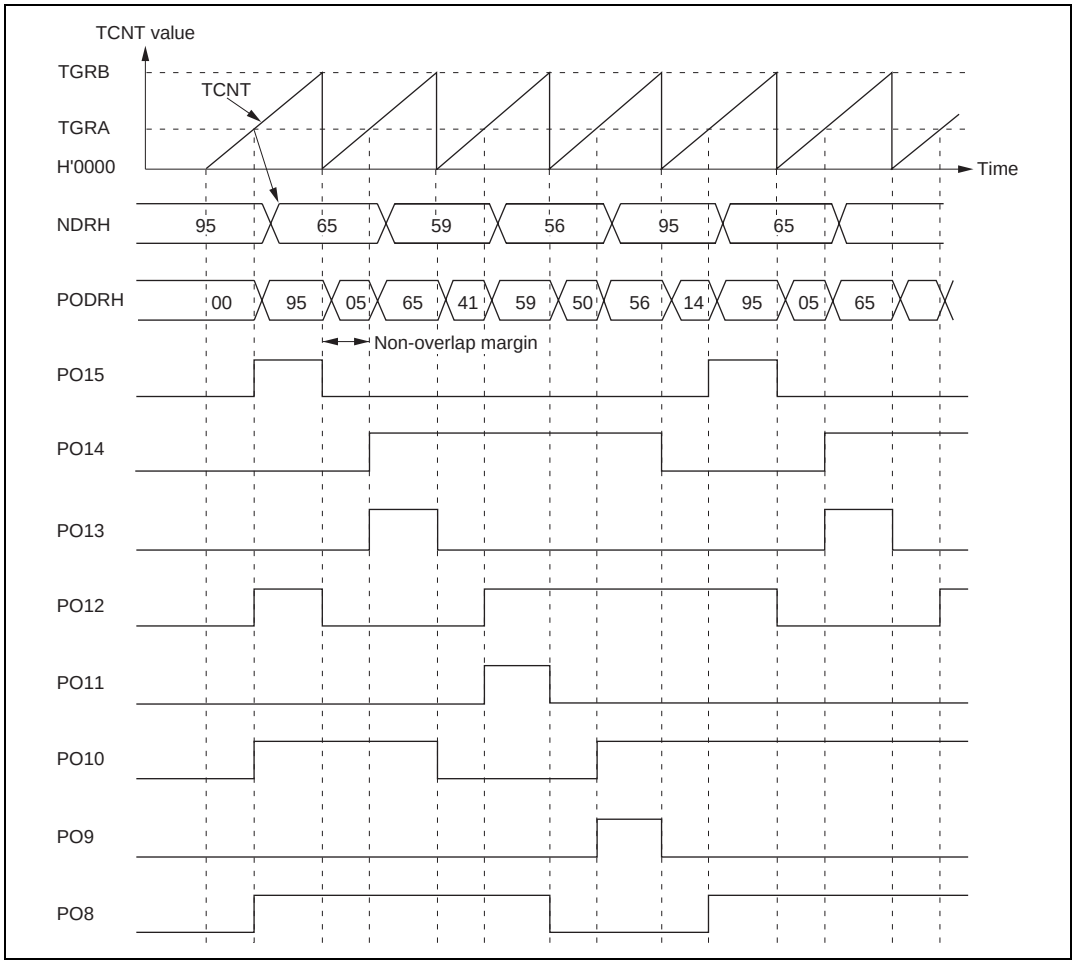

Figure 11.7 Non-Overlapping Pulse Output Example (Four-Phase Complementary)

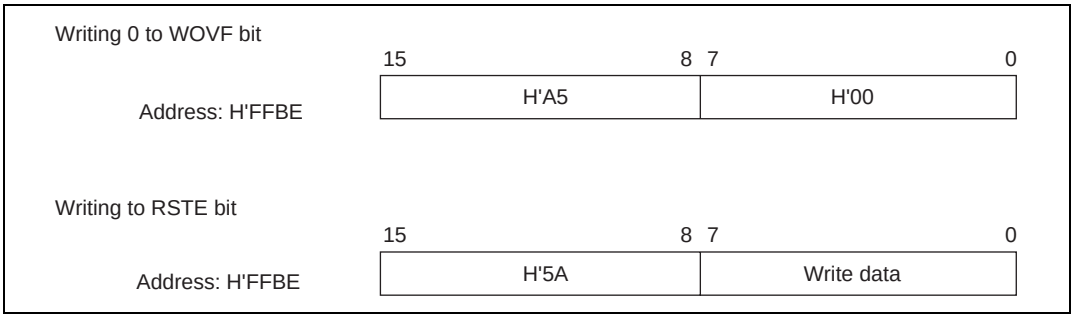

Figure 13.3 Writing to RSTCSR

Reading TCNT, TCSR, and RSTCSR: These registers are read in the same way as other registers. The read addresses are H'FFBC for TCSR, H'FFBD for TCNT, and H'FFBF for RSTCSR.

13.3 Operation

13.3.1 Operation in Watchdog Timer Mode

To use the WDT as a watchdog timer, set the WT/$\overline{IT}$ and TME bits to 1. Software must prevent TCNT overflows by rewriting the TCNT value (normally be writing H'00) before overflow occurs. This ensures that TCNT does not overflow while the system is operating normally. If TCNT overflows without being rewritten because of a system crash or other error, the $\overline{WDTOVF}$ signal* is output. This is shown in figure 13.4. This $\overline{WDTOVF}$ signal* can be used to reset the system. The $\overline{WDTOVF}$ signal* is output for 132 states when RSTE = 1, and for 130 states when RSTE = 0.

If TCNT overflows when 1 is set in the RSTE bit in RSTCSR, a signal that resets the chip internally is generated at the same time as the $\overline{WDTOVF}$ signal*. The internal reset signal is output for 518 states.

If a reset caused by a signal input to the $\overline{RES}$ pin occurs at the same time as a reset caused by a WDT overflow, the $\overline{RES}$ pin reset has priority and the WOVF bit in RSTCSR is cleared to 0.

Note: * The $\overline{WDTOVF}$ pin function cannot be used in the F-ZTAT versions.

	φ = 3.6864 MHz			φ = 4 MHz			φ = 4.9152 MHz			φ = 5 MHz		
Bit Rate (bits/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	64	0.70	2	70	0.03	2	86	0.31	2	88	–0.25
150	1	191	0.00	1	207	0.16	1	255	0.00	2	64	0.16
300	1	95	0.00	1	103	0.16	1	127	0.00	1	129	0.16
600	0	191	0.00	0	207	0.16	0	255	0.00	1	64	0.16
1200	0	95	0.00	0	103	0.16	0	127	0.00	0	129	0.16
2400	0	47	0.00	0	51	0.16	0	63	0.00	0	64	0.16
4800	0	23	0.00	0	25	0.16	0	31	0.00	0	32	–1.36
9600	0	11	0.00	0	12	0.16	0	15	0.00	0	15	1.73
19200	0	5	0.00	0	6	—	0	7	0.00	0	7	1.73
31250	—	—	—	0	3	0.00	0	4	–1.70	0	4	0.00
38400	0	2	0.00	0	2	—	0	3	0.00	0	3	1.73

	φ = 6 MHz			φ = 6.144 MHz			φ = 7.3728 MHz			φ = 8 MHz		
Bit Rate (bits/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	106	–0.44	2	108	0.08	2	130	–0.07	2	141	0.03
150	2	77	0.16	2	79	0.00	2	95	0.00	2	103	0.16
300	1	155	0.16	1	159	0.00	1	191	0.00	1	207	0.16
600	1	77	0.16	1	79	0.00	1	95	0.00	1	103	0.16
1200	0	155	0.16	0	159	0.00	0	191	0.00	0	207	0.16
2400	0	77	0.16	0	79	0.00	0	95	0.00	0	103	0.16
4800	0	38	0.16	0	39	0.00	0	47	0.00	0	51	0.16
9600	0	19	–2.34	0	19	0.00	0	23	0.00	0	25	0.16
19200	0	9	–2.34	0	9	0.00	0	11	0.00	0	12	0.16
31250	0	5	0.00	0	5	2.40	—	—	—	0	7	0.00
38400	0	4	–2.34	0	4	0.00	0	5	0.00	—	—	—

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). Writing 1 to the FLSHE bit enables the flash memory control registers to be read and written to. Clearing FLSHE to 0 designates these registers as unselected (the register contents are retained).

Bit 3 FLSHE	Description
0	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB (Initial value)
1	Flash control registers are selected for addresses H'FFFFC8 to H'FFFFCB

Bits 2 to 0—Reserved: These bits cannot be modified and are always read as 0.

19.14.6 RAM Emulation Register (RAMER)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

RAMER specifies the area of flash memory to be overlapped with part of RAM when emulating real-time flash memory programming. RAMER is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode. RAMER settings should be made in user mode or user program mode.

Flash memory area divisions are shown in table 19.29. To ensure correct operation of the emulation function, the ROM for which RAM emulation is performed should not be accessed immediately after this register has been modified. Normal execution of an access immediately after register modification is not guaranteed.

Bits 7 to 4—Reserved: These bits cannot be modified and are always read as 0.

- Before branching to the programming control program (RAM area H'FFE400 to H'FFFBFF), the chip terminates transmit and receive operations by the on-chip SCI (channel 1) (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. The transmit data output pin, TxD1, goes to the high-level output state (P31DDR = 1, P31DR = 1).

- The contents of the CPU's internal general registers are undefined at this time, so these registers must be initialized immediately after branching to the programming control program. In particular, since the stack pointer (SP) is used implicitly in subroutine calls, etc., a stack area must be specified for use by the programming control program.

- Initial settings must also be made for the other on-chip registers.

- Boot mode can be entered by making the pin settings shown in table 19.30 and executing a reset-start.

- Boot mode can be cleared by driving the reset pin low, waiting at least 20 states, then setting the FWE pin and mode pins, and executing reset release*1. Boot mode can also be cleared by a WDT overflow reset.

- Do not change the mode pin input levels in boot mode, and do not drive the FWE pin low while the boot program is being executed or while flash memory is being programmed or erased*2.

- If the mode pin input levels are changed (for example, from low to high) during a reset, the state of ports with multiplexed address functions and bus control output pins ($\overline{AS}$, $\overline{RD}$, $\overline{HWR}$) will change according to the change in the microcomputer's operating mode*3.

  Therefore, care must be taken to make pin settings to prevent these pins from becoming output signal pins during a reset, or to prevent collision with signals outside the microcomputer.

Notes: 1. Mode pins and FWE pin input must satisfy the mode programming setup time (t_{MDS} = 200 ns) with respect to the reset release timing, as shown in figures 19.56 to 19.58.
2. For further information on FWE application and disconnection, see section 19.21, Flash Memory Programming and Erasing Precautions.
3. See section 9, I/O Ports.

Automatic SCI Bit Rate Adjustment: When boot mode is initiated, the H8S/2326 F-ZTAT chip measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The chip calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the chip's system clock frequency, there will be a discrepancy between the bit rates of the host and the chip. To ensure correct SCI operation, the host's transfer bit rate should be set to 9,600 or 19,200 bps.

Table 19.52 shows typical host transfer bit rates and system clock frequencies for which automatic adjustment of the MCU's bit rate is possible. The boot program should be executed within this system clock range.

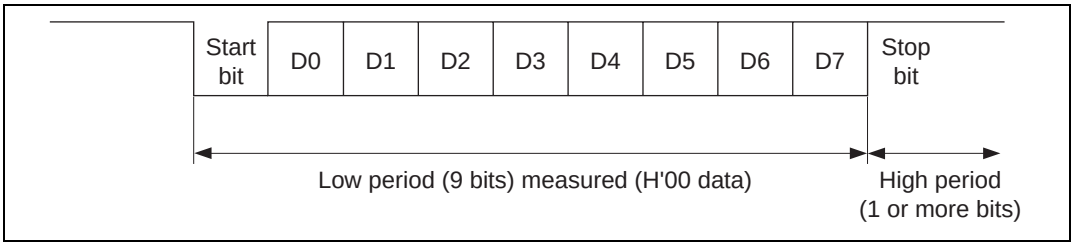

Figure 19.68 Automatic SCI Bit Rate Adjustment

Table 19.52 System Clock Frequencies for which Automatic Adjustment of H8S/2326 F-ZTAT Bit Rate is Possible

Host Bit Rate	System Clock Frequency for which Automatic Adjustment of H8S/2326 F-ZTAT Bit Rate is Possible
19,200 bps	16 MHz to 25 MHz
9,600 bps	8 MHz to 25 MHz

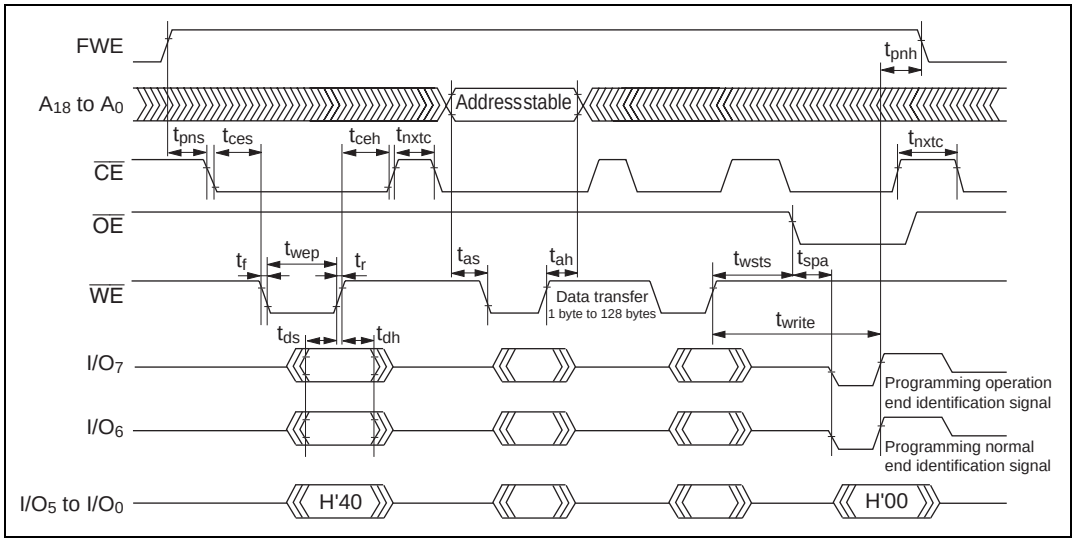

Figure 19.82 Auto-Program Mode Timing Waveforms

19.29.6 Auto-Erase Mode

- Auto-erase mode supports only total memory erasing.
- Do not perform a command write during auto-erasing.
- Confirm normal end of auto-erasing by checking I/O_6. Alternatively, status read mode can also be used for this purpose (the I/O_7 status polling pin is used to identify the end of an auto-erase operation).
- Status polling I/O_6 and I/O_7 pin information is retained until the next command write. As long as the next command write has not been performed, reading is possible by enabling $\overline{CE}$ and $\overline{OE}$.

PCDDR—Port C Data Direction Register H'FEBB Port C

Bit	7	6	5	4	3	2	1	0
	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port C pins

PDDDR—Port D Data Direction Register H'FEBC Port D

Bit	7	6	5	4	3	2	1	0
	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port D pins

PEDDR—Port E Data Direction Register H'FEBD Port E

Bit	7	6	5	4	3	2	1	0
	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port E pins

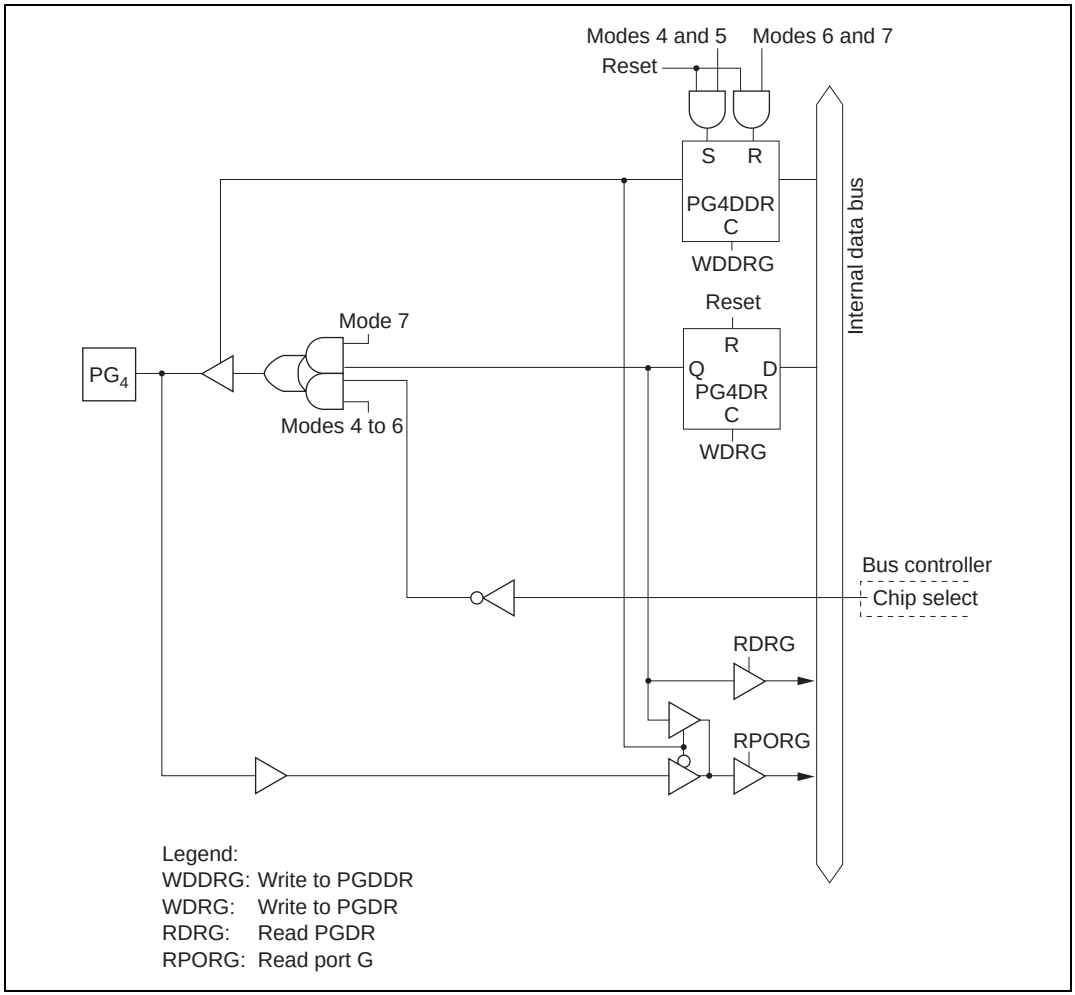

Figure C.13 (d) Port G Block Diagram (Pin PG_4)