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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2329bvte25v

Type	Symbol	Pin No. TFP-120	Pin No. FP-128B	I/O	Name and Function
Operating mode control	MD_2 to MD_0	115 to 113	125 to 123	Input	Mask ROM and ROMless versions, H8S/2329B F-ZTAT:

MD_2	MD_1	MD_0	Operating Mode
0	0	1	—
	1	0	Mode 2*1
		1	Mode 3*1
1	0	0	Mode 4*2
		1	Mode 5*2
	1	0	Mode 6
		1	Mode 7

Notes: 1. Applies to the H8S/2329B F-ZTAT only.

2. The ROMless versions can use only modes 4 and 5.

Type	Symbol	Pin No. TFP-120	Pin No. FP-128B	I/O	Name and Function
System control	$\overline{RES}$	73	81	Input	**Reset input:** When this pin is driven low, the chip is reset.
	$\overline{STBY}$	75	83	Input	**Standby:** When this pin is driven low, a transition is made to hardware standby mode.
	$\overline{BREQ}$	88	96	Input	**Bus request:** Used by an external bus master to issue a bus request to the chip.
	$\overline{BREQO}$	86, 92	94, 102	Output	**Bus request output:** The external bus request signal used when an internal bus master accesses external space in the external bus-released state.
	$\overline{BACK}$	87	95	Output	**Bus request acknowledge:** Indicates that the bus has been released to an external bus master.

Type	Instruction	Size*1	Function
Bit-manipulation instructions	BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C Exclusive-ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
	BIXOR	B	C ⊕ ¬ (<bit-No.> of <EAd>) → C Exclusive-ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
	BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory operand to the carry flag.
	BILD	B	¬ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
	BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand.
	BIST	B	¬ C → (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.

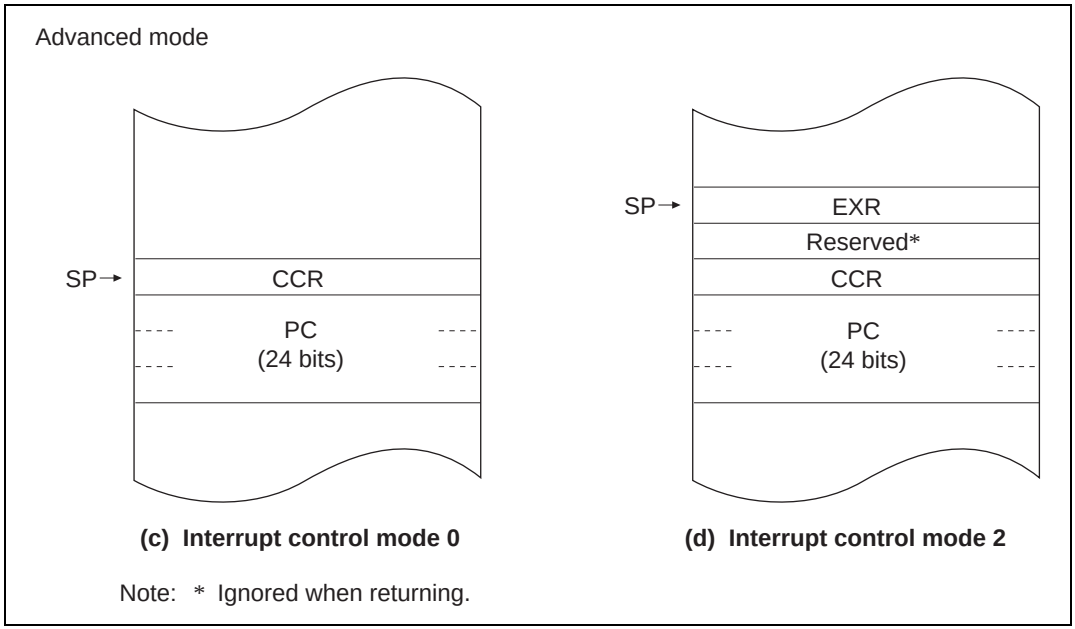


Figure 2.13 Stack Structure after Exception Handling (Examples)

2.8.4 Program Execution State

In this state the CPU executes program instructions in sequence.

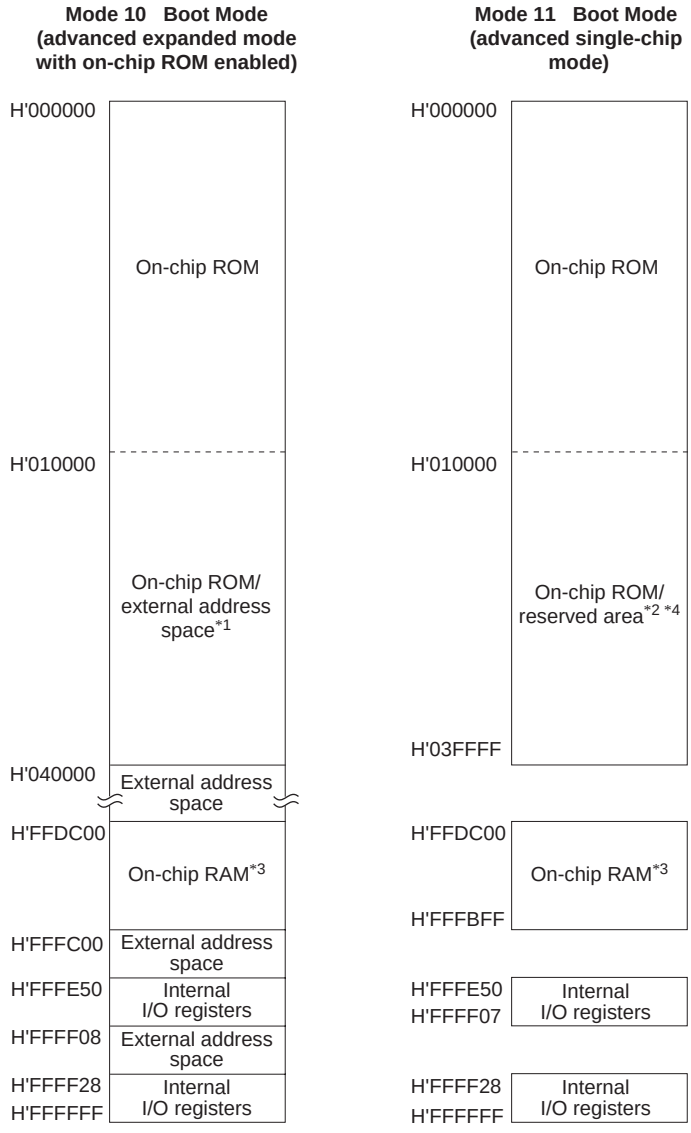
2.8.5 Bus-Released State

This is a state in which the bus has been released in response to a bus request from a bus master other than the CPU. While the bus is released, the CPU halts.

There is one other bus master in addition to the CPU: the DMA controller (DMAC)* and data transfer controller (DTC).

For further details, refer to section 6, Bus Controller.

Note: * The DMAC is not supported in the H8S/2321.



Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.
4. Do not access a reserved area.

Figure 3.2 (b) H8S/2328 Memory Map in Each Operating Mode (F-ZTAT Only)

5.1.2 Block Diagram

A block diagram of the interrupt controller is shown in figure 5.1.

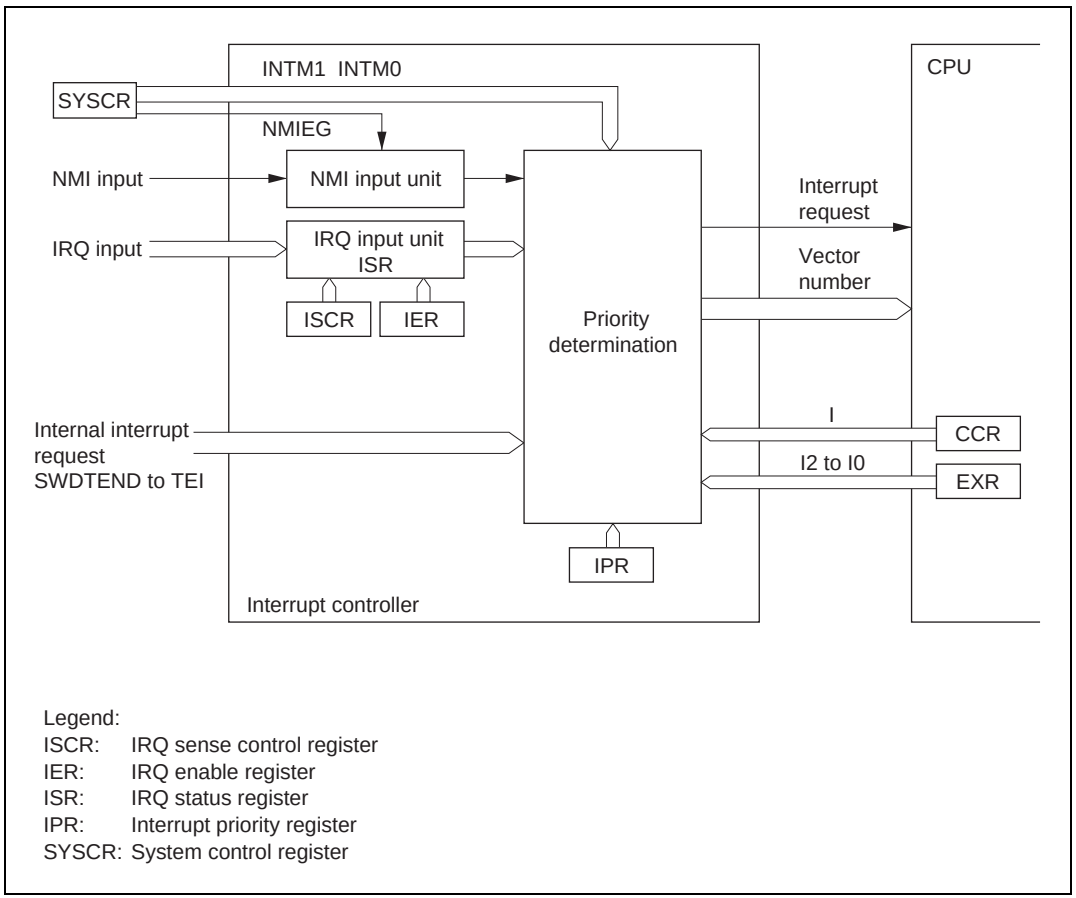


Figure 5.1 Block Diagram of Interrupt Controller

6.3 Overview of Bus Control

6.3.1 Area Partitioning

In advanced mode, the bus controller partitions the 16-Mbyte address space into eight areas, 0 to 7, in 2-Mbyte units, and performs bus control for external space in area units. Figure 6.2 shows an outline of the memory map.

Chip select signals ($\overline{CS0}$ to $\overline{CS7}$) can be output for each area.

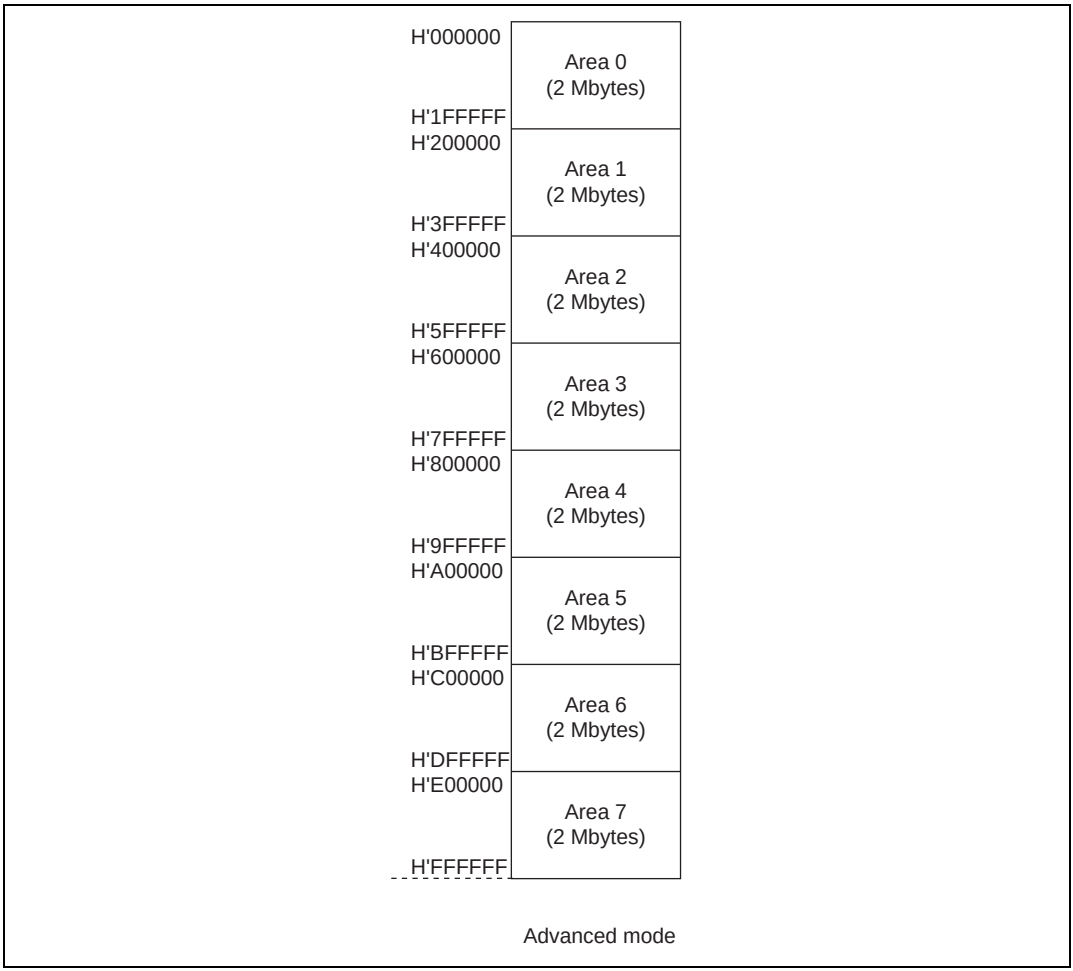


Figure 6.2 Overview of Area Partitioning

Figure 6.14 shows an example of wait state insertion timing.

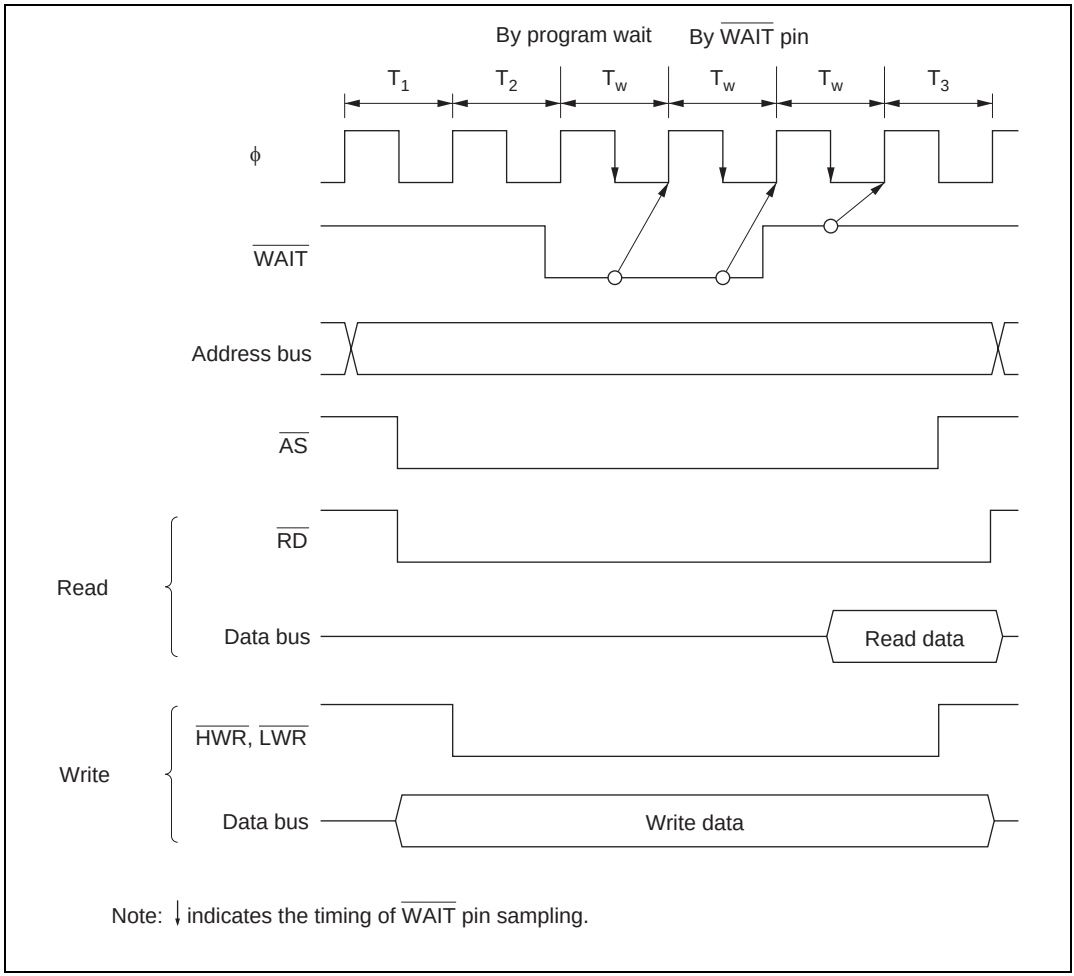


Figure 6.14 Example of Wait State Insertion Timing

The settings after a power-on reset are: 3-state access, 3 program wait state insertion, and WAIT input disabled.

Bit 14—Full Address Enable 0 (FAE0): Specifies whether channel 0 is to be used in short address mode or full address mode.

In short address mode, channels 0A and 0B can be used as independent channels.

Bit 14 FAE0	Description	
0	Short address mode	(Initial value)
1	Full address mode	

Bit 13—Single Address Enable 1 (SAE1): Specifies whether channel 1B is to be used for transfer in dual address mode or single address mode.

This bit is invalid in full address mode.

Bit 13 SAE1	Description	
0	Transfer in dual address mode	(Initial value)
1	Transfer in single address mode	

Bit 12—Single Address Enable 0 (SAE0): Specifies whether channel 0B is to be used for transfer in dual address mode or single address mode.

This bit is invalid in full address mode.

Bit 12 SAE0	Description	
0	Transfer in dual address mode	(Initial value)
1	Transfer in single address mode	

Bits 11 to 8—Data Transfer Acknowledge (DTA): These bits enable or disable clearing, when DMA transfer is performed, of the internal interrupt source selected by the data transfer factor setting.

When DTE = 1 and DTA = 1, the internal interrupt source selected by the data transfer factor setting is cleared automatically by DMA transfer. When DTE = 1 and DTA = 1, the internal interrupt source selected by the data transfer factor setting does not issue an interrupt request to the CPU or DTC.

Bit 1 TGIEB	Description	
0	Interrupt requests (TGIB) by TGFB disabled	(Initial value)
1	Interrupt requests (TGIB) by TGFB enabled	

Bit 0—TGR Interrupt Enable A (TGIEA): Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1.

Bit 0 TGIEA	Description	
0	Interrupt requests (TGIA) by TGFA disabled	(Initial value)
1	Interrupt requests (TGIA) by TGFA enabled	

10.2.5 Timer Status Registers (TSR)

Channel 0: TSR0

Channel 3: TSR3

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

Channel 1: TSR1

Channel 2: TSR2

Channel 4: TSR4

Channel 5: TSR5

Bit	:	7	6	5	4	3	2	1	0
		TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

Figure 10.27 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

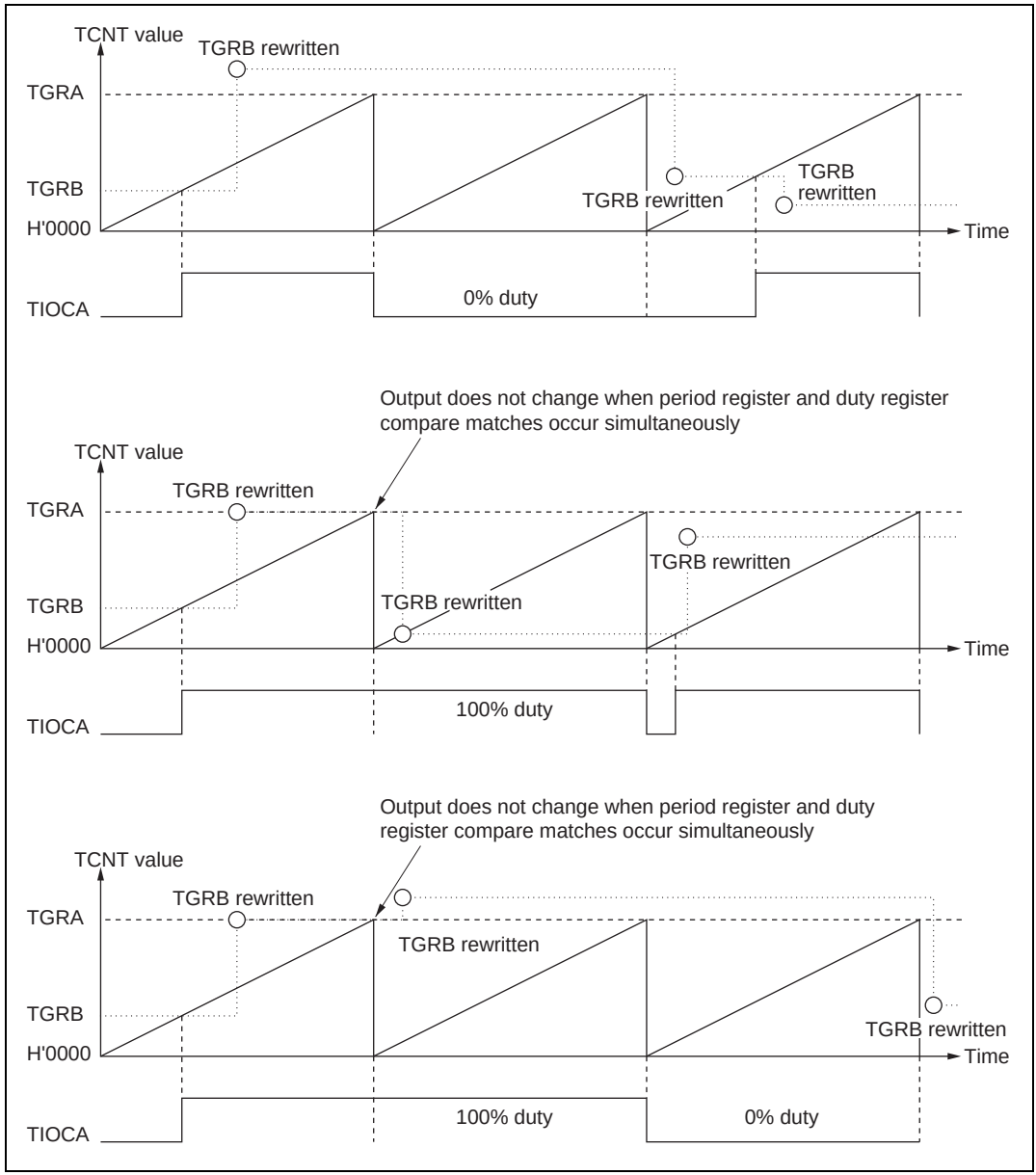


Figure 10.27 Examples of PWM Mode Operation (3)

14.3.4 Operation in Synchronous Mode

In synchronous mode, data is transmitted or received in synchronization with clock pulses, making it suitable for high-speed serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

Figure 14.14 shows the general format for synchronous serial communication.

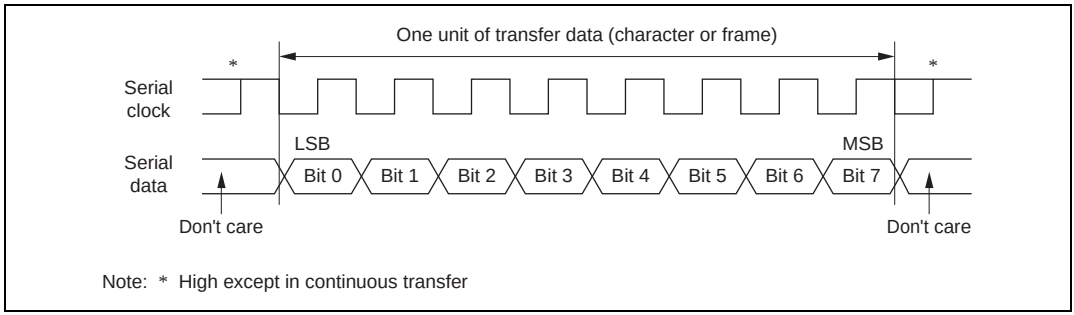


Figure 14.14 Data Format in Synchronous Communication

In synchronous serial communication, data on the communication line is output from one falling edge of the serial clock to the next. Data confirmation is guaranteed at the rising edge of the serial clock.

In synchronous serial communication, one character consists of data output starting with the LSB and ending with the MSB. After the MSB is output, the communication line holds the MSB state.

In synchronous mode, the SCI receives data in synchronization with the rising edge of the serial clock.

Data Transfer Format

A fixed 8-bit data format is used.

No parity or multiprocessor bits are added.

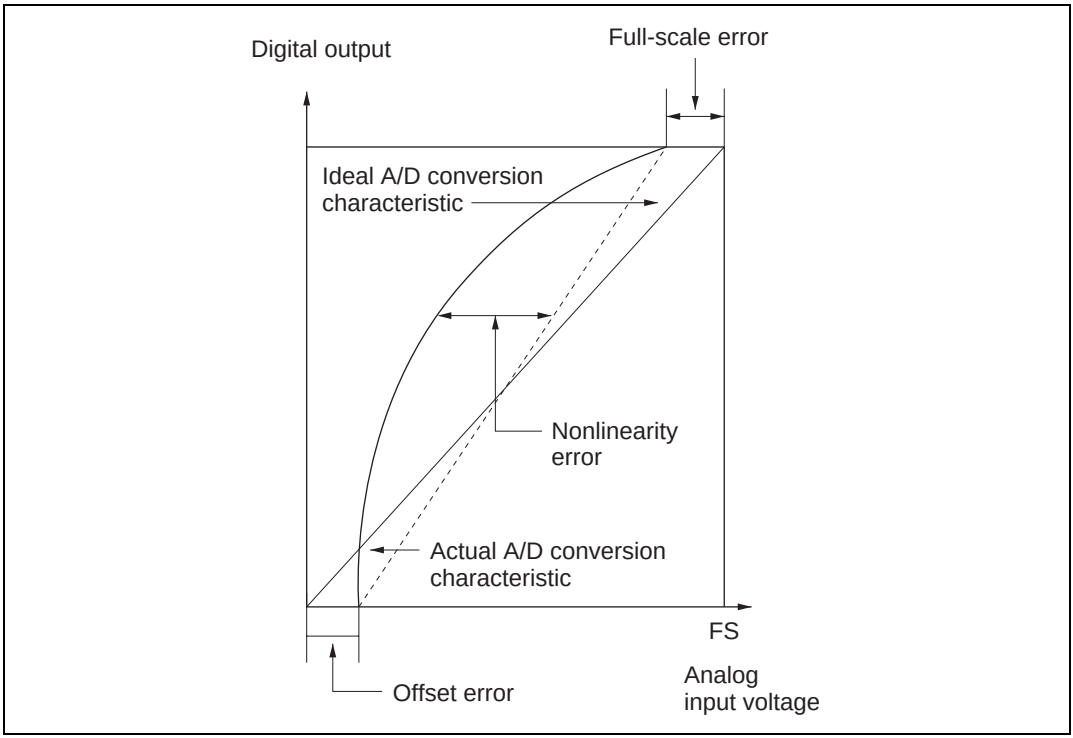


Figure 16.9 A/D Conversion Precision Definitions (2)

Permissible Signal Source Impedance: The chip's analog input is designed so that conversion precision is guaranteed for an input signal for which the signal source impedance is 5 kΩ or less. This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance exceeds 5 kΩ, charging may be insufficient and it may not be possible to guarantee the A/D conversion precision.

If a large capacitance is provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, since a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., 5 mV/μs or greater).

When converting a high-speed analog signal, a low-impedance buffer should be inserted.

21.5 Module Stop Mode

21.5.1 Module Stop Mode

Module stop mode can be set for individual on-chip supporting modules.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. The CPU continues operating independently.

Table 21.3 shows MSTP bits and the corresponding on-chip supporting modules.

When the corresponding MSTP bit is cleared to 0, module stop mode is cleared and the module starts operating at the end of the bus cycle. In module stop mode, the internal states of modules other than the SCI and A/D converter are retained.

After reset clearance, all modules other than DMAC* and DTC are in module stop mode.

When an on-chip supporting module is in module stop mode, read/write access to its registers is disabled.

Do not make a transition to sleep mode with MSTPCR set to H'FFFF or H'EFFF, as this will halt operation of the bus controller.

Note: * The DMAC is not supported in the H8S/2321.

Table 21.3 MSTP Bits and Corresponding On-Chip Supporting Modules

Register	Bit	Module
MSTPCRH	MSTP15	DMA controller (DMAC)*
	MSTP14	Data transfer controller (DTC)
	MSTP13	16-bit timer-pulse unit (TPU)
	MSTP12	8-bit timer module
	MSTP11	Programmable pulse generator (PPG)
	MSTP10	D/A converter (channels 0 and 1)
	MSTP9	A/D converter
	MSTP8	—
MSTPCRL	MSTP7	Serial communication interface (SCI) channel 2
	MSTP6	Serial communication interface (SCI) channel 1
	MSTP5	Serial communication interface (SCI) channel 0
	MSTP4	—
	MSTP3	—
	MSTP2	—
	MSTP1	—
	MSTP0	—

Notes: Bits 8 and 4 to 0 can be read or written to, but do not affect operation.
* The DMAC is not supported in the H8S/2321.

21.5.2 Usage Notes

DMAC*/DTC Module Stop: Depending on the operating status of the DMAC* or DTC, the MSTP15 and MSTP14 bits may not be set to 1. Setting of the DMAC* or DTC module stop mode should be carried out only when the respective module is not activated.

For details, refer to section 7, DMA Controller, and section 8, Data Transfer Controller.

On-Chip Supporting Module Interrupts: Relevant interrupt operations cannot be performed in module stop mode. Consequently, if module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DMAC* or DTC activation source. Interrupts should therefore be disabled before entering module stop mode.

Writing to MSTPCR: MSTPCR should only be written to by the CPU.

Note: * The DMAC is not supported in the H8S/2321.

Table 22.14 Permissible Output Currents

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	$\sum I_{OL}$	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Note: To protect chip reliability, do not exceed the output current values in table 22.14.

(6) Branch Instructions

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes) #xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	—	Operation	Branching Condition	Condition Code I	H	N	Z	V	C	No. of States*1 Advanced
Bcc	BRA d:8(BT d:8)	—							2			if condition is true then	Always	—	—	—	—	—	—	2
	BRA d:16(BT d:16)	—							4			PC←PC+d		—	—	—	—	—	—	3
	BRN d:8(BF d:8)	—							2			else next;	Never	—	—	—	—	—	—	2
	BRN d:16(BF d:16)	—							4					—	—	—	—	—	—	3
	BHI d:8	—							2				C∨Z=0	—	—	—	—	—	—	2
	BHI d:16	—							4					—	—	—	—	—	—	3
	BLS d:8	—							2				C∨Z=1	—	—	—	—	—	—	2
	BLS d:16	—							4					—	—	—	—	—	—	3
	BCC d:B(BHS d:8)	—							2				C=0	—	—	—	—	—	—	2
	BCC d:16(BHS d:16)	—							4					—	—	—	—	—	—	3
	BCS d:8(BLO d:8)	—							2				C=1	—	—	—	—	—	—	2
	BCS d:16(BLO d:16)	—							4					—	—	—	—	—	—	3
	BNE d:8	—							2				Z=0	—	—	—	—	—	—	2
	BNE d:16	—							4					—	—	—	—	—	—	3
	BEQ d:8	—							2				Z=1	—	—	—	—	—	—	2
	BEQ d:16	—							4					—	—	—	—	—	—	3
	BVC d:8	—							2				V=0	—	—	—	—	—	—	2
	BVC d:16	—							4					—	—	—	—	—	—	3

IPRA — Interrupt Priority Register A	**H'FEC4**	**Interrupt Controller**
IPRB — Interrupt Priority Register B	**H'FEC5**	**Interrupt Controller**
IPRC — Interrupt Priority Register C	**H'FEC6**	**Interrupt Controller**
IPRD — Interrupt Priority Register D	**H'FEC7**	**Interrupt Controller**
IPRE — Interrupt Priority Register E	**H'FEC8**	**Interrupt Controller**
IPRF — Interrupt Priority Register F	**H'FEC9**	**Interrupt Controller**
IPRG — Interrupt Priority Register G	**H'FECA**	**Interrupt Controller**
IPRH — Interrupt Priority Register H	**H'FECB**	**Interrupt Controller**
IPRI — Interrupt Priority Register I	**H'FECC**	**Interrupt Controller**
IPRJ — Interrupt Priority Register J	**H'FECD**	**Interrupt Controller**
IPRK — Interrupt Priority Register K	**H'FECE**	**Interrupt Controller**

Bit :	7	6	5	4	3	2	1	0
	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0
Initial value :	0	1	1	1	0	1	1	1
Read/Write :	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Set priority (levels 7 to 0) for interrupt sources

Correspondence between Interrupt Sources and IPR Settings

Register	Bits	
	6 to 4	2 to 0
IPRA	IRQ0	IRQ1
IPRB	IRQ2	IRQ4
	IRQ3	IRQ5
IPRC	IRQ6	DTC
	IRQ7	
IPRD	WDT	Refresh timer*2
IPRE	—*1	A/D converter
IPRF	TPU channel 0	TPU channel 1
IPRG	TPU channel 2	TPU channel 3
IPRH	TPU channel 4	TPU channel 5
IPRI	8-bit timer channel 0	8-bit timer channel 1
IPRJ	DMAC*2	SCI channel 0
IPRK	SCI channel 1	SCI channel 2

Notes: 1. Reserved bits.
2. Reserved bit in the H8S/2321.

Short address mode

Bit	:	15	14	13	12	11	10	9	8
DMABCRH	:	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0A Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0B Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1A Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1B Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0B Single Address Enable

0	Transfer in dual address mode
1	Transfer in single address mode

Channel 1B Single Address Enable

0	Transfer in dual address mode
1	Transfer in single address mode

Channel 0 Full Address Enable

0	Short address mode
1	Full address mode

Channel 1 Full Address Enable

0	Short address mode
1	Full address mode

(Continued on next page)

SMR2—Serial Mode Register 2 **H'FF88** **Smart Card Interface 2**

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ϕ clock
	1	ϕ/4 clock
1	0	ϕ/16 clock
	1	ϕ/64 clock

Base Clock Pulse

BCP1	BCP0	Base Clock Pulse
0	0	32 clocks
	1	64 clocks
1	0	372 clocks
	1	256 clocks

Parity Mode
(Set to 1 when using the smart card interface)

0	Even parity
1	Odd parity

Parity Enable

0	Setting prohibited
1	Parity bit addition and checking enabled

Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generated 12.5 etu (11.5 etu in block transfer mode) after beginning of start bit • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generated 11.0 etu after beginning of start bit • Fixed high/low-level control possible (set in SCR) in addition to clock output on/off control

Note: etu: Elementary time unit (time for transfer of 1 bit)