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Details

Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2329bvte25wv

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4.7 Notes on Use of the Stack

When accessing word data or longword data, the chip assumes that the lowest address bit is 0. The stack should always be accessed by word transfer instruction or longword transfer instruction, and the value of the stack pointer (SP, ER7) should always be kept even. Use the following instructions to save registers:

```
PUSH.W   Rn      (or MOV.W Rn, @-SP)
PUSH.L   ERn     (or MOV.L ERn, @-SP)
```

Use the following instructions to restore registers:

```
POP.W    Rn      (or MOV.W @SP+, Rn)
POP.L    ERn     (or MOV.L @SP+, ERn)
```

Setting SP to an odd value may lead to a malfunction. Figure 4.5 shows an example of what happens when the SP value is odd.

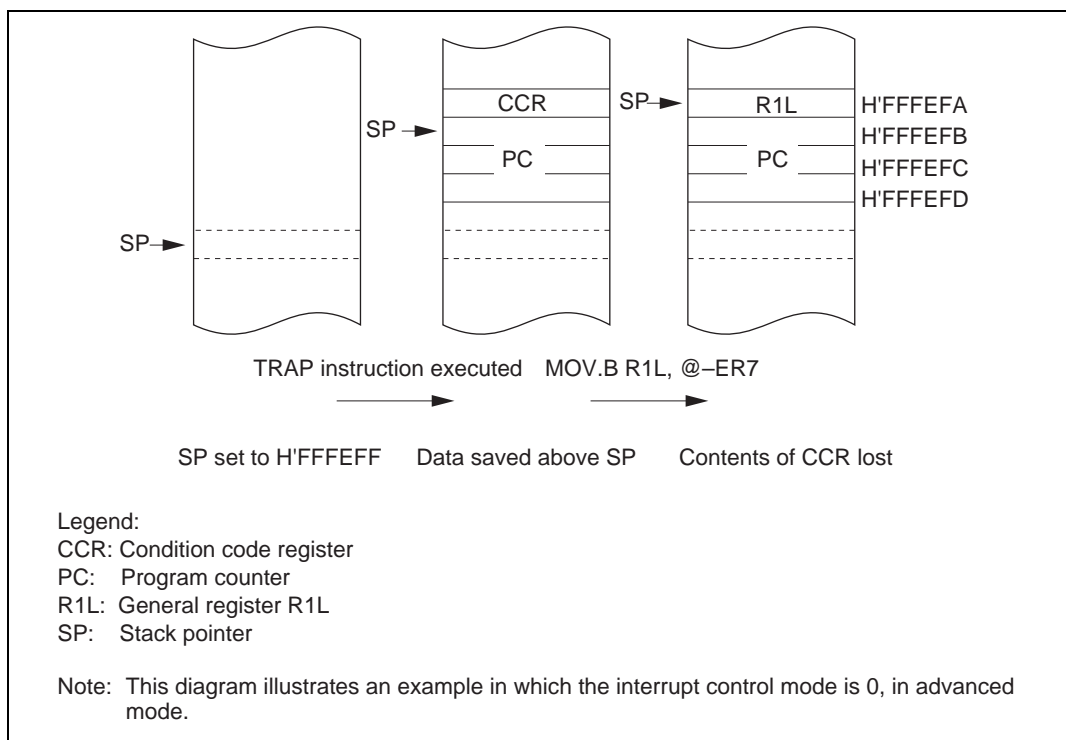


Figure 4.5 Operation when SP Value is Odd



Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address ^{*1}	IPR	Priority	DTC Activation	DMAC Activation ^{*2}
Power-on reset		0	H'0000	—	<div>High</div> <div></div> <div>Low</div>	—	—
Reserved		1	H'0004				
Reserved for system use		2	H'0008				
		3	H'000C				
		4	H'0010				
Trace		5	H'0014				
Reserved for system use		6	H'0018				
NMI	External pin	7	H'001C				
Trap instruction (4 sources)		8	H'0020				
		9	H'0024				
		10	H'0028				
		11	H'002C				
Reserved for system use		12	H'0030				
		13	H'0034				
		14	H'0038				
		15	H'003C				
IRQ ₀	External pin	16	H'0040	IPRA6 to IPRA4		○	—
IRQ ₁		17	H'0044	IPRA2 to IPRA0		○	—
IRQ ₂		18	H'0048	IPRB6 to IPRB4		○	—
IRQ ₃		19	H'004C			○	—
IRQ ₄		20	H'0050	IPRB2 to IPRB0		○	—
IRQ ₅		21	H'0054			○	—
IRQ ₆		22	H'0058	IPRC6 to IPRC4		○	—
IRQ ₇		23	H'005C			○	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*1	IPR	Priority	DTC Activation	DMAC*2 Activation
TGI1A (TGR1A input capture/compare match)	TPU channel 1	40	H'00A0	IPRF2 to IPRF0	High	○	○
TGI1B (TGR1B input capture/compare match)		41	H'00A4			○	—
TCI1V (overflow 1)		42	H'00A8			—	—
TCI1U (underflow 1)		43	H'00AC			—	—
TGI2A (TGR2A input capture/compare match)	TPU channel 2	44	H'00B0	IPRG6 to IPRG4		○	○
TGI2B (TGR2B input capture/compare match)		45	H'00B4			○	—
TCI2V (overflow 2)		46	H'00B8			—	—
TCI2U (underflow 2)		47	H'00BC			—	—
TGI3A (TGR3A input capture/compare match)	TPU channel 3	48	H'00C0	IPRG2 to IPRG0		○	○
TGI3B (TGR3B input capture/compare match)		49	H'00C4			○	—
TGI3C (TGR3C input capture/compare match)		50	H'00C8			○	—
TGI3D (TGR3D input capture/compare match)		51	H'00CC			○	—
TCI3V (overflow 3)	—	52	H'00D0		Low	—	—
Reserved		53	H'00D4			—	—
		54	H'00D8				
		55	H'00DC				

5.5 Usage Notes

5.5.1 Contention between Interrupt Generation and Disabling

When an interrupt enable bit is cleared to 0 to disable interrupts, the disabling becomes effective after execution of the instruction.

In other words, when an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request of higher priority than that interrupt, interrupt exception handling will be executed for the higher-priority interrupt, and the lower-priority interrupt will be ignored.

The same also applies when an interrupt source flag is cleared.

Figure 5.8 shows an example in which the TGIEA bit in the TPU's TIER0 register is cleared to 0.

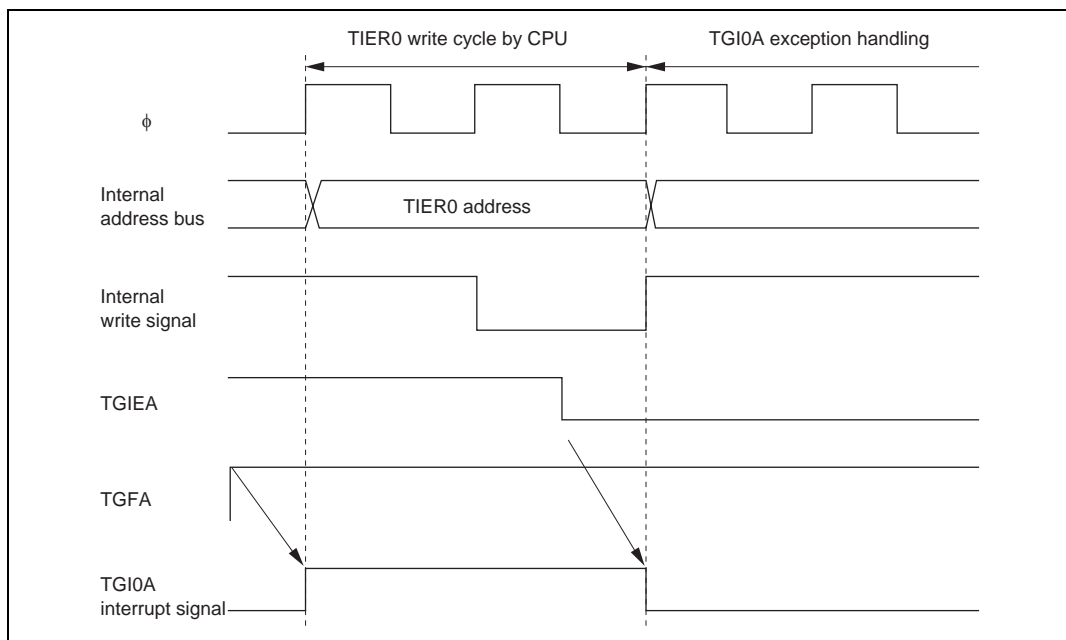


Figure 5.8 Contention between Interrupt Generation and Disabling

The above contention will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

6.10.4 Transition Timing

Figure 6.37 shows the timing for transition to the bus released state.

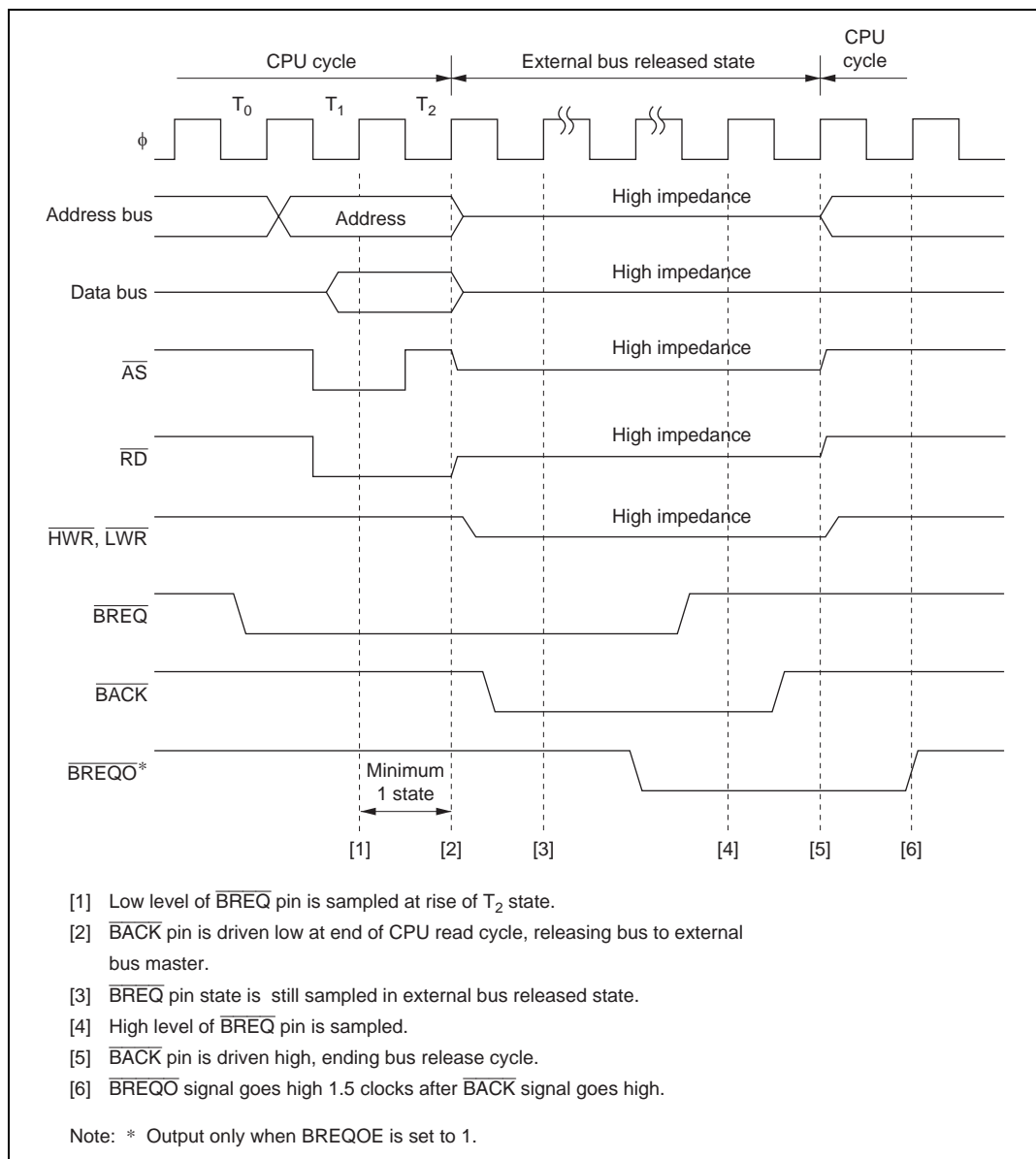


Figure 6.37 Bus Released State Transition Timing

As a refresh* and an external access by an internal bus master can be executed simultaneously, there is no relative order of priority for these two operations.

Note: * The DMAC and DRAM interface are not supported in the H8S/2321.

6.11.3 Bus Transfer Timing

Even if a bus request is received from a bus master with a higher priority than that of the bus master that has acquired the bus and is currently operating, the bus is not necessarily transferred immediately. There are specific times at which each bus master can relinquish the bus.

CPU: The CPU is the lowest-priority bus master, and if a bus request is received from the DTC or DMAC*, the bus arbiter transfers the bus to the bus master that issued the request. The timing for transfer of the bus is as follows:

- The bus is transferred at a break between bus cycles. However, if a bus cycle is executed in discrete operations, as in the case of a longword-size access, the bus is not transferred between the operations. See appendix A.5, Bus States during Instruction Execution, for timings at which the bus is not transferred.
- If the CPU is in sleep mode, it transfers the bus immediately.

DTC: The DTC sends the bus arbiter a request for the bus when an activation request is generated.

The DTC can release the bus after a vector read, a register information read (3 states), a single data transfer, or a register information write (3 states). It does not release the bus during a register information read (3 states), a single data transfer, or a register information write (3 states).

DMAC*: The DMAC sends the bus arbiter a request for the bus when an activation request is generated.

In the case of an external request in short address mode or normal mode, and in cycle steal mode, the DMAC releases the bus after a single transfer.

In block transfer mode, it releases the bus after transfer of one block, and in burst mode, after completion of a transfer.

Note: * The DMAC is not supported in the H8S/2321.

Bit 2—Data Transfer Interrupt Enable 1A (DTIE1A): Enables or disables the channel 1 transfer end interrupt.

Bit 2

DTIE1A	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

Bit 0—Data Transfer Interrupt Enable 0A (DTIE0A): Enables or disables the channel 0 transfer end interrupt.

Bit 0

DTIE0A	Description	
0	Transfer end interrupt disabled	(Initial value)
1	Transfer end interrupt enabled	

DREQ Pin Falling Edge Activation Timing: Set the DTA bit for the channel for which the DREQ pin is selected to 1.

Figure 7.31 shows an example of DREQ pin falling edge activated single address mode transfer.

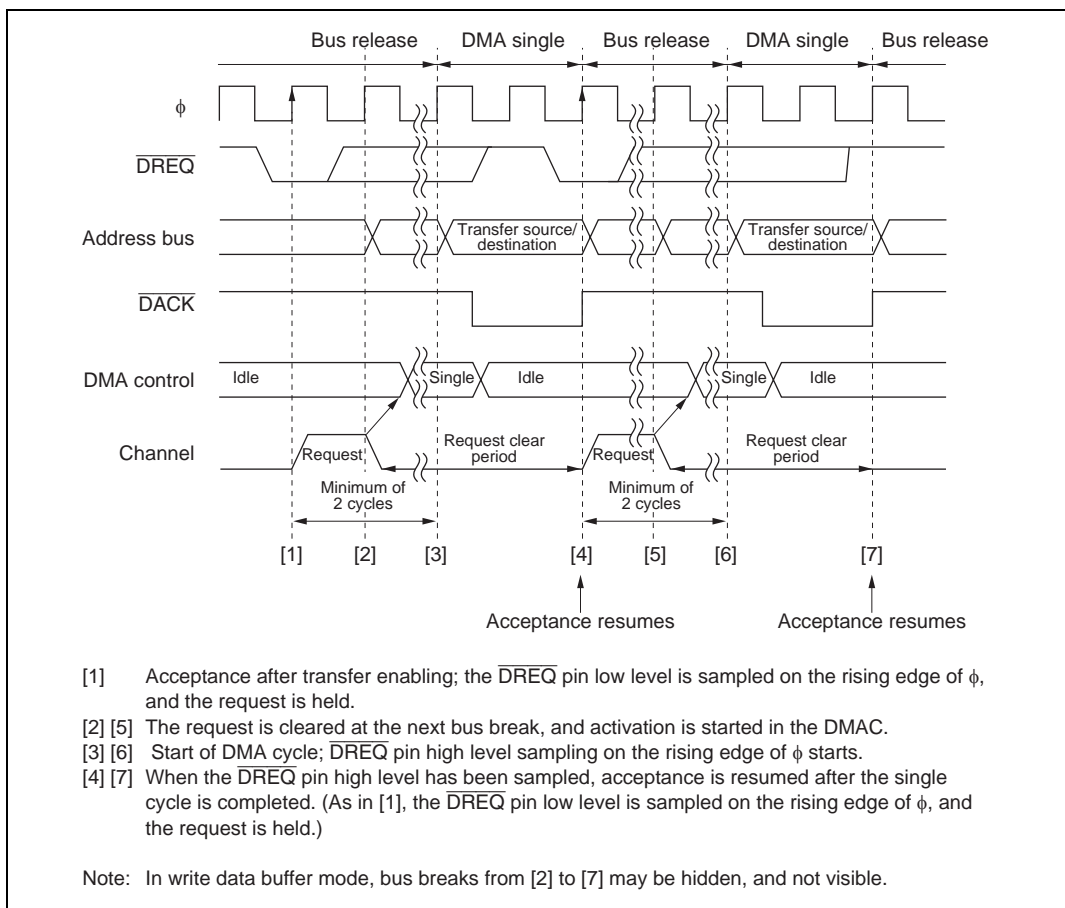


Figure 7.31 Example of DREQ Pin Falling Edge Activated Single Address Mode Transfer

DREQ pin sampling is performed every cycle, with the rising edge of the next ϕ cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the DREQ pin low level is sampled while acceptance by means of the DREQ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared, and DREQ pin high level sampling for edge detection is started. If DREQ pin high level sampling has been completed by the time the DMA single cycle ends, acceptance

- Free-running count operation and periodic count operation

Immediately after a reset, the TPU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, the TPU requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

Figure 10.7 illustrates free-running counter operation.

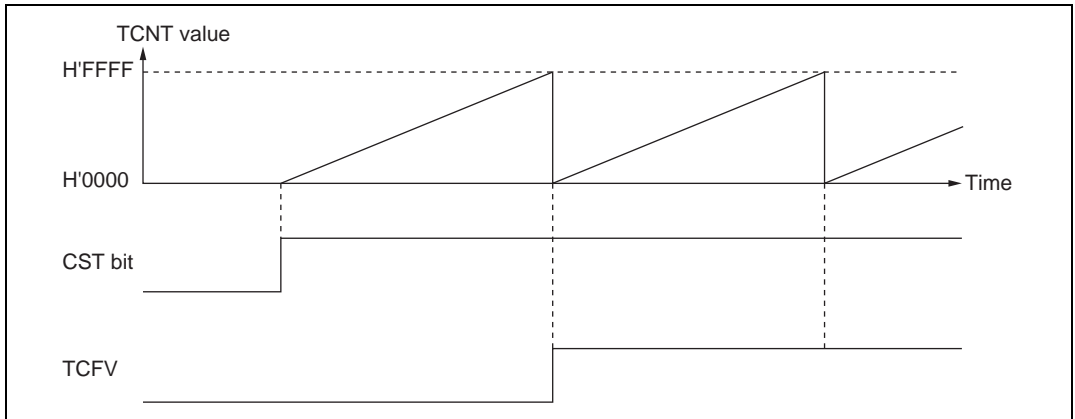


Figure 10.7 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR2 to CCLR0 in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTR is set to 1. When the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the TPU requests an interrupt. After a compare match, TCNT starts counting up again from H'0000.

Figure 10.8 illustrates periodic counter operation.

- Phase counting mode 4

Figure 10.32 shows an example of phase counting mode 4 operation, and table 10.12 summarizes the TCNT up/down-count conditions.

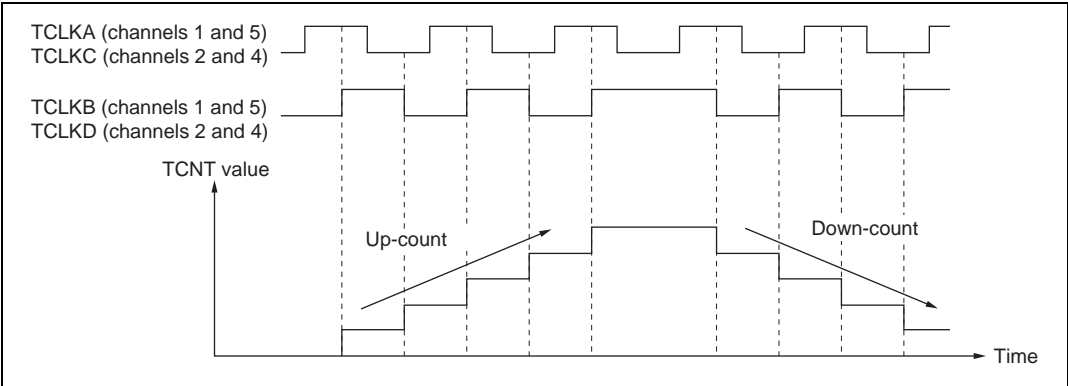


Figure 10.32 Example of Phase Counting Mode 4 Operation

Table 10.12 Up/Down-Count Conditions in Phase Counting Mode 4

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level		Up-count
Low level		Up-count
	Low level	Don't care
	High level	Don't care
High level		Down-count
Low level		Down-count
	High level	Don't care
	Low level	Don't care

Legend:

- : Rising edge
- : Falling edge

11.1.3 Pin Configuration

Table 11.1 summarizes the PPG pins.

Table 11.1 PPG Pins

Name	Symbol	I/O	Function
Pulse output 0	PO0	Output	Group 0 pulse output
Pulse output 1	PO1	Output	
Pulse output 2	PO2	Output	
Pulse output 3	PO3	Output	
Pulse output 4	PO4	Output	Group 1 pulse output
Pulse output 5	PO5	Output	
Pulse output 6	PO6	Output	
Pulse output 7	PO7	Output	
Pulse output 8	PO8	Output	Group 2 pulse output
Pulse output 9	PO9	Output	
Pulse output 10	PO10	Output	
Pulse output 11	PO11	Output	
Pulse output 12	PO12	Output	Group 3 pulse output
Pulse output 13	PO13	Output	
Pulse output 14	PO14	Output	
Pulse output 15	PO15	Output	

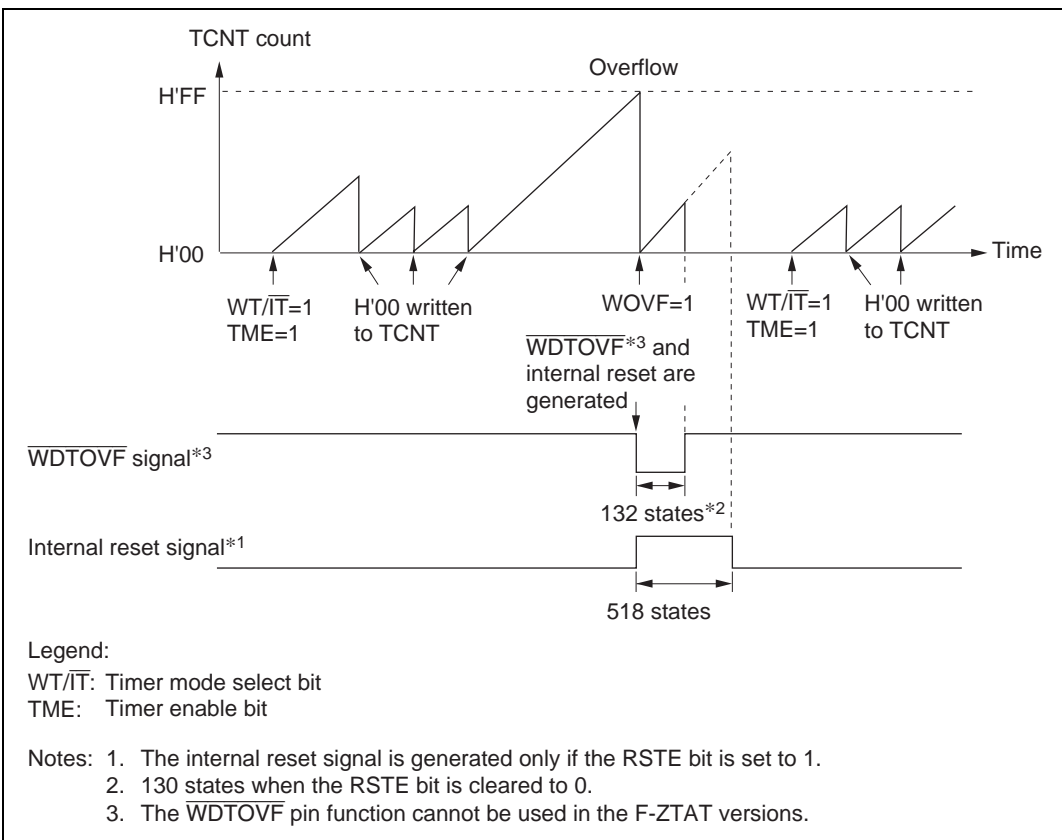


Figure 13.4 Operation in Watchdog Timer Mode

16.1.4 Register Configuration

Table 16.2 summarizes the registers of the A/D converter.

Table 16.2 A/D Converter Registers

Name	Abbreviation	R/W	Initial Value	Address ^{*1}
A/D data register AH	ADDRAH	R	H'00	H'FF90
A/D data register AL	ADDRAL	R	H'00	H'FF91
A/D data register BH	ADDRBH	R	H'00	H'FF92
A/D data register BL	ADDRBL	R	H'00	H'FF93
A/D data register CH	ADDRCH	R	H'00	H'FF94
A/D data register CL	ADDRCL	R	H'00	H'FF95
A/D data register DH	ADDRDH	R	H'00	H'FF96
A/D data register DL	ADDRDL	R	H'00	H'FF97
A/D control/status register	ADCSR	R/(W) ^{*2}	H'00	H'FF98
A/D control register	ADCR	R/W	H'3F	H'FF99
Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C

Notes: 1. Lower 16 bits of the address.

2. Bit 7 can only be written with 0 for flag clearing.

On-Chip RAM Area Divisions in Boot Mode: In boot mode, the 2-kbyte area from H'FFDC00 to H'FFE3FF is reserved for use by the boot program, as shown in figure 19.69. The area to which the programming control program is transferred is H'FFE400 to H'FFFBFF. The boot program area can be used when the programming control program transferred into RAM enters the execution state. A stack area should be set up as required.

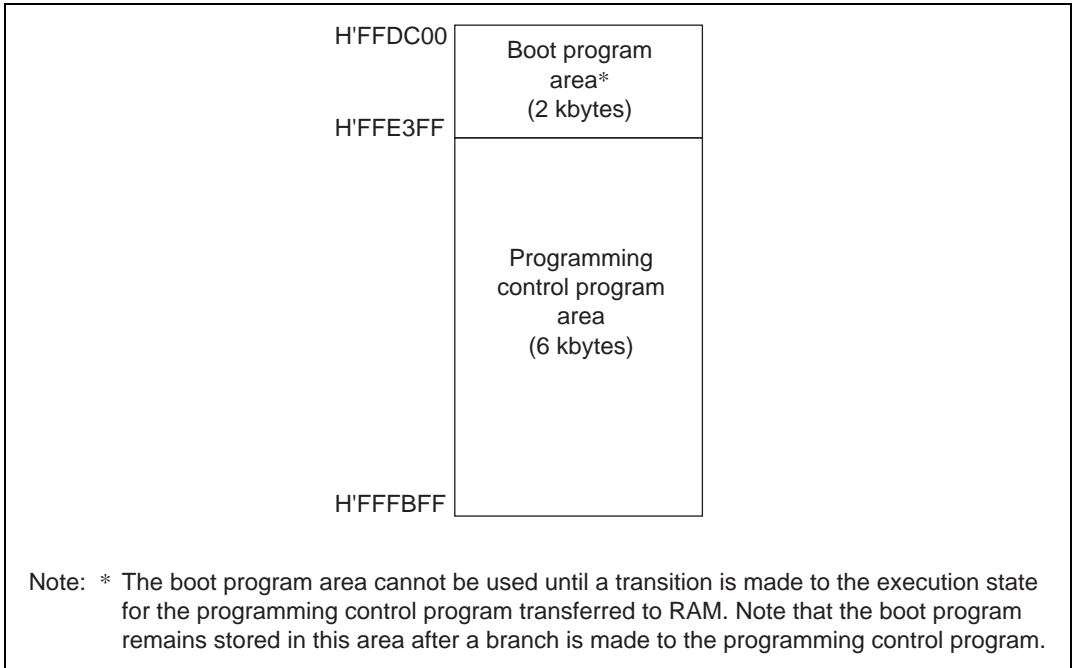


Figure 19.69 RAM Areas in Boot Mode

Notes on Use of Boot Mode

- When the chip comes out of reset in boot mode, it measures the low-level period of the input at the SCI's RxD1 pin. The reset should end with RxD1 high. After the reset ends, it takes approximately 100 states before the chip is ready to measure the low-level period of the RxD1 pin.
- In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.
- Interrupts cannot be used while the flash memory is being programmed or erased.

- The RxD1 and TxD1 pins should be pulled up on the board.
- Before branching to the programming control program (RAM area H'FFE400 to H'FFFBFF), the chip terminates transmit and receive operations by the on-chip SCI (channel 1) (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. The transmit data output pin, TxD1, goes to the high-level output state ($P31DDR = 1$, $P31DR = 1$).
- The contents of the CPU's internal general registers are undefined at this time, so these registers must be initialized immediately after branching to the programming control program. In particular, since the stack pointer (SP) is used implicitly in subroutine calls, etc., a stack area must be specified for use by the programming control program.
Initial settings must also be made for the other on-chip registers.
- Boot mode can be entered by making the pin settings shown in table 19.51 and executing a reset-start.
Boot mode can be cleared by driving the reset pin low, waiting at least 20 states, then setting the mode pins, and executing reset release^{*1}. Boot mode can also be cleared by a WDT overflow reset.
Do not change the mode pin input levels in boot mode. Do not make the FWE pin low level while a boot program is executing, or while programming or erasing flash memory^{*2}.
- If the mode pin input levels are changed (for example, from low to high) during a reset, the state of ports with multiplexed address functions and bus control output pins (\overline{AS} , \overline{RD} , \overline{HWR}) will change according to the change in the microcomputer's operating mode^{*3}.
Therefore, care must be taken to make pin settings to prevent these pins from becoming output signal pins during a reset, or to prevent collision with signals outside the microcomputer.

- Notes:
1. Input to the mode pins and FWE pin must satisfy the mode programming setup time ($t_{MDS} = 200 \text{ ns}$) requirement with regard to the reset release timing, as shown in figures 19.86 to 19.88.
 2. Refer to section 19.30, Flash Memory Programming and Erasing Precautions, for precautions regarding applying signals to and releasing the FWE pin.
 3. See section 9, I/O Ports.

		Mnemonic	Operand Size	Addressing Mode/ Instruction Length (Bytes)							Operation	Condition Code							No. of States ^{#1}	
				#xx	Rn	@ERn	@(d,ERn)	@-ERn/@ERn+	@aa	@(d,PC)		@@aa	I	H	N	Z	V	C	Advanced	Advanced
EXTS	EXTS.W Rd	W	2									—	—	↕	↕	0	—	1		
	EXTS.L ERd	L	2									—	—	↕	↕	0	—	1		
TAS	TAS @ERd ^{#3}	B		4								—	—	↕	↕	0	—	4		
MAC	MAC @ERn+, @ERm+	Cannot be used in the chip															[2]			
CLRMAC	CLRMAC																			
LDMAC	LDMAC ERs,MACH																			
	LDMAC ERs,MACL																			
STMAC	STMAC MACH,ERd																			
	STMAC MACL,ERd																			

Module	Register	Abbreviation	R/W	Initial Value	Address ^{*1}
TPU0	Timer control register 0	TCR0	R/W	H'00	H'FFD0
	Timer mode register 0	TMDR0	R/W	H'C0	H'FFD1
	Timer I/O control register 0H	TIOR0H	R/W	H'00	H'FFD2
	Timer I/O control register 0L	TIOR0L	R/W	H'00	H'FFD3
	Timer interrupt enable register 0	TIER0	R/W	H'40	H'FFD4
	Timer status register 0	TSR0	R/(W) ^{*2}	H'C0	H'FFD5
	Timer counter 0	TCNT0	R/W	H'0000	H'FFD6
	Timer general register 0A	TGR0A	R/W	H'FFFF	H'FFD8
	Timer general register 0B	TGR0B	R/W	H'FFFF	H'FFDA
	Timer general register 0C	TGR0C	R/W	H'FFFF	H'FFDC
	Timer general register 0D	TGR0D	R/W	H'FFFF	H'FFDE
TPU1	Timer control register 1	TCR1	R/W	H'00	H'FFE0
	Timer mode register 1	TMDR1	R/W	H'C0	H'FFE1
	Timer I/O control register 1	TIOR1	R/W	H'00	H'FFE2
	Timer interrupt enable register 1	TIER1	R/W	H'40	H'FFE4
	Timer status register 1	TSR1	R/(W) ^{*2}	H'C0	H'FFE5
	Timer counter 1	TCNT1	R/W	H'0000	H'FFE6
	Timer general register 1A	TGR1A	R/W	H'FFFF	H'FFE8
	Timer general register 1B	TGR1B	R/W	H'FFFF	H'FFEA
TPU2	Timer control register 2	TCR2	R/W	H'00	H'FFF0
	Timer mode register 2	TMDR2	R/W	H'C0	H'FFF1
	Timer I/O control register 2	TIOR2	R/W	H'00	H'FFF2
	Timer interrupt enable register 2	TIER2	R/W	H'40	H'FFF4
	Timer status register 2	TSR2	R/(W) ^{*2}	H'C0	H'FFF5
	Timer counter 2	TCNT2	R/W	H'0000	H'FFF6
	Timer general register 2A	TGR2A	R/W	H'FFFF	H'FFF8
	Timer general register 2B	TGR2B	R/W	H'FFFF	H'FFFA

C.3 Port 3

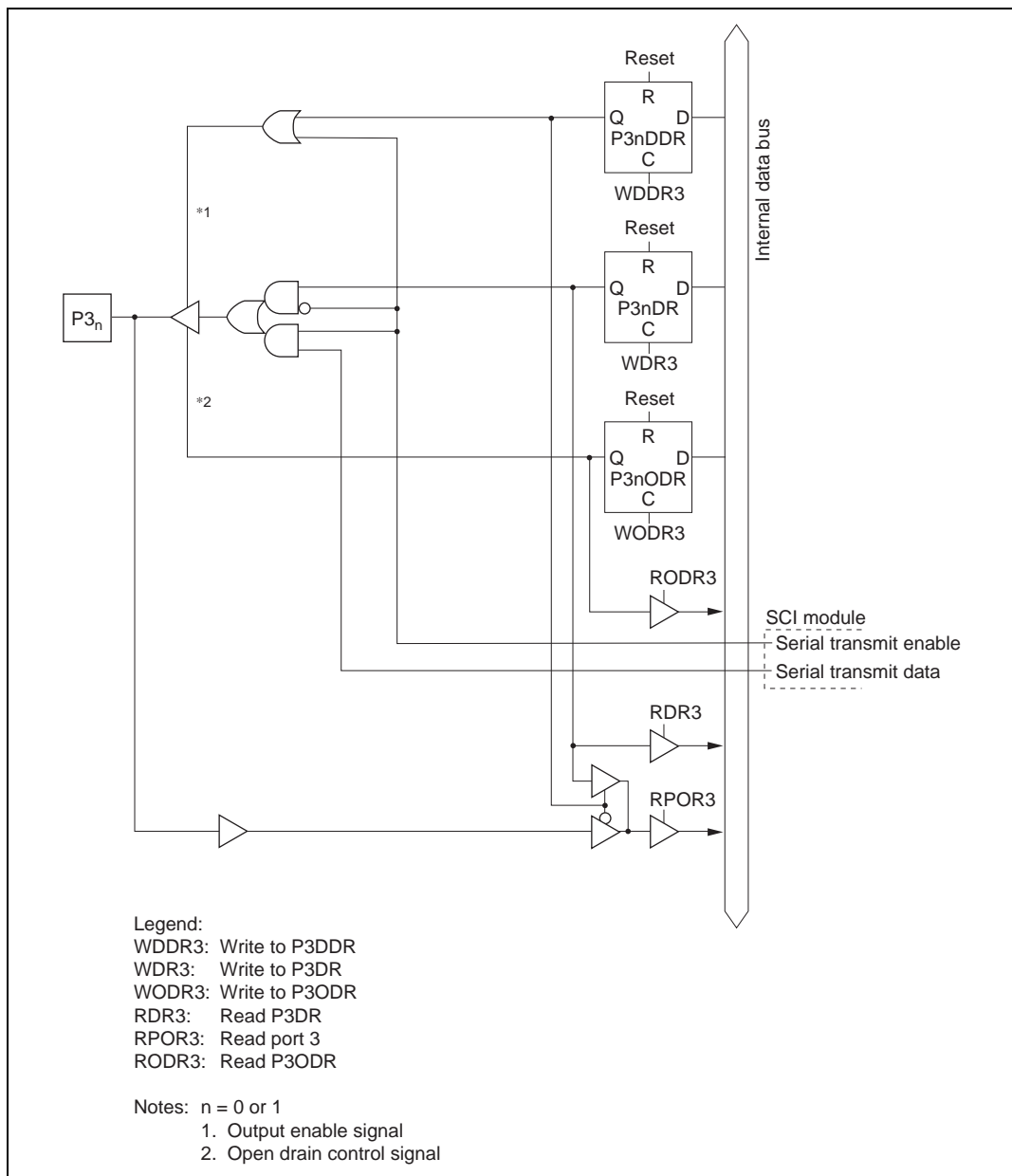


Figure C.3 (a) Port 3 Block Diagram (Pins P3₀ and P3₁)