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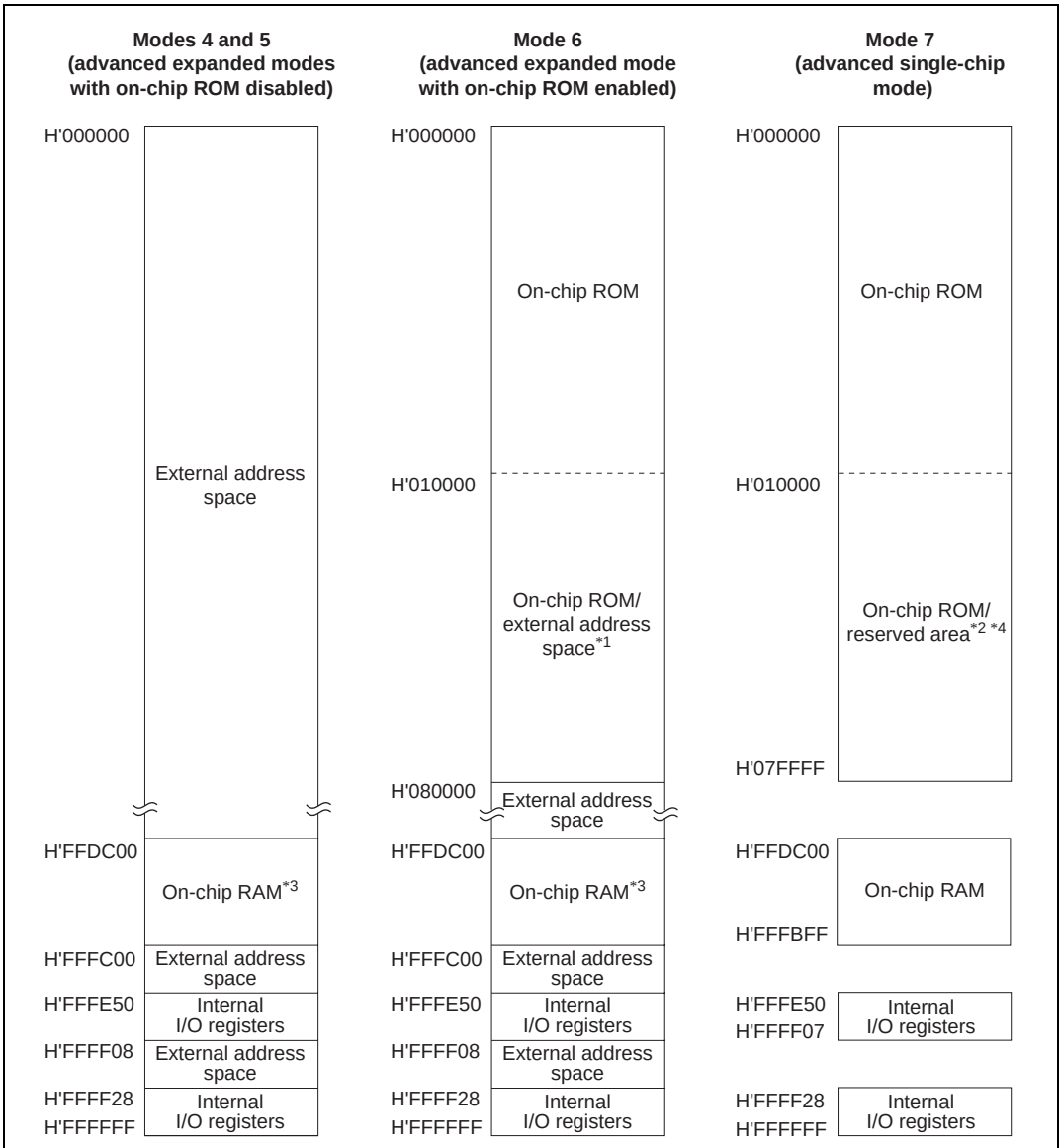
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2329evf25v

Type	Symbol	Pin No. TFP-120	Pin No. FP-128B	I/O	Name and Function
Bus control	$\overline{CAS}$*4	116	126	Output	**Upper column address strobe/ column address strobe:** The 2-CAS type DRAM upper column address strobe signal.
	$\overline{LCAS}$*4	86	94	Output	**Lower column address strobe:** The 2-CAS type DRAM lower column address strobe signal.
	$\overline{WAIT}$	86, 92	94, 102	Input	**Wait:** Requests insertion of a wait state in the bus cycle when accessing external 3-state access space.
DMA controller (DMAC) *3	$\overline{DREQ}_1$, $\overline{DREQ}_0$	62, 60	70, 66	Input	**DMA request 1 and 0:** These pins request DMAC activation.
	$\overline{TEND}_1$, $\overline{TEND}_0$	63, 61	71, 69	Output	**DMA transfer end 1 and 0:** These pins indicate the end of DMAC data transfer.
	$\overline{DACK}_1$, $\overline{DACK}_0$	111, 112	121, 122	Output	**DMA transfer acknowledge 1 and 0:** These are the DMAC single address transfer acknowledge pins.
16-bit timer pulse unit (TPU)	TCLKD to TCLKA	105, 107, 109, 110	115, 117, 119, 120	Input	**Clock input D to A:** These pins input an external clock.
	$TIOCA_0$, $TIOCB_0$, $TIOCC_0$, $TIOCD_0$	112 to 109	122 to 119	I/O	**Input capture/output compare match A0 to D0:** The TGR0A to TGR0D input capture input or output compare output, or PWM output pins.
	$TIOCA_1$, $TIOCB_1$	108, 107	118, 117	I/O	**Input capture/output compare match A1 and B1:** The TGR1A and TGR1B input capture input or output compare output, or PWM output pins.
	$TIOCA_2$, $TIOCB_2$	106, 105	116, 115	I/O	**Input capture/output compare match A2 and B2:** The TGR2A and TGR2B input capture input or output compare output, or PWM output pins.
	$TIOCA_3$, $TIOCB_3$, $TIOCC_3$, $TIOCD_3$	71 to 68	79 to 76	I/O	**Input capture/output compare match A3 to D3:** The TGR3A to TGR3D input capture input or output compare output, or PWM output pins.



Notes: 1. External addresses when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
2. Reserved area when EAE = 1 in BCRL; on-chip ROM when EAE = 0.
3. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
4. Do not access a reserved area.

Figure 3.4 (a) H8S/2326 F-ZTAT Memory Map in Each Operating Mode

6.5.8 Wait Control

There are two ways of inserting wait states in a DRAM access cycle: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Program Wait Insertion: When the bit in ASTCR corresponding to an area designated as DRAM space is set to 1, from 0 to 3 wait states can be inserted automatically between the T_{c1} state and T_{c2} state, according to the settings of WCRH and WCRL.

Pin Wait Insertion: When the WAITE bit in BCRH is set to 1, wait input by means of the $\overline{\text{WAIT}}$ pin is enabled regardless of the setting of the AST bit in ASTCR. When DRAM space is accessed in this state, a program wait is first inserted. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ϕ in the last T_{c1} or T_w state, another T_w state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted until it goes high.

Figure 6.17 shows an example of wait state insertion timing.

6.9 Write Data Buffer Function

The chip has a write data buffer function in the external data bus. Using the write data buffer function enables external writes and DMA single address mode transfers to be executed in parallel with internal accesses. The write data buffer function is made available by setting the WDBE bit in BCRL to 1.

Figure 6.36 shows an example of the timing when the write data buffer function is used. When this function is used, if an external write or DMA single address mode transfer* continues for 2 states or longer, and there is an internal access next, only an external write is executed in the first state, but from the next state onward an internal access (on-chip memory or internal I/O register read/write) is executed in parallel with the external write rather than waiting until it ends.

Note: * The DMAC is not supported in the H8S/2321.

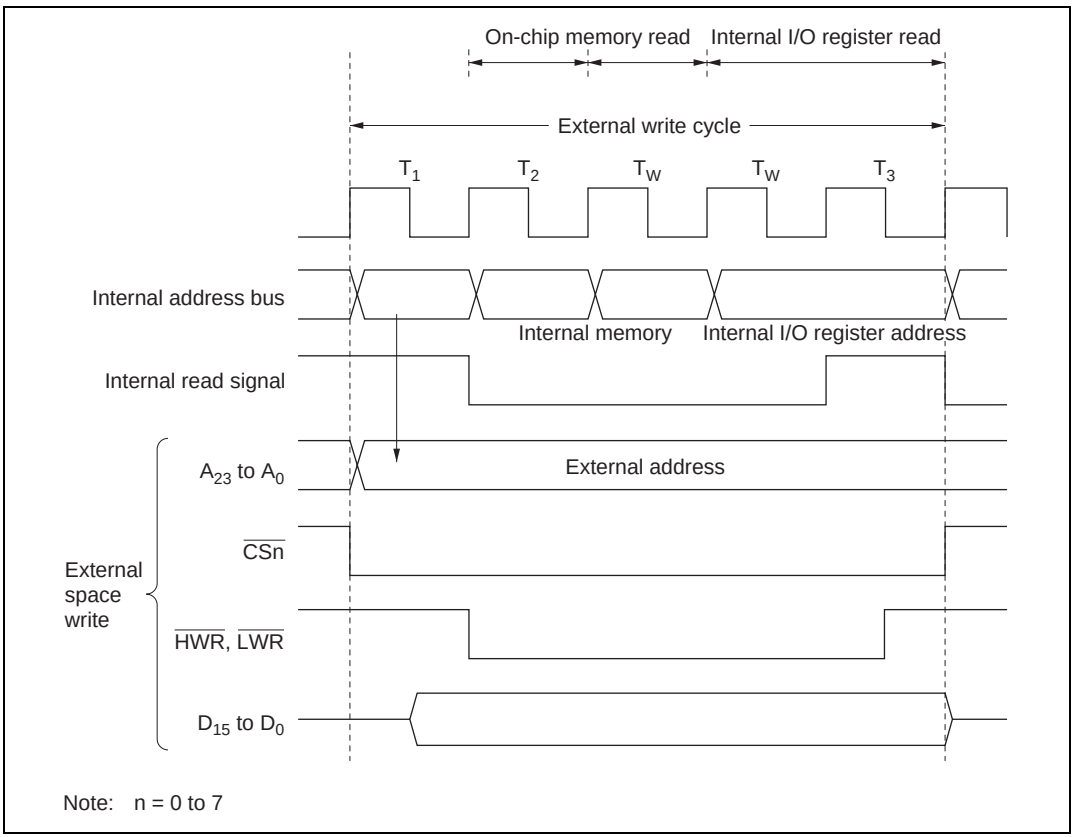


Figure 6.36 Example of Timing when Write Data Buffer Function is Used

Bit 7—DTC Chain Transfer Enable (CHNE): Specifies chain transfer. With chain transfer, a number of data transfers can be performed consecutively in response to a single transfer request.

In data transfer with CHNE set to 1, determination of the end of the specified number of transfers, clearing of the interrupt source flag, and clearing of DTCER are not performed.

When CHNE is set to 1, the chain transfer condition can be selected with the CHNS bit.

Bit 7 CHNE	Description
0	End of DTC data transfer (activation waiting state)
1	DTC chain transfer (new register information is read, then data is transferred)

Bit 6—DTC Interrupt Select (DISEL): Specifies whether interrupt requests to the CPU are disabled or enabled after a data transfer.

Bit 6 DISEL	Description
0	After a data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0 (the DTC clears the interrupt source flag of the activating interrupt to 0)
1	After a data transfer ends, the CPU interrupt is enabled (the DTC does not clear the interrupt source flag of the activating interrupt to 0)

Bit 5—DTC Chain Transfer Select (CHNS): Specifies the chain transfer condition when CHNE is 1.

Bit 7 CHNE	Bit 5 CHNS	Description
0	–	No chain transfer (DTC data transfer end, activation waiting state entered)
1	0	DTC chain transfer
1	1	Chain transfer only when transfer counter = 0

Bits 4 to 0—Reserved: These bits have no effect on DTC operation in the chip and should always be written with 0.

Port Function Control Register 2 (PFCR2)

Bit	:	7	6	5	4	3	2	1	0
		WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	:	0	0	1	1	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R	R	R

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'30 by a reset, and in hardware standby mode.

Bit 7—WAIT Pin Select (WAITPS): Selects the $\overline{\text{WAIT}}$ input pin. For details, see section 9.6, Port 5.

Bit 6—BREQO Pin Select (BREQOPS): Selects the $\overline{\text{BREQO}}$ output pin. For details, see section 9.6, Port 5.

Bit 5—CS167 Enable (CS167E): Enables or disables $\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output. Clear the DDR bits to 0 before changing the CS167E bit setting.

Bit 5 CS167E	Description	
0	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_1$, $\overline{\text{CS}}_6$, and $\overline{\text{CS}}_7$ output enabled	(Initial value)

Bit 4—CS25 Enable (CS25E): Enables or disables $\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output. Clear the DDR bits to 0 before changing the CS25E bit setting.

Bit 4 CS25E	Description	
0	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output disabled (can be used as I/O ports)	
1	$\overline{\text{CS}}_2$, $\overline{\text{CS}}_3$, $\overline{\text{CS}}_4$, and $\overline{\text{CS}}_5$ output enabled	(Initial value)

Bit 3—As Output Disable (ASOD): Enables or disables $\overline{\text{AS}}$ output. For details, see section 9.13, Port F.

Bits 2 to 0—Reserved: These bits are always read as 0.

9.11.3 Pin Functions

Modes 4 to 6: In modes 4 to 6, port D pins are automatically designated as data I/O pins.

Port D pin functions in modes 4 to 6 are shown in figure 9.17.

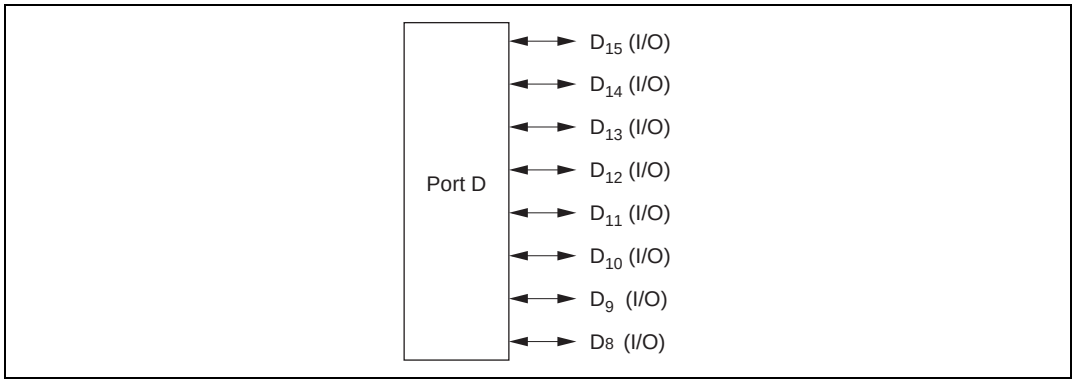


Figure 9.17 Port D Pin Functions (Modes 4 to 6)

Mode 7: In mode 7, port D pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting a PDDDR bit to 1 makes the corresponding port D pin an output port, while clearing the bit to 0 makes the pin an input port.

Port D pin functions in mode 7 are shown in figure 9.18.

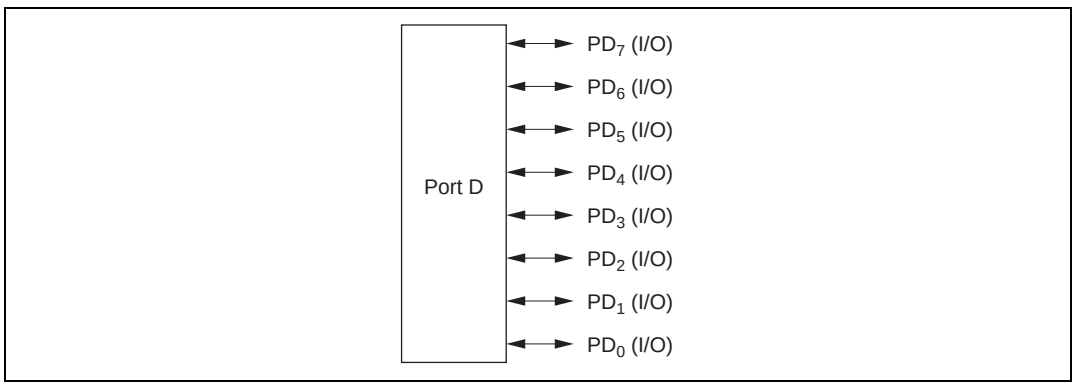


Figure 9.18 Port D Pin Functions (Mode 7)

- Example of input capture operation

  Figure 10.13 shows an example of input capture operation.

  In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

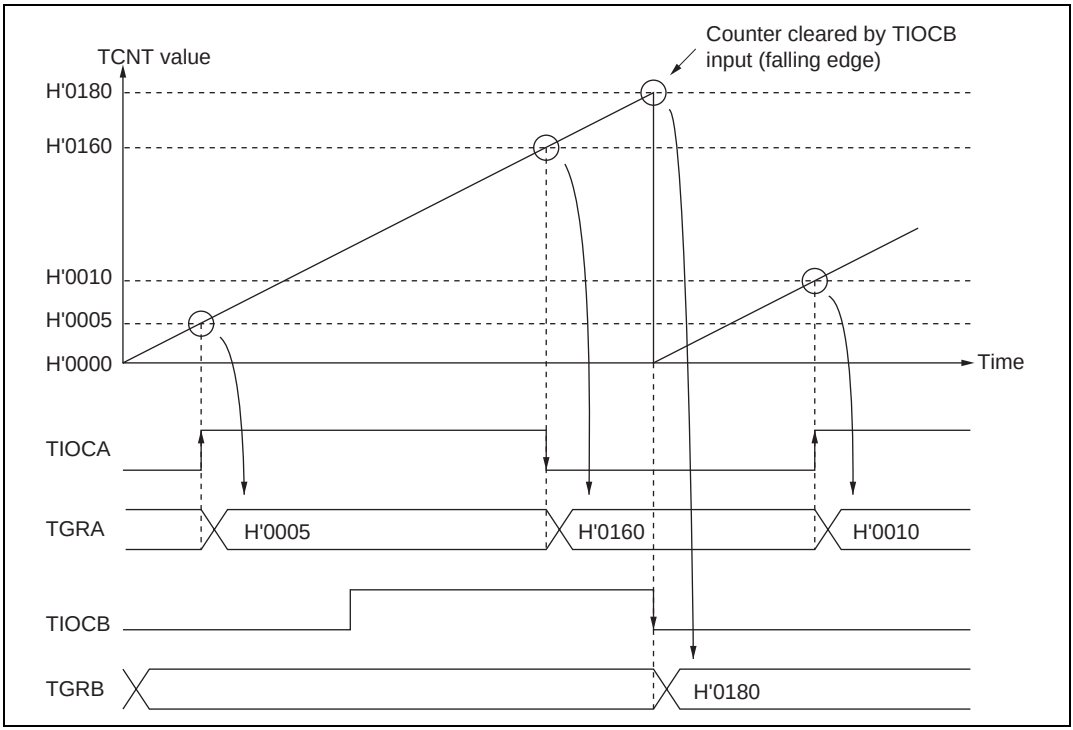


Figure 10.13 Example of Input Capture Operation

16.1.2 Block Diagram

Figure 16.1 shows a block diagram of the A/D converter.

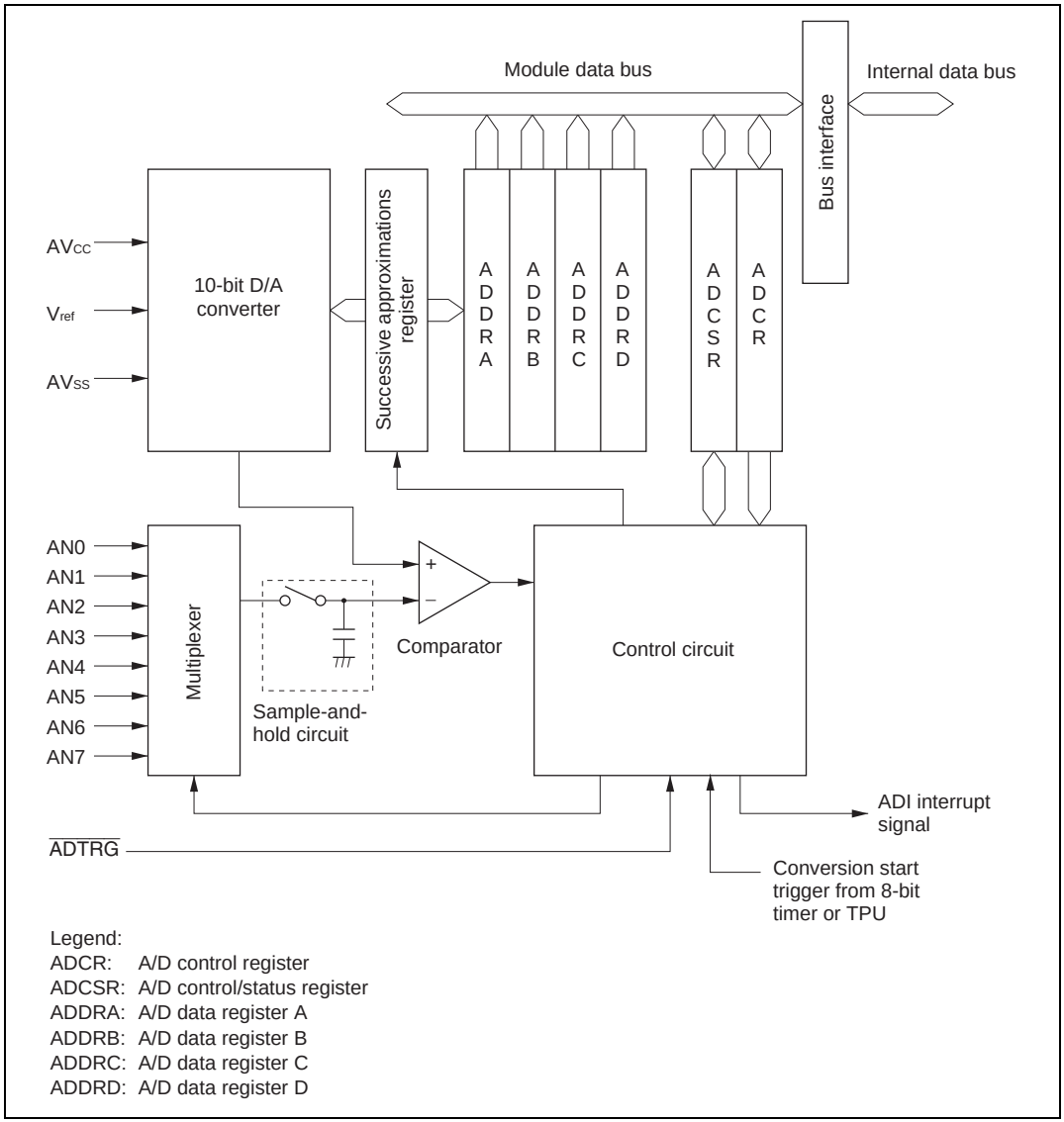


Figure 16.1 Block Diagram of A/D Converter

16.2 Register Descriptions

16.2.1 A/D Data Registers A to D (ADDRA to ADDRD)

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

There are four 16-bit read-only ADDR registers, ADDRA to ADDRD, used to store the results of A/D conversion.

The 10-bit data resulting from A/D conversion is transferred to the ADDR register for the selected channel and stored there. The upper 8 bits of the converted data are transferred to the upper byte (bits 15 to 8) of ADDR, and the lower 2 bits are transferred to the lower byte (bits 7 and 6) and stored. Bits 5 to 0 are always read as 0.

The correspondence between the analog input channels and ADDR registers is shown in table 16.3.

The ADDR registers can always be read by the CPU. The upper byte can be read directly, but for the lower byte, data transfer is performed via a temporary register (TEMP). For details, see section 16.3, Interface to Bus Master.

The ADDR registers are initialized to H'0000 by a reset, and in standby mode or module stop mode.

Table 16.3 Analog Input Channels and Corresponding ADDR Registers

Analog Input Channel		
Group 0	**Group 1**	**A/D Data Register**
AN0	AN4	ADDRA
AN1	AN5	ADDRB
AN2	AN6	ADDRC
AN3	AN7	ADDRD

Automatic SCI Bit Rate Adjustment: When boot mode is initiated, the H8S/2329B F-ZTAT chip measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The chip calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the chip's system clock frequency, there will be a discrepancy between the bit rates of the host and the chip. To ensure correct SCI operation, the host's transfer bit rate should be set to 9,600 or 19,200 bps.

Table 19.10 shows typical host transfer bit rates and system clock frequencies for which automatic adjustment of the MCU's bit rate is possible. The boot program should be executed within this system clock range.

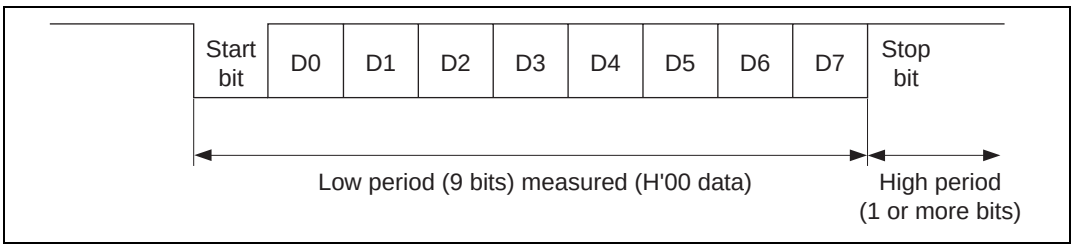


Figure 19.11 Automatic SCI Bit Rate Adjustment

Table 19.10 System Clock Frequencies for which Automatic Adjustment of H8S/2329B F-ZTAT Bit Rate is Possible

Host Bit Rate	System Clock Frequency for which Automatic Adjustment of H8S/2329B F-ZTAT Bit Rate is Possible
19,200 bps	16 MHz to 25 MHz
9,600 bps	8 MHz to 25 MHz

On-Chip RAM Area Divisions in Boot Mode: In boot mode, the 2-kbyte area from H'FF7C00 to H'FF83FF is reserved for use by the boot program, as shown in figure 19.12. The area to which the programming control program is transferred is H'FF8400 to H'FFFBFF. The boot program area can be used when the programming control program transferred into RAM enters the execution state. A stack area should be set up as required.

- PROM mode

  Flash memory can be programmed/erased in PROM mode, using a PROM programmer, as well as in on-board programming mode.

19.13.2 Overview

Block Diagram

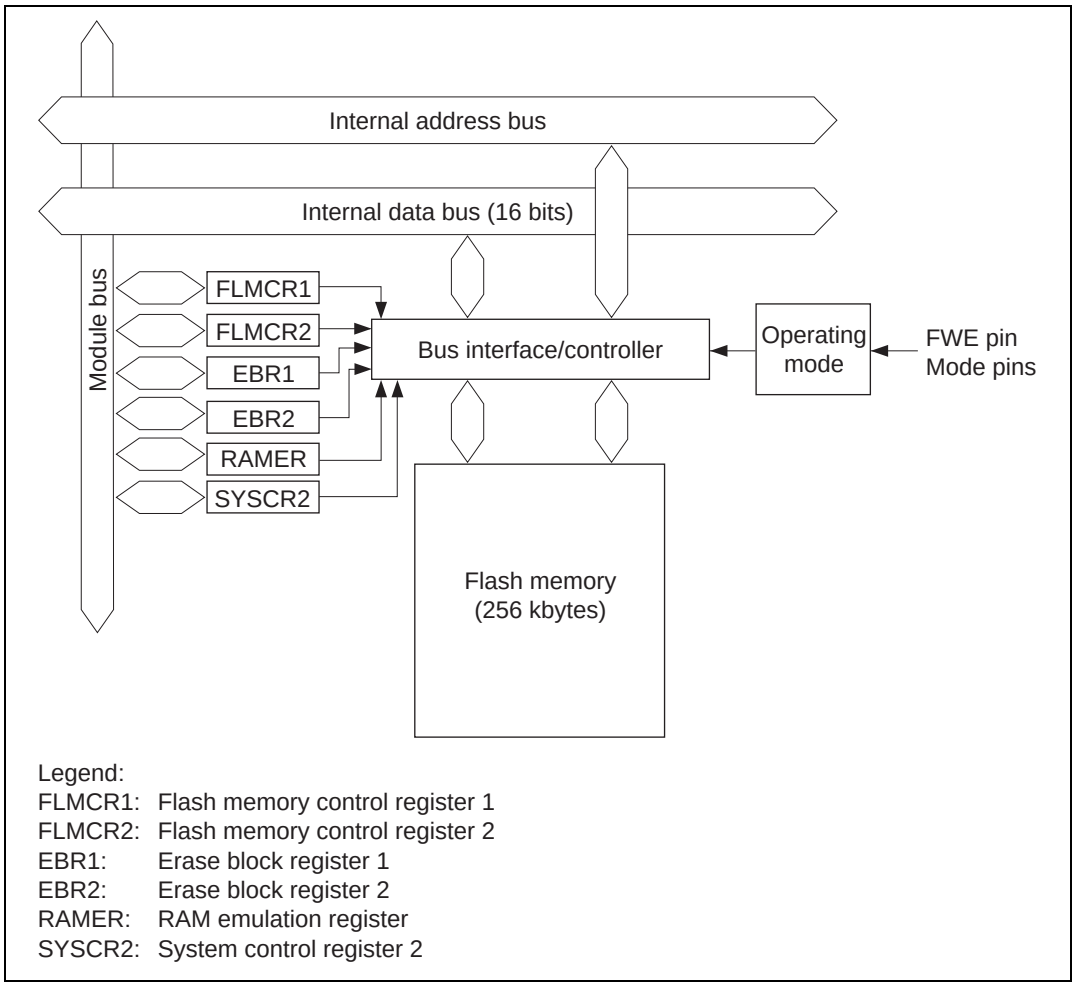


Figure 19.29 Block Diagram of Flash Memory

Bit 2—Program-Verify (PV): Selects program-verify mode transition or clearing. Do not set the SWE, ESU, PSU, EV, E, or P bit at the same time.

Bit 2 PV	Description	
0	Program-verify mode cleared	(Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE = 1	

Bit 1—Erase (E): Selects erase mode transition or clearing. Do not set the SWE, ESU, PSU, EV, PV, or P bit at the same time.

Bit 1 E	Description	
0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1	

Bit 0—Program (P): Selects program mode transition or clearing. Do not set the SWE, PSU, ESU, EV, PV, or E bit at the same time.

Bit 0 P	Description	
0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1	

Table 19.64 Status Read Mode Return Commands

Pin Name	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Attribute	Normal end identification	Command error	Program-ming error	Erase error	—	—	Program-ming or erase count exceeded	Effective address error
Initial value	0	0	0	0	0	0	0	0
Indications	Normal end: 0 Abnormal end: 1	Command error: 1 Otherwise: 0	Program-ming error: 1 Otherwise: 0	Erase error: 1 Otherwise: 0	—	—	Count exceeded: 1 Otherwise: 0	Effective address error: 1 Otherwise: 0

Note: I/O_3 and I/O_2 are undefined.

19.29.8 Status Polling

- The I/O_7 status polling flag indicates the operating status in auto-program or auto-erase mode.
- The I/O_6 status polling flag indicates a normal or abnormal end in auto-program or auto-erase mode.

Table 19.65 Status Polling Output Truth Table

Pin Names	Internal Operation in Progress	Abnormal End	—	Normal End
I/O_7	0	1	0	1
I/O_6	0	0	1	1
I/O_0 to I/O_5	0	0	0	0

19.29.9 PROM Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the PROM mode setup period. After the PROM mode setup time, a transition is made to memory read mode.

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)								Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa		I	H	N	Z	V	C	Advanced
MOV	MOV.L ERs,@ERd	L			4						ERs32→@ERd	—	—	↕	↕	0	—	4
	MOV.L ERs,@(d:16,ERd)	L				6					ERs32→@(d:16,ERd)	—	—	↕	↕	0	—	5
	MOV.L ERs,@(d:32,ERd)	L				10					ERs32→@(d:32,ERd)	—	—	↕	↕	0	—	7
	MOV.L ERs,@-ERd	L					4				ERd32-4→ERd32,ERs32→@ERd	—	—	↕	↕	0	—	5
	MOV.L ERs,@aa:16	L						6			ERs32→@aa:16	—	—	↕	↕	0	—	5
	MOV.L ERs,@aa:32	L						8			ERs32→@aa:32	—	—	↕	↕	0	—	6
POP	POP.W Rn	W								2	@SP→Rn16,SP+2→SP	—	—	↕	↕	0	—	3
	POP.L ERn	L								4	@SP→ERn32,SP+4→SP	—	—	↕	↕	0	—	5
PUSH	PUSH.W Rn	W								2	SP-2→SP,Rn16→@SP	—	—	↕	↕	0	—	3
	PUSH.L ERn	L								4	SP-4→SP,ERn32→@SP	—	—	↕	↕	0	—	5
LDM	LDM @SP+,(ERm-ERn)	L								4	(@SP→ERn32,SP+4→SP) Repeated for each register restored	—	—	—	—	—	—	7/9/11 [1]
STM	STM (ERm-ERn),@-SP	L								4	(SP-4→SP,ERn32→@SP) Repeated for each register saved	—	—	—	—	—	—	7/9/11 [1]
MOVFPE	MOVFPE @aa:16,Rd	Cannot be used in the chip																[2]
MOVTPE	MOVTPE Rs,@aa:16	Cannot be used in the chip																[2]

TIER4—Timer Interrupt Enable Register 4 H'FE94 TPU4

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

DMABCRH — DMA Band Control Register H'FF06 DMAC
(Not supported in H8S/2321)
DMABCRL — DMA Band Control Register H'FF07 DMAC
(Not supported in H8S/2321)

Full address mode

Bit :	15	14	13	12	11	10	9	8
DMABCRH :	FAE1	FAE0	—	—	DTA1	—	DTA0	—
Initial value :	0	0	0	0	0	0	0	0
Read/Write :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reserved
Only 0 should be written to this bit

Channel 0 Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Reserved
Only 0 should be written to this bit

Channel 1 Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Reserved
Only 0 should be written to these bits

Channel 0 Full Address Enable

0	Short address mode
1	Full address mode

Channel 1 Full Address Enable

0	Short address mode
1	Full address mode

(Continued on next page)

RDR0—Receive Data Register 0 **H'FF7D** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR0—Smart Card Mode Register 0 **H'FF7E** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Smart Card Data Invert

0	TDR contents are transmitted as they are Receive data is stored in RDR as it is
1	TDR contents are inverted before being transmitted Receive data is stored in RDR in inverted form

Smart Card Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

ADDRAH	**A/D Data Register AH**	**H'FF90**	**A/D Converter**
ADDRAL	**A/D Data Register AL**	**H'FF91**	**A/D Converter**
ADDRBH	**A/D Data Register BH**	**H'FF92**	**A/D Converter**
ADDRBL	**A/D Data Register BL**	**H'FF93**	**A/D Converter**
ADDRCH	**A/D Data Register CH**	**H'FF94**	**A/D Converter**
ADDRCL	**A/D Data Register CL**	**H'FF95**	**A/D Converter**
ADDRDH	**A/D Data Register DH**	**H'FF96**	**A/D Converter**
ADDRDL	**A/D Data Register DL**	**H'FF97**	**A/D Converter**

Bit	:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Stores the results of A/D conversion

Analog Input Channel		A/D Data Register
Group 0	Group 1	
AN0	AN4	ADDRA
AN1	AN5	ADDRB
AN2	AN6	ADDRC
AN3	AN7	ADDRD

PFCR2—Port Function Control Register 2 **H'FFAC** **Ports**

Bit	7	6	5	4	3	2	1	0
	WAITPS	BREQOPS	CS167E	CS25E	ASOD	—	—	—
Initial value	0	0	1	1	R/W	0	0	0
Read/Write	R/W	R/W	R/W	R/W		R	R	R

AS Output Disable

0	PF_6 is designated as $\overline{AS}$ output pin
1	PF_6 is designated as I/O port, and does not function as $\overline{AS}$ output pin

Note: This bit is valid in modes 4 to 6.

CS25 Enable

0	$\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$, and $\overline{CS}_5$ output disabled (can be used as I/O ports)
1	$\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$, and $\overline{CS}_5$ output enabled

Note: Clear the DDR bits to 0 before changing the CS25E setting.

CS167 Enable

0	$\overline{CS}_1$, $\overline{CS}_6$, and $\overline{CS}_7$ output disabled (can be used as I/O ports)
1	$\overline{CS}_1$, $\overline{CS}_6$, and $\overline{CS}_7$ output enabled

Note: Clear the DDR bits to 0 before changing the CS167E setting.

BREQO Pin Select

0	$\overline{BREQO}$ output is PF_2 pin
1	$\overline{BREQO}$ output is $P5_3$ pin

Note: Set BREQOPS before setting the BREQOE bit in BCRL to 1.

WAIT Pin Select

0	$\overline{WAIT}$ input is PF_2 pin
1	$\overline{WAIT}$ input is $P5_3$ pin

Note: Set WAITPS before setting the WAITE bit in BCRL to 1.