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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2329evte25v

2.4 Register Configuration

2.4.1 Overview

The CPU has the internal registers shown in figure 2.4. There are two types of registers: general registers and control registers.

General Registers (Rn) and Extended Registers (En)

	15	07	07	0
ER0	E0	R0H	R0L	
ER1	E1	R1H	R1L	
ER2	E2	R2H	R2L	
ER3	E3	R3H	R3L	
ER4	E4	R4H	R4L	
ER5	E5	R5H	R5L	
ER6	E6	R6H	R6L	
ER7 (SP)	E7	R7H	R7L	

Control Registers (CR)

23	0
PC	

	7	6	5	4	3	2	1	0
EXR	T	—	—	—	—	I2	I1	I0

	7	6	5	4	3	2	1	0
CCR	I	UI	H	U	N	Z	V	C

Legend:

SP:	Stack pointer	H:	Half-carry flag
PC:	Program counter	U:	User bit
EXR:	Extended control register	N:	Negative flag
T:	Trace bit	Z:	Zero flag
I2 to I0:	Interrupt mask bits	V:	Overflow flag
CCR:	Condition-code register	C:	Carry flag
I:	Interrupt mask bit		
UI:	User bit or interrupt mask bit*		

Note: * In the H8S/2329 Group and H8S/2328 Group, this bit cannot be used as an interrupt mask.

Figure 2.4 CPU Registers

The CPU's architecture allows for 4 Gbytes of address space, but the H8S/2328B F-ZTAT and H8S/2326 F-ZTAT actually accesses a maximum of 16 Mbytes.

Modes 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The external expansion modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Note that the functions of each pin depend on the operating mode.

Modes 10, 11, 14, and 15 are boot modes and user program modes in which the flash memory can be programmed and erased. For details, see section 19, ROM.

The H8S/2328B F-ZTAT and H8S/2326 F-ZTAT can only be used in modes 4 to 7, 10, 11, 14, and 15. This means that the flash write enable pin and mode pins must be set to select one of these modes.

Do not change the inputs at the mode pins during operation.

3.1.2 Operating Mode Selection (Mask ROM and ROMless Versions, H8S/2329B F-ZTAT)

The ROMless and mask ROM versions have four operating modes (modes 4 to 7). H8S/2329B F-ZTAT has six operating modes (modes 2 to 7). The operating mode is determined by the mode pins (MD_2 to MD_0). The CPU operating mode, enabling or disabling of on-chip ROM, and the initial bus width setting can be selected as shown in table 3.2.

Table 3.2 lists the MCU operating modes.

3.2.2 System Control Register (SYSCR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	INTM1	INTM0	NMIEG	LWROD	IRQPAS	RAME
Initial value	:	0	0	0	0	0	0	0	1
R/W	:	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7—Reserved: Only 0 should be written to this bit.

Bit 6—Reserved: This bit is always read as 0, and cannot be modified.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select the control mode of the interrupt controller. For details of the interrupt control modes, see section 5.4.1, Interrupt Control Modes and Interrupt Operation.

Bit 5 INTM1	Bit 4 INTM0	Interrupt Control Mode	Description	
0	0	0	Control of interrupts by I bit	(Initial value)
	1	—	Setting prohibited	
1	0	2	Control of interrupts by I2 to I0 bits and IPR	
	1	—	Setting prohibited	

Bit 3—NMI Edge Select (NMIEG): Selects the valid edge of the NMI interrupt input.

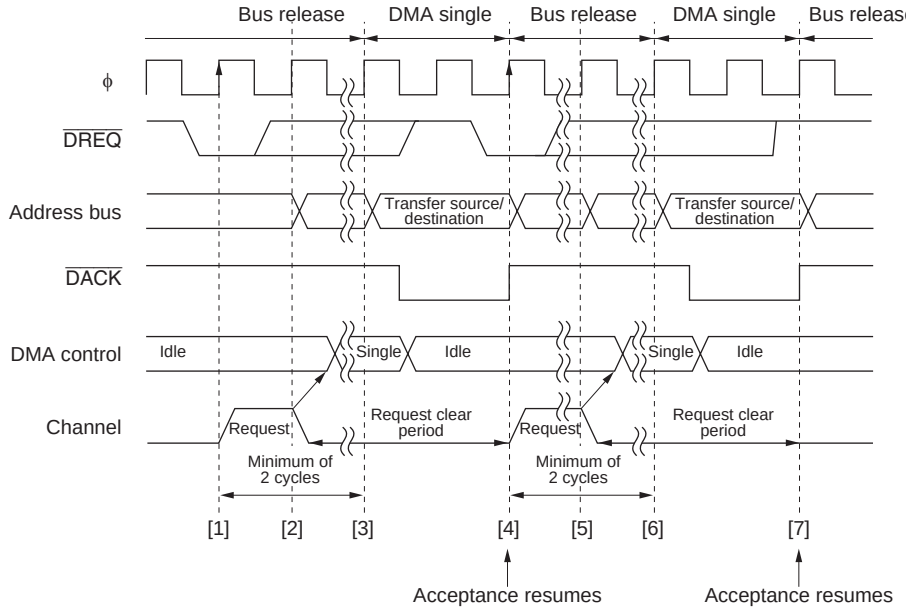
Bit 3 NMIEG	Description	
0	An interrupt is requested at the falling edge of NMI input	(Initial value)
1	An interrupt is requested at the rising edge of NMI input	

Bit 2—LWR Output Disable (LWROD): Enables or disables $\overline{\text{LWR}}$ output.

Bit 2 LWROD	Description	
0	PF_3 is designated as $\overline{\text{LWR}}$ output pin	(Initial value)
1	PF_3 is designated as I/O port, and does not function as $\overline{\text{LWR}}$ output pin	

$\overline{\text{DREQ}}$ Pin Falling Edge Activation Timing: Set the DTA bit for the channel for which the $\overline{\text{DREQ}}$ pin is selected to 1.

Figure 7.31 shows an example of $\overline{\text{DREQ}}$ pin falling edge activated single address mode transfer.



[1] Acceptance after transfer enabling; the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of φ, and the request is held.

[2] [5] The request is cleared at the next bus break, and activation is started in the DMAC.

[3] [6] Start of DMA cycle; $\overline{\text{DREQ}}$ pin high level sampling on the rising edge of φ starts.

[4] [7] When the $\overline{\text{DREQ}}$ pin high level has been sampled, acceptance is resumed after the single cycle is completed. (As in [1], the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of φ, and the request is held.)

Note: In write data buffer mode, bus breaks from [2] to [7] may be hidden, and not visible.

Figure 7.31 Example of $\overline{\text{DREQ}}$ Pin Falling Edge Activated Single Address Mode Transfer

$\overline{\text{DREQ}}$ pin sampling is performed every cycle, with the rising edge of the next φ cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the $\overline{\text{DREQ}}$ pin low level is sampled while acceptance by means of the $\overline{\text{DREQ}}$ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared, and $\overline{\text{DREQ}}$ pin high level sampling for edge detection is started. If $\overline{\text{DREQ}}$ pin high level sampling has been completed by the time the DMA single cycle ends, acceptance

Port A Data Register (PADR)

Bit	:	7	6	5	4	3	2	1	0
		PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PADR is an 8-bit readable/writable register that stores output data for the port A pins (PA_7 to PA_0).

PADR is initialized to H'00 by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Port A Register (PORTA)

Bit	:	7	6	5	4	3	2	1	0
		PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PA_7 to PA_0.

PORTA is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port A pins (PA_7 to PA_0) must always be performed on PADR.

If a port A read is performed while PADDR bits are set to 1, the PADR values are read. If a port A read is performed while PADDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTA contents are determined by the pin states, as PADDR and PADR are initialized. PORTA retains its prior state in software standby mode.

14.2.3 Transmit Shift Register (TSR)

Bit	:	7	6	5	4	3	2	1	0
R/W	:	—	—	—	—	—	—	—	—

TSR is a register used to transmit serial data.

To perform serial data transmission, the SCI first transfers transmit data from TDR to TSR, then sends the data to the TxD pin starting with the LSB (bit 0).

When transmission of one byte is completed, the next transmit data is transferred from TDR to TSR, and transmission started, automatically. However, data transfer from TDR to TSR is not performed if the TDRE bit in SSR is set to 1.

TSR cannot be directly read or written to by the CPU.

14.2.4 Transmit Data Register (TDR)

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TDR is an 8-bit register that stores data for serial transmission.

When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts serial transmission. Continuous serial transmission can be carried out by writing the next transmit data to TDR during serial transmission of the data in TSR.

TDR can be read or written to by the CPU at all times.

TDR is initialized to H'FF by a reset, and in standby mode or module stop mode.

15.3.4 Register Settings

Table 15.3 shows a bit map of the registers used by the smart card interface.

Bits indicated as 0 or 1 must be set to the value shown. The setting of other bits is described below.

Table 15.3 Smart Card Interface Register Settings

	Bit							
Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
SMR	GM	BLK	1	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
BRR	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
SCR	TIE	RIE	TE	RE	0	0	CKE1*	CKE0
TDR	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
SSR	TDRE	RDRF	ORER	ERS	PER	TEND	0	0
RDR	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
SCMR	—	—	—	—	SDIR	SINV	—	SMIF

Notes: — : Unused bit.

* The CKE1 bit must be cleared to 0 when the GM bit in SMR is cleared to 0.

SMR Settings: The GM bit is cleared to 0 in normal smart card interface mode, and set to 1 in GSM mode. The O/$\overline{E}$ bit is cleared to 0 if the IC card is of the direct convention type, and set to 1 if of the inverse convention type.

Bits CKS1 and CKS0 select the clock source of the built-in baud rate generator, and bits BCP1 and BCP0 select the number of base clock cycles during transfer of one bit. For details, see section 15.3.5, Clock.

The BLK bit is cleared to 0 when using the normal smart card interface mode, and set to 1 when using block transfer mode.

BRR Setting: BRR is used to set the bit rate. See section 15.3.5, Clock, for the method of calculating the value to be set.

SCR Settings: The function of the TIE, RIE, TE, and RE bits is the same as for the normal SCI. For details, see section 14, Serial Communication Interface (SCI).

Bits CKE1 and CKE0 specify the clock output. When the GM bit in SMR is cleared to 0, set these bits to B'00 if a clock is not to be output, or to B'01 if a clock is to be output. When the GM bit in SMR is set to 1, clock output is performed. The clock output can also be fixed high or low.

H8S/2329B F-ZTAT			Socket Adapter (40-Pin Conversion)	HN27C4096HG (40 Pins)	
TFP-120	FP-128B	Pin Name		Pin No.	Pin Name
2	6	A_0		21	A_0
3	7	A_1		22	A_1
4	8	A_2		23	A_2
5	9	A_3		24	A_3
7	11	A_4		25	A_4
8	12	A_5		26	A_5
9	13	A_6		27	A_6
10	14	A_7		28	A_7
11	15	A_8		29	A_8
12	16	A_9		31	A_9
13	17	A_{10}		32	A_{10}
14	18	A_{11}		33	A_{11}
16	20	A_{12}		34	A_{12}
17	21	A_{13}		35	A_{13}
18	22	A_{14}		36	A_{14}
19	23	A_{15}		37	A_{15}
20	24	A_{16}		38	A_{16}
21	25	A_{17}		39	A_{17}
22	26	A_{18}		10	A_{18}
43	49	D_8		19	I/O_0
44	50	D_9		18	I/O_1
45	51	D_{10}		17	I/O_2
46	52	D_{11}		16	I/O_3
48	54	D_{12}		15	I/O_4
49	55	D_{13}		14	I/O_5
50	56	D_{14}		13	I/O_6
51	57	D_{15}		12	I/O_7
68	76	$\overline{CE}$		2	$\overline{CE}$
69	77	$\overline{OE}$		20	$\overline{OE}$
67	75	$\overline{WE}$		3	$\overline{WE}$
72	80	EMLE*3		4	FWE
1, 30, 33, 52, 55,74, 75, 76, 81, 93, 94	5, 34, 39, 58, 61, 82, 83, 84, 89, 103, 104	V_{CC}		1, 40	V_{CC}
6, 15, 24, 31, 32, 38, 47, 59, 66, 79, 103, 104, 113, 114, 115	3, 10, 19, 28, 35, 36, 37, 38, 44, 53, 65, 67, 68, 74, 87, 99, 100, 113, 114, 123, 124, 125	V_{SS}		11, 30	V_{SS}
				5, 6, 7	NC
				8	A_{20}
				9	A_{19}
73	81	$\overline{RES}$	Reset circuit *1		
77	85	XTAL	Oscillation circuit *2		
78	86	EXTAL			
Other pins		NC (OPEN)			

Legend:
EMLE: Emulation enable
I/O_7 to I/O_0: Data input/output
A_{18} to A_0: Address input
$\overline{CE}$: Chip enable
$\overline{OE}$: Output enable
$\overline{WE}$: Write enable

Notes: 1. A reset oscillation stabilization time (t_{osc1}) of at least 10 ms is required.
2. A 12 MHz crystal resonator should be used.
3. As the FWE pin becomes VCC in the H8S/2329B F-ZTAT, the EMLE pin is ignored in PROM mode.

This figure shows pin assignments, and does not show the entire socket adapter circuit.

Figure 19.20 H8S/2329B F-ZTAT Socket Adapter Pin Assignments

Error protection is released only by a reset and in hardware standby mode.

Figure 19.43 shows the flash memory state transition diagram.

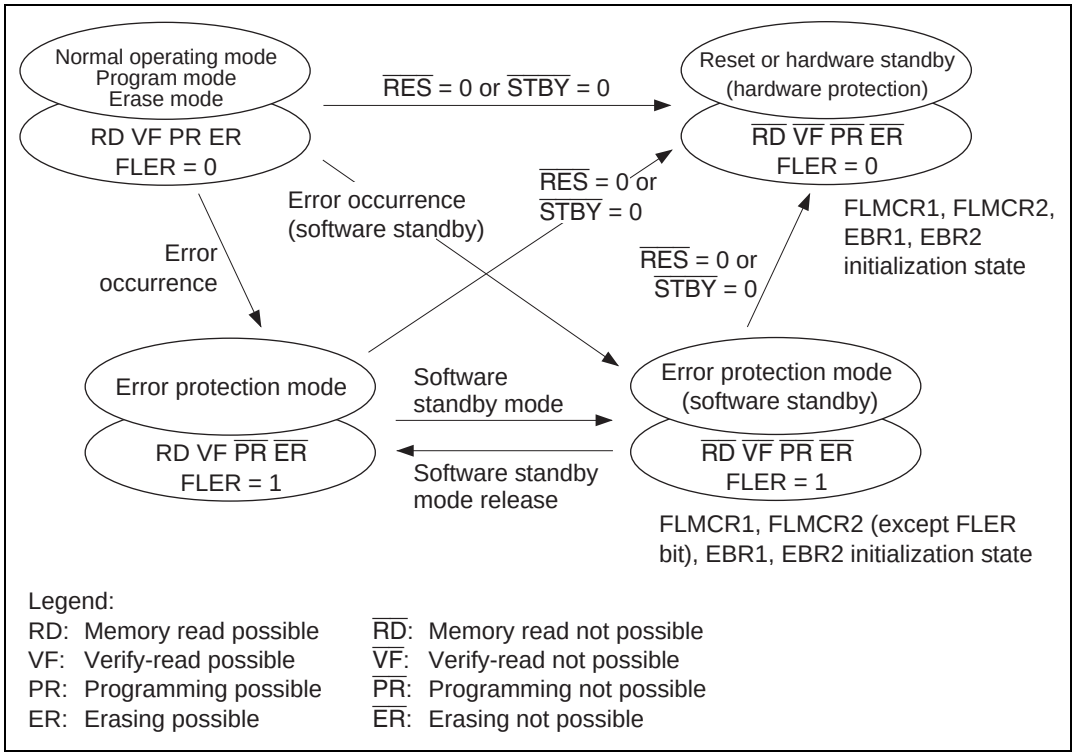
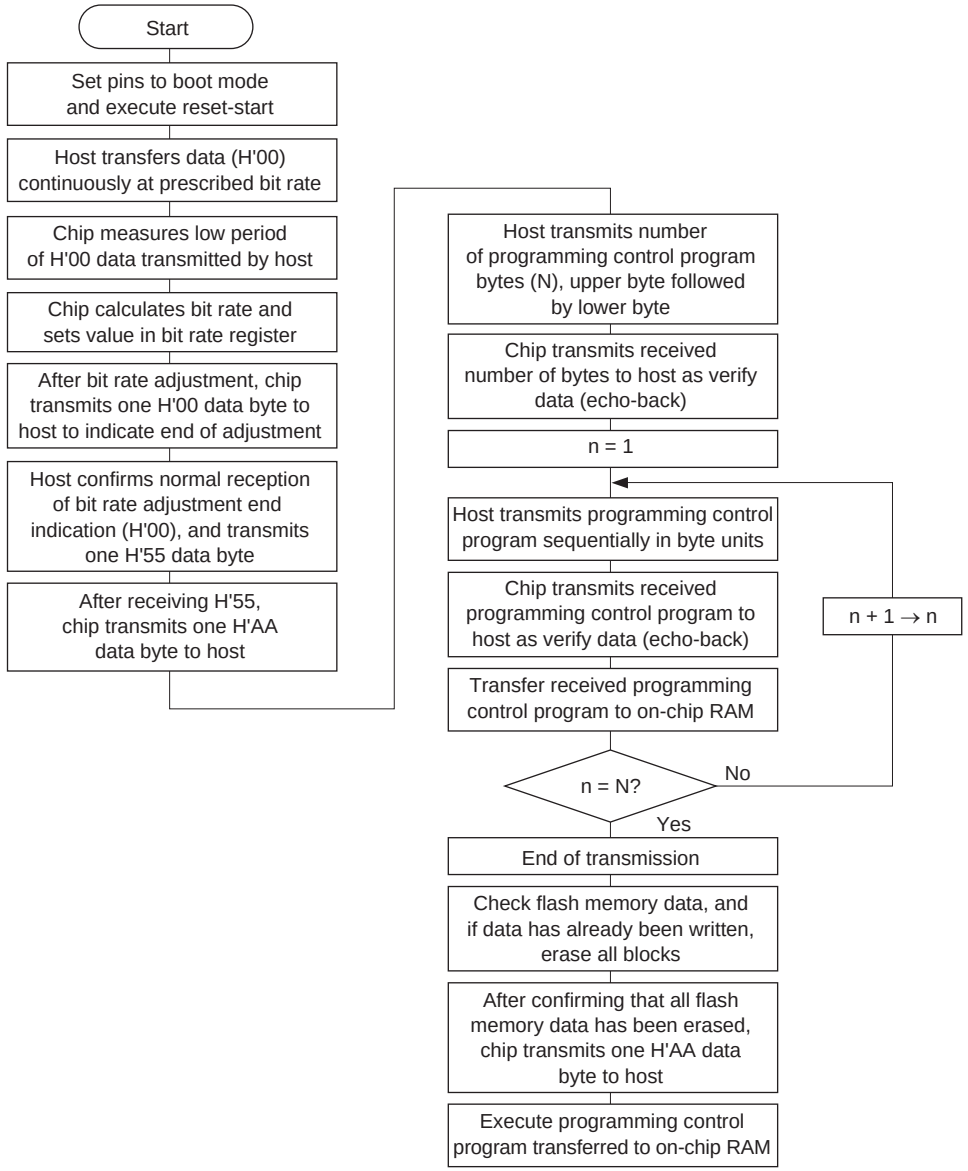


Figure 19.43 Flash Memory State Transitions



Note: If a memory cell does not operate normally and cannot be erased, one H'FF byte is transmitted as an erase error, and the erase operation and subsequent operations are halted.

Figure 19.67 Boot Mode Execution Procedure

19.27.2 RAM Overlap

An example in which flash memory block area EB1 is overlapped is shown below.

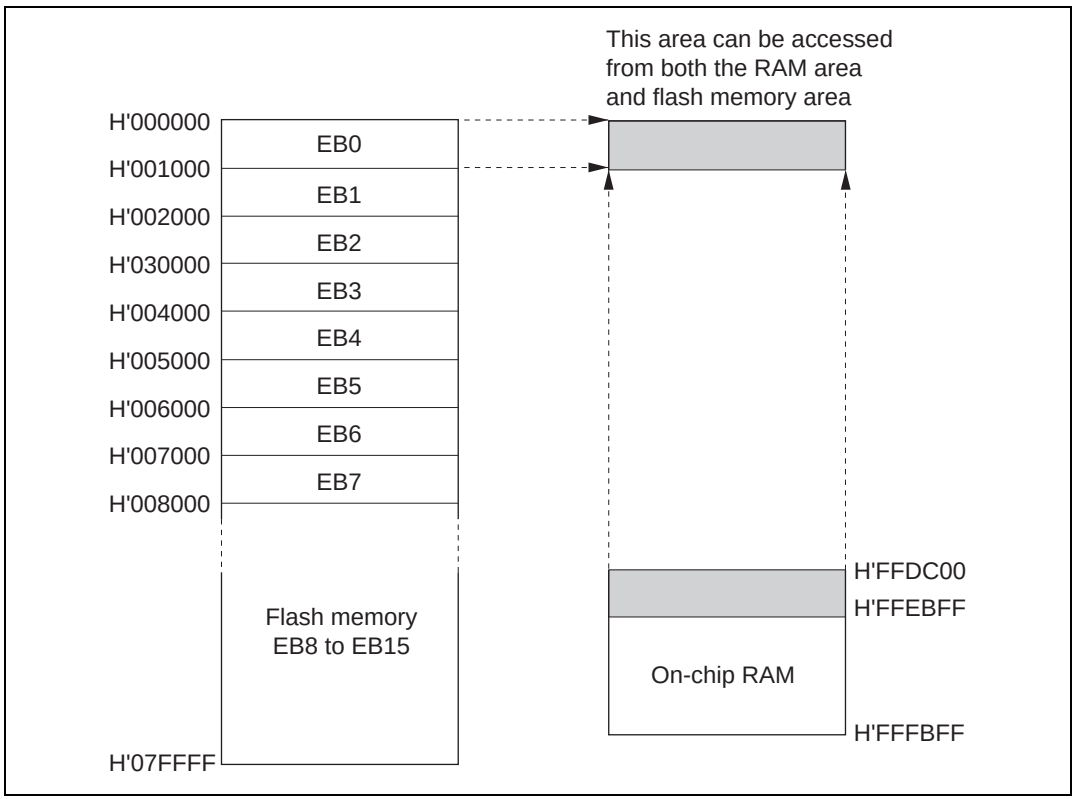


Figure 19.75 Example of RAM Overlap Operation

Example in which Flash Memory Block Area EB1 is Overlapped

1. Set bits RAMS, RAM2, RAM1, and RAM0 in RAMER to 1, 0, 0, 1, to overlap part of RAM onto the area (EB1) for which real-time programming is required.
2. Real-time programming is performed using the overlapping RAM.
3. After the program data has been confirmed, the RAMS bit is cleared, releasing RAM overlap.
4. The data written in the overlapping RAM is written into the flash memory space (EB1).

Notes: 1. When the RAMS bit is set to 1, program/erase protection is enabled for all blocks regardless of the value of RAM2, RAM1, and RAM0 (emulation protection). In this state, setting the P1 or E1 bit in flash memory control register 1 (FLMCR1), or setting

20.1.2 Register Configuration

The clock pulse generator is controlled by SCKCR. Table 20.1 shows the register configuration.

Table 20.1 Clock Pulse Generator Register

Name	Abbreviation	R/W	Initial Value	Address*
System clock control register	SCKCR	R/W	H'00	H'FF3A

Note: * Lower 16 bits of the address.

20.2 Register Descriptions

20.2.1 System Clock Control Register (SCKCR)

Bit	:	7	6	5	4	3	2	1	0
		PSTOP	—	DIV	—	—	SCK2	SCK1	SCK0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	—	—	R/W	R/W	R/W

SCKCR is an 8-bit readable/writable register that controls φ clock output, the medium-speed mode in which the bus master runs on a medium-speed clock and the other supporting modules run on the high-speed clock, and a function that allows the medium-speed mode to be disabled and the clock division ratio to be changed for the entire chip.

SCKCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—φ Clock Output Disable (PSTOP): Controls φ output.

	Description			
Bit 7 PSTOP	**Normal Operation**	**Sleep Mode**	**Software Standby Mode**	**Hardware Standby Mode**
0	φ output (Initial value)	φ output	Fixed high	High impedance
1	Fixed high	Fixed high	Fixed high	High impedance

Bit 6—Reserved: This bit can be read or written to, but only 0 should be written.

Table 22.3 DC Characteristics (H8S/2324S, H8S/2322R, H8S/2321, H8S/2320)

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $P6_4$ to $P6_7$	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
	PA_4 to PA_7	$V_T^+ - V_T^-$	$V_{CC} \times 0.06$	—	—	V	
	Port 5 (when using $\overline{IRQ}$)						
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Ports 3, 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		2.2	—	$V_{CC} + 0.3$	V	
	Port 4		2.2	—	AV_{CC} + 0.3V		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, Ports 3 to 5, B to G, $P6_0$ to $P6_3$, PA_0 to PA_3		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} – 0.5$	—	—	V	I_{OH} = –200 μA
			$V_{CC} – 1.0$	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	| I_{in} |	—	—	10.0	μA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2 to MD_0		—	—	1.0	μA	
	Port 4		—	—	1.0	μA	V_{in} = 0.5 V to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, 5, 6, A to G	| I_{TSI} |	—	—	1.0	μA	V_{in} = 0.5 V to V_{CC} – 0.5 V

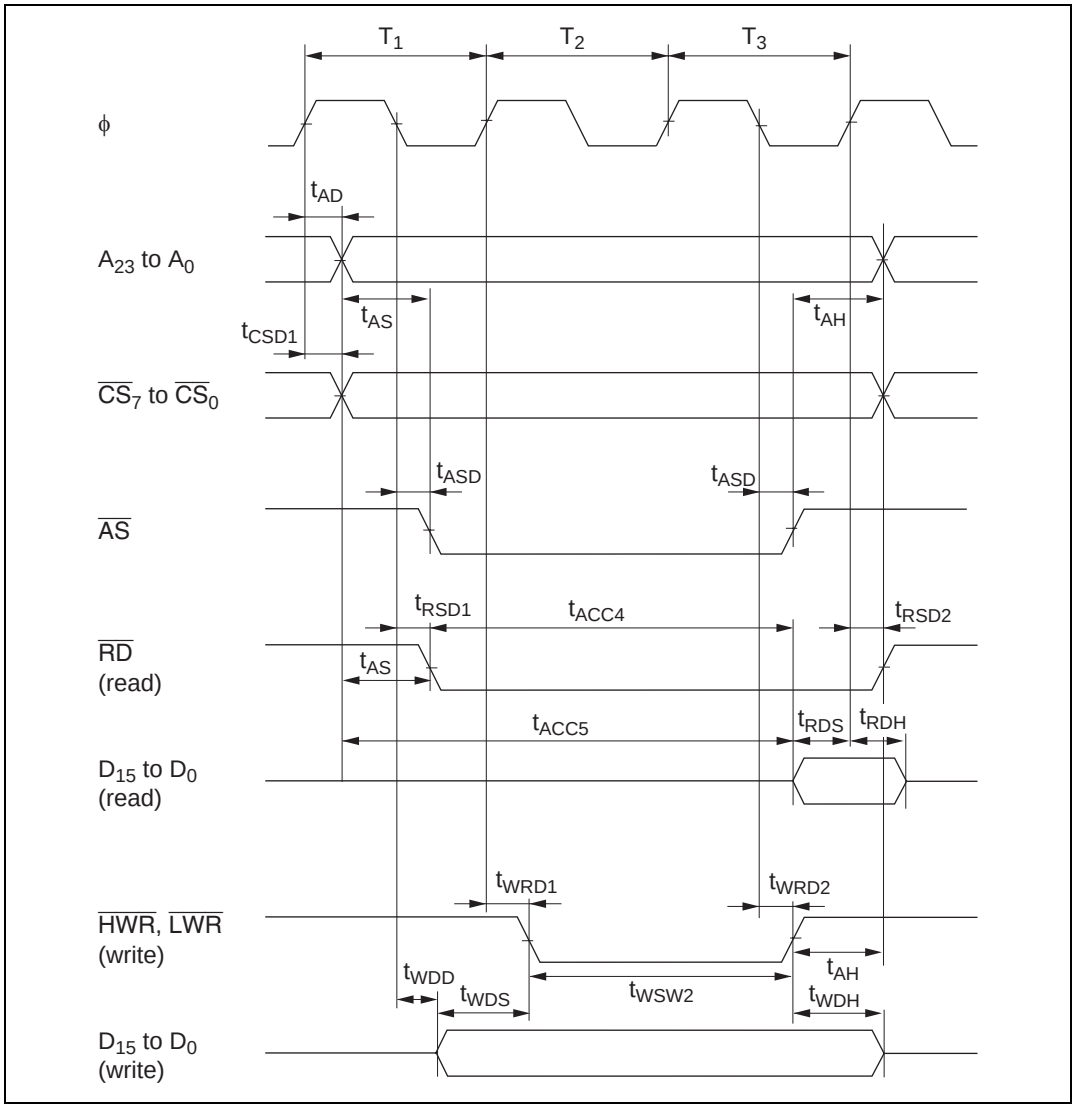


Figure 22.7 Basic Bus Timing (3-State Access)

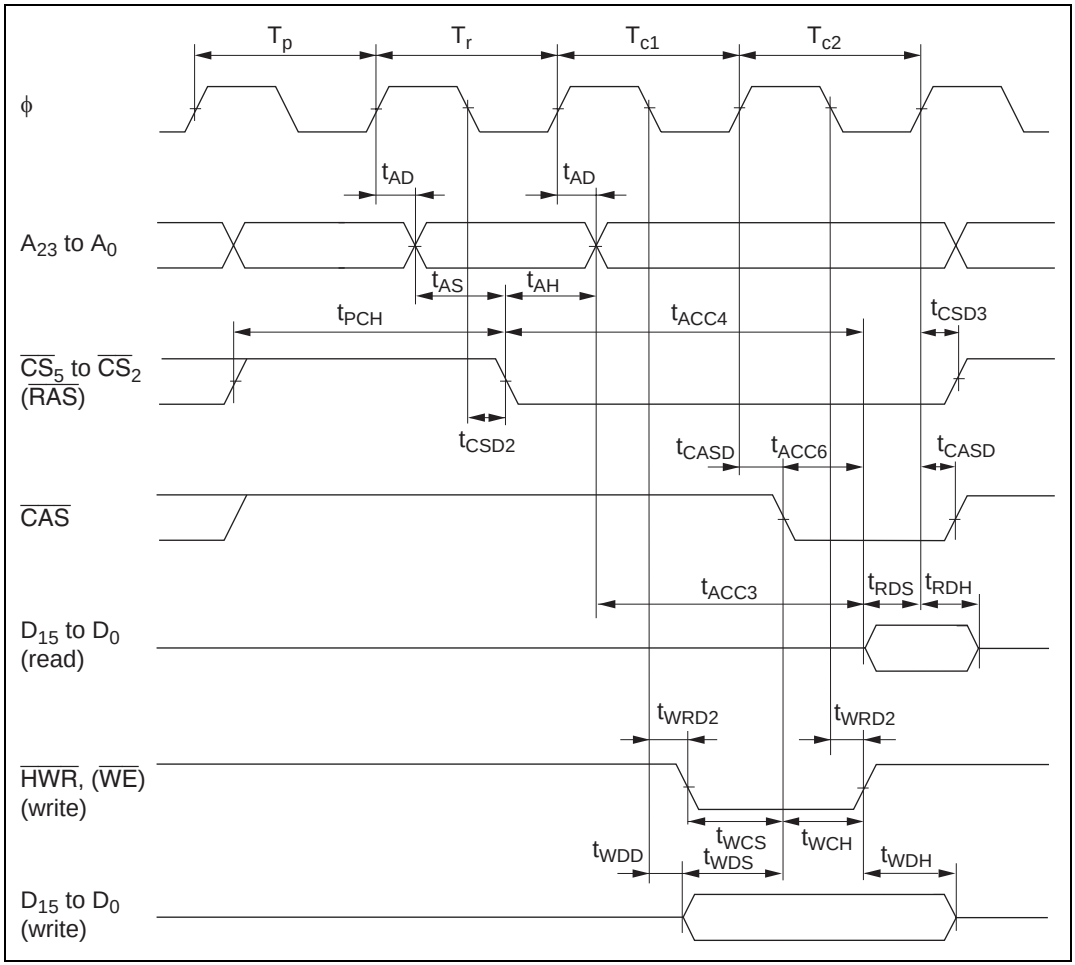


Figure 22.9 DRAM Bus Timing (Not Supported in the H8S/2321)

22.2.6 Flash Memory Characteristics

Table 22.22 Flash Memory Characteristics

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 0°C to +75°C (program/erase operating temperature range: regular specifications), T_a = 0°C to +85°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*1 *2 *4		t_P		—	10	200	ms/ 128 bytes	
Erase time*1 *3 *6		t_E		—	50	1000	ms/block	
Rewrite times		N_{WEC}		100*7	10000*8	—	Times	
Data hold time		t_{DRP}*9		10	—	—	year	
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after PSU bit setting*1	y		50	—	—	µs	
	Wait time after P bit setting*1 *4	z	(z1)	—	—	30	µs	1 ≤ n ≤ 6
			(z2)	—	—	200	µs	7 ≤ n ≤ 1000
			(z3)	—	—	10	µs	Wait time for additional writing
	Wait time after P bit clearing*1	α		5	—	—	µs	
	Wait time after PSU bit clearing*1	β		5	—	—	µs	
	Wait time after PV bit setting*1	γ		4	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after PV bit clearing*1	η		2	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of writes*1 *4	N		—	—	1000*5	Times	
Erasing	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after ESU bit setting*1	y		100	—	—	µs	
	Wait time after E bit setting*1 *6	z		—	—	10	ms	Wait time for erase time
	Wait time after E bit clearing*1	α		10	—	—	µs	
	Wait time after ESU bit clearing*1	β		10	—	—	µs	
	Wait time after EV bit setting*1	γ		20	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after EV bit clearing*1	η		4	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of erases*1 *6	N		—	—	100	Times	

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte	10th byte
BIST	BIST #xx:3,Rd	B	6	7	1	IMM rd														
	BIST #xx:3,@ERd	B	7	D	0	erd 0	6	7	1	IMM 0										
	BIST #xx:3,@aa:8	B	7	F	abs		6	7	1	IMM 0										
	BIST #xx:3,@aa:16	B	6	A	1	8	abs				6	7	1	IMM 0						
	BIST #xx:3,@aa:32	B	6	A	3	8	abs								6	7	1	IMM 0		
BIXOR	BIXOR #xx:3,Rd	B	7	5	1	IMM rd														
	BIXOR #xx:3,@ERd	B	7	C	0	erd 0	7	5	1	IMM 0										
	BIXOR #xx:3,@aa:8	B	7	E	abs		7	5	1	IMM 0										
	BIXOR #xx:3,@aa:16	B	6	A	1	0	abs				7	5	1	IMM 0						
	BIXOR #xx:3,@aa:32	B	6	A	3	0	abs								7	5	1	IMM 0		
BLD	BLD #xx:3,Rd	B	7	7	0	IMM rd														
	BLD #xx:3,@ERd	B	7	C	0	erd 0	7	7	0	IMM 0										
	BLD #xx:3,@aa:8	B	7	E	abs		7	7	0	IMM 0										
	BLD #xx:3,@aa:16	B	6	A	1	0	abs				7	7	0	IMM 0						
	BLD #xx:3,@aa:32	B	6	A	3	0	abs								7	7	0	IMM 0		
BNOT	BNOT #xx:3,Rd	B	7	1	0	IMM rd														
	BNOT #xx:3,@ERd	B	7	D	0	erd 0	7	1	0	IMM 0										
	BNOT #xx:3,@aa:8	B	7	F	abs		7	1	0	IMM 0										
	BNOT #xx:3,@aa:16	B	6	A	1	8	abs				7	1	0	IMM 0						
	BNOT #xx:3,@aa:32	B	6	A	3	8	abs								7	1	0	IMM 0		
	BNOT Rn,Rd	B	6	1	rn	rd														
	BNOT Rn,@ERd	B	7	D	0	erd 0	6	1	rn	0										
	BNOT Rn,@aa:8	B	7	F	abs		6	1	rn	0										
	BNOT Rn,@aa:16	B	6	A	1	8	abs				6	1	rn	0						
	BNOT Rn,@aa:32	B	6	A	3	8	abs								6	1	rn	0		

PFDDR—Port F Data Direction Register H'FEBE Port F

Bit	:	7	6	5	4	3	2	1	0
		PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 4 to 6									
Initial value	:	1	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W
Mode 7									
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	W	W	W	W	W	W	W	W

Specify input or output for individual port F pins

PGDDR—Port G Data Direction Register H'FEBF Port G

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 4 and 5									
Initial value	:	Undefined	Undefined	Undefined	1	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W
Modes 6 and 7									
Initial value	:	Undefined	Undefined	Undefined	0	0	0	0	0
Read/Write	:	—	—	—	W	W	W	W	W

Specify input or output for individual port G pins

MAR0AH—Memory Address Register 0AH **H'FEE0** **DMAC**
(Not supported in H8S/2321)

MAR0AL—Memory Address Register 0AL **H'FEE2** **DMAC**
(Not supported in H8S/2321)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR0AH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR0AL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Specifies transfer source address

IOAR0A—I/O Address Register 0A **H'FEE4** **DMAC**
(Not supported in H8S/2321)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR0A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

* : Undefined

In short address mode: Specifies transfer source/transfer destination address
In full address mode: Not used