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Applications of "Embedded - Microcontrollers"

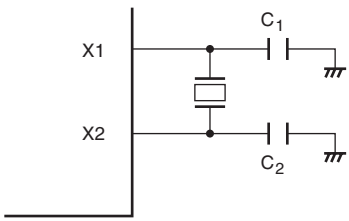
Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI, SSU
Peripherals	POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN
Supplier Device Package	32-VQFN (5x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38602rft10v

4.3 Subclock Oscillator

A subclock can be provided by connecting a crystal resonator or inputting an external clock. Either the subclock oscillator or on-chip oscillator can be selected, as shown in figure 4.1. For the selecting method, see section 4.3.4, On-Chip Oscillator Selection Method.

4.3.1 Connecting 32.768-kHz/38.4-kHz Crystal Resonator

Figure 4.5 shows an example of connecting a 32.768-kHz or 38.4-kHz crystal resonator. Notes described in section 4.5.2, Notes on Board Design also apply to this connection.



Frequency	Manufacturer	Products Name	Equivalent Series Resistance
38.4 kHz	EPSON TOYOCOM CORPORATION	C-4-TYPE	30 kΩ (max.)
32.768 kHz	EPSON TOYOCOM CORPORATION	C-001R	35 kΩ (max.)

$C_1 = C_2 = 7$ pF (typ.)

Note: Consult with the crystal resonator manufacturer to determine the parameters.

Figure 4.5 Typical Connection to 32.768-kHz/38.4-kHz Crystal Resonator

1. When the resonator other than ones listed above is used, perform matching evaluation with the crystal resonator manufacture and connect it under the optimum condition. Even when the resonator listed above or the equivalent is used, as the oscillation characteristics depend on the board specification, perform matching evaluation on the mounting board.
2. Perform matching evaluation in the reset state (the $\overline{\text{RES}}$ pin is low) and on exit from the reset state (the $\overline{\text{RES}}$ pin is driven from low to high).

3. Functions if ϕ_w, $\phi_w/4$, or $\phi_w/16$ is selected as an internal clock. Halted and retained otherwise.
4. Functions if the on-chip oscillator is selected. Halted and retained otherwise.
5. Functions if the on-chip oscillator is selected or if $\phi_w/16$ or $\phi_w/256$ is selected as an internal clock. Halted and retained otherwise.
6. Functions if the 32.768-kHz RTC is selected as an internal clock. Halted and retained otherwise.
7. Functions if ϕ_w is selected as an internal clock. Halted and retained otherwise.
8. Functions if $\phi_{SUB}/2$ is selected as an internal clock. Halted and retained otherwise.
9. Functions if $\phi_w/2$ is selected as an internal clock. Halted and retained otherwise.

5.2.1 Sleep Mode

In sleep mode, CPU operation is halted but the system clock oscillator, subclock oscillator, and on-chip peripheral modules function. In sleep (medium-speed) mode, the on-chip peripheral modules function at the clock frequency set by the MA1 and MA0 bits in SYSCR1. CPU register contents are retained.

Sleep mode is cleared by an interrupt. When an interrupt is requested, sleep mode is cleared and interrupt exception handling starts. Sleep mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable bit. After sleep mode is cleared, a transition is made from sleep (high-speed) mode to active (high-speed) mode or from sleep (medium-speed) mode to active (medium-speed) mode.

When the $\overline{\text{RES}}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared. Since an interrupt request signal is synchronous with the system clock, the maximum time of $2/\phi$ (s) may be delayed from the point at which an interrupt request signal occurs until the interrupt exception handling is started.

9.5 Timer B1 Operating Modes

Table 9.1 shows the timer B1 operating modes.

Table 9.1 Timer B1 Operating Modes

	Active		Sleep						Oscillation Stabilization Time		
Clock Source	High-speed	Medium-speed	High-speed	Medium-speed	Watch	Sub-active	Sub-sleep	Standby	Standby to Active	Subsleep to Active	Watch to Active
φw/256, φw/1024	o	o	o	o	o	o	o	×	×	o	o
φ/4, φ/16, φ/64, φ/256, φ/2048, φ/8192	o	o	o	o	×	×	×	×	×	×	×

[Legend] o: Counting enabled
×: Counting disabled (Counter value retained)

11.3.4 Day-of-Week Data Register (RWKDR)

RWKDR counts the BCD-coded day-of-week value on the carry generated once per day by RHRDR. The setting range is decimal 0 to 6 using bits WK2 to WK0.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—/(0)*	R	RTC Busy This bit is set to 1 when the RTC is updating (operating) the values of second, minute, hour, and day-of-week data registers. When this bit is 0, the values of second, minute, hour, and day-of-week data registers must be adopted.
6 to 3	—	All 0	—	Reserved These bits are always read as 0.
2	WK2	—/(0)*	R/W	Day-of-Week Counting
1	WK1	—/(0)*	R/W	Day-of-week is indicated with a binary code
0	WK0	—/(0)*	R/W	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday 111: Reserved (setting prohibited)

Note: * Initial value after a reset caused by the RST bit in RTCCR1.

11.3.7 Clock Source Select Register (RTCCSR)

RTCCSR selects clock source. A free running counter controls start/stop of counter operation by the RUN bit in RTCCR1. When a clock other than $\phi_w/4$ is selected, the RTC is disabled and operates as an 8-bit free running counter. When the RTC operates as an 8-bit free running counter, RSECDR enables counter values to be read. An interrupt can be generated by setting 1 to the FOIE bit in RTCCR2 and enabling an overflow interrupt of the free running counter. A clock generated by dividing the system clock by 32, 16, 8, or 4 is output in active or sleep mode. ϕ_w is output in active, sleep, subactive, subsleep, or watch mode.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	Select a clock output from the TMOW pin when enabling TMOW output in PMR1.
4	SUB32K	0	R/W	000: $\phi/4$ 010: $\phi/8$ 100: $\phi/16$ 110: $\phi/32$ xx1: ϕ_w
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: $\phi/8$ ····· Free running counter operation
1	RCS1	0	R/W	0001: $\phi/32$ ····· Free running counter operation
0	RCS0	0	R/W	0010: $\phi/128$ ····· Free running counter operation 0011: $\phi/256$ ····· Free running counter operation 0100: $\phi/512$ ····· Free running counter operation 0101: $\phi/2048$ ····· Free running counter operation 0110: $\phi/4096$ ····· Free running counter operation 0111: $\phi/8192$ ····· Free running counter operation 1000: $\phi_w/4$ ····· RTC operation 1001 to 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
1	CKE1	0	R/W	Clock Enable 0 and 1
0	CKE0	0	R/W	Select the clock source. Asynchronous mode: 00: Internal baud rate generator (SCK3 pin functions as an I/O port) 01: Internal baud rate generator (Outputs a clock of the same frequency as the bit rate from the SCK3 pin) 10: External clock (Inputs a clock with a frequency 16 times the bit rate from the SCK3 pin) 11: Reserved Clock synchronous mode: 00: Internal clock (SCK3 pin functions as clock output) 01: Reserved 10: External clock (SCK3 pin functions as clock input) 11: Reserved

Table 14.6 BRR Settings for Various Bit Rates (Clock Synchronous Mode) (1)

ϕ	32.8 kHz			38.4 kHz			2 MHz		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
200	0	40	0.00	0	47	0.00	2	155	0.16
250	0	32	–0.61	0	37	1.05	2	124	0.00
300	0	26	1.23	0	31	0.00	2	103	0.16
500	0	15	2.50	0	18	1.05	2	62	–0.79
1k	0	7	2.50	—	—	—	2	30	0.81
2.5k	—	—	—	—	—	—	0	199	0.00
5k	—	—	—	—	—	—	0	99	0.00
10k	—	—	—	—	—	—	0	49	0.00
25k	—	—	—	—	—	—	0	19	0.00
50k	—	—	—	—	—	—	0	9	0.00
100k	—	—	—	—	—	—	0	4	0.00
250k	—	—	—	—	—	—	0	1	0.00
500k	—	—	—	—	—	—	0*	0*	0.00*
1M	—	—	—	—	—	—	—	—	—

Note: * Continuous transmission/reception is not possible.

14.7 Interrupt Requests

The SCI3 creates the following six interrupt requests: transmit end, transmit data empty, receive data full, and receive errors (overrun error, framing error, and parity error). Table 14.13 shows the interrupt sources.

Table 14.13 SCI3 Interrupt Requests

Interrupt Requests	Abbreviation	Interrupt Sources
Receive Data Full	RXI	Setting RDRF in SSR
Transmit Data Empty	TXI	Setting TDRE in SSR
Transmission End	TEI	Setting TEND in SSR
Receive Error	ERI	Setting OER, FER, and PER in SSR

Each interrupt request can be enabled or disabled by means of bits TIE and RIE in SCR.

When the TDRE bit in SSR is set to 1, a TXI3 interrupt is requested. When the TEND bit in SSR is set to 1, a TEI3 interrupt is requested. These two interrupts are generated during transmission.

The initial value of the TDRE flag in SSR is 1. Thus, when the TIE bit in SCR is set to 1 before transferring the transmit data to TDR, a TXI3 interrupt request is generated even if the transmit data is not ready. The initial value of the TEND flag in SSR is 1. Thus, when the TEIE bit in SCR is set to 1 before transferring the transmit data to TDR, a TEI3 interrupt request is generated even if the transmit data has not been sent. It is possible to make use of the most of these interrupt requests efficiently by transferring the transmit data to TDR in the interrupt routine. To prevent the generation of these interrupt requests (TXI3 and TEI3), clear the enable bits (TIE and TEIE) that correspond to these interrupt requests to 0, after transferring the transmit data to TDR.

When the RDRF bit in SSR is set to 1, an RXI3 interrupt is requested, and if any of bits OER, PER, and FER is set to 1, an ERI3 interrupt is requested. These two interrupt requests are generated during reception.

The SCI3 can carry out continuous reception using an RXI3 and continuous transmission using a TXI3.

15.4.4 Communication Modes and Pin Functions

The SSU switches functions of the input/output pin in each communication mode according to the settings of the MSS bit in SSCRH and the RE and TE bits in SSER. Figure 15.2 shows the relationship between communication modes and the input/output pins. In bidirectional communication mode, neither TE nor RE should be set to 1.

Table 15.2 Relationship between Communication Modes and Input/Output Pins

Communication Mode	Register State					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clocked Synchronous Communication Mode	0	x	0	0	1	In	—	In
				1	0	—	Out	In
					1	In	Out	In
			1	0	1	In	—	Out
				1	0	—	Out	Out
					1	In	Out	Out
Four-Line Bus Communication Mode	1	0	0	0	1	—	In	In
				1	0	Out	—	In
					1	Out	In	In
			1	0	1	In	—	Out
				1	0	—	Out	Out
					1	In	Out	Out
Four-Line Bus (Bidirectional) Communication Mode	1	1	0	0	1	—	In	In
				1	0	—	Out	In
			1	0	1	—	In	Out
				1	0	—	Out	Out

[Legend] x: Don't care.
—: Can be used as a general I/O port.

15.4.8 Serial Data Transmission

Figure 15.11 shows an example of the SSU operation for transmission. In serial transmission, the SSU operates as described below.

When the SSU is set as a master device, it outputs a synchronous clock and data. When the SSU is set as a slave device, the $\overline{\text{SCS}}$ pin is in the low-input state and the SSU outputs data in synchronized with the input clock.

When the SSU writes transmit data in SSTDR after setting the TE bit to 1, the TDRE flag is automatically cleared to 0 and data is transferred from SSTDR to SSTRSR. Then the SSU sets the TDRE flag to 1 and starts transmission. If the TIE bit in SSER is set to 1 at this time, a TXI is generated.

When the TDRE flag is 0 and one frame of data has transferred, data is transferred from SSTDR to SSTRSR and serial transmission of the next frame is started. If the eighth bit is transmitted while the TDRE flag is 1, the TEND bit in SSSR is set to 1 and the state is retained. If the TEIE bit in SSER is set to 1 at this time, a TEI is generated. After transmission is ended, the SSCK pin is fixed high and the $\overline{\text{SCS}}$ pin goes high. When continuous transmission is performed with the $\overline{\text{SCS}}$ pin low, the next data should be written to SSTDR before transmitting the eighth bit of the frame.

While the ORER bit in SSSR is set to 1, transmission cannot be performed. Therefore confirm that the ORER bit is cleared to 0 before transmission.

The difference between this mode and clocked synchronous communication mode is as follows: when the SSU is set as a master device, the SSO pin is in the Hi-Z state if the $\overline{\text{SCS}}$ pin is in the Hi-Z state and when the SSU is set as a slave device, the SSI pin is in the Hi-Z state if the $\overline{\text{SCS}}$ pin is in the high-input state. The sample flowchart for serial data transmission is the same as that in clocked synchronous communication mode.

16.3.4 I²C Bus Interrupt Enable Register (ICIER)

ICIER enables or disables interrupt sources and acknowledge bits, sets acknowledge bits to be transferred, and confirms acknowledge bits to be received.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When the TDRE bit in ICSR is set to 1, this bit enables or disables the transmit data empty interrupt (TXI). 0: Transmit data empty interrupt request (TXI) is disabled. 1: Transmit data empty interrupt request (TXI) is enabled.
6	TEIE	0	R/W	Transmit End Interrupt Enable This bit enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Transmit end interrupt request (TEI) is disabled. 1: Transmit end interrupt request (TEI) is enabled.
5	RIE	0	R/W	Receive Interrupt Enable This bit enables or disables the receive data full interrupt request (RXI) and the overrun error interrupt request (ERI) with the clock synchronous format, when a receive data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Receive data full interrupt request (RXI) and overrun error interrupt request (ERI) with the clock synchronous format are disabled. 1: Receive data full interrupt request (RXI) and overrun error interrupt request (ERI) with the clock synchronous format are enabled.

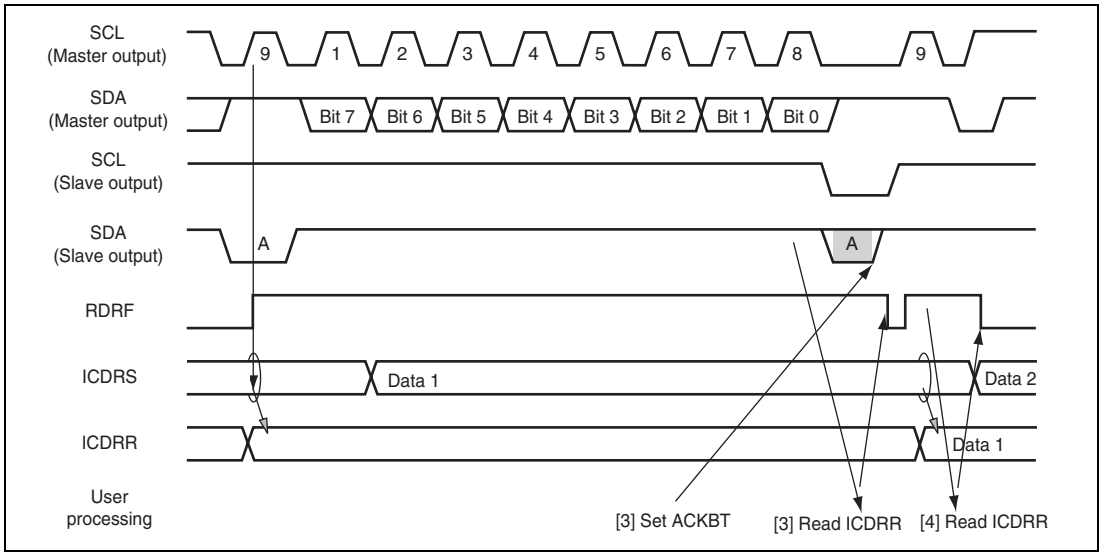


Figure 16.12 Slave Receive Mode Operation Timing (2)

16.4.6 Clock Synchronous Serial Format

This module can be operated with the clock synchronous serial format, by setting the FS bit in SAR to 1. When the MST bit in ICCR1 is 1, the transfer clock output from SCL is selected. When MST is 0, the external clock input is selected.

(1) Data Transfer Format

Figure 16.13 shows the clock synchronous serial transfer format.

The transfer data is output from the rise to the fall of the SCL clock, and the data at the rising edge of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in either the MSB first or LSB first. The output level of SDA can be changed during the transfer wait, by the SDAO bit in ICCR2.

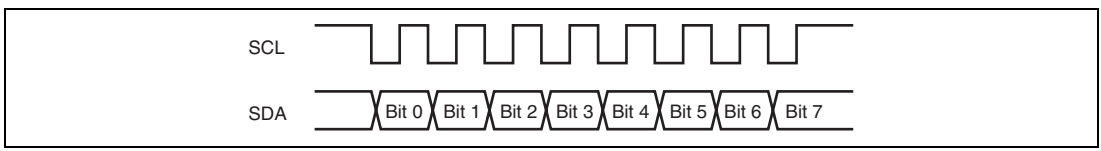


Figure 16.13 Clock Synchronous Serial Transfer Format

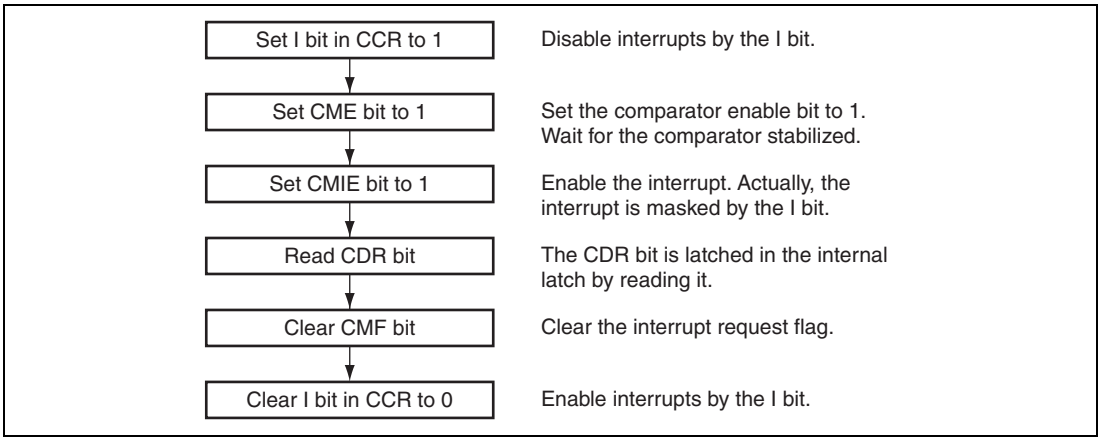


Figure 18.4 Procedure for Setting Interrupt (2)

18.5 Usage Notes

1. The COMP pin whose channel is operating as a comparator becomes a comparator analog input pin. It cannot be used for any other function.
2. When external input is used as the reference voltage (CMR0 = 1 or CMR1 = 1), the VCref pin cannot be used for any other function.
3. To stop the operation of a comparator, clear the CME0 and CME1 bits in CMCR0 and CMCR1 to 0, before clearing the COMPCKSTP bit in CKSTPR2 to 0.
4. If the LSI enters the standby mode or watch mode when a comparator is operating, the internal operation of the comparator is maintained. Since the comparator operates even in standby mode or watch mode, it returns to the same mode after the specified interrupt is canceled, though the current for the comparator is consumed.
   If a comparator is not required to return to the standby mode or watch mode when an interrupt is canceled and the current consumption needs to be reduced, stop the comparator by clearing the CME0 and CME1 bits in CMCR0 and CMCR1 to 0 before shifting the mode.

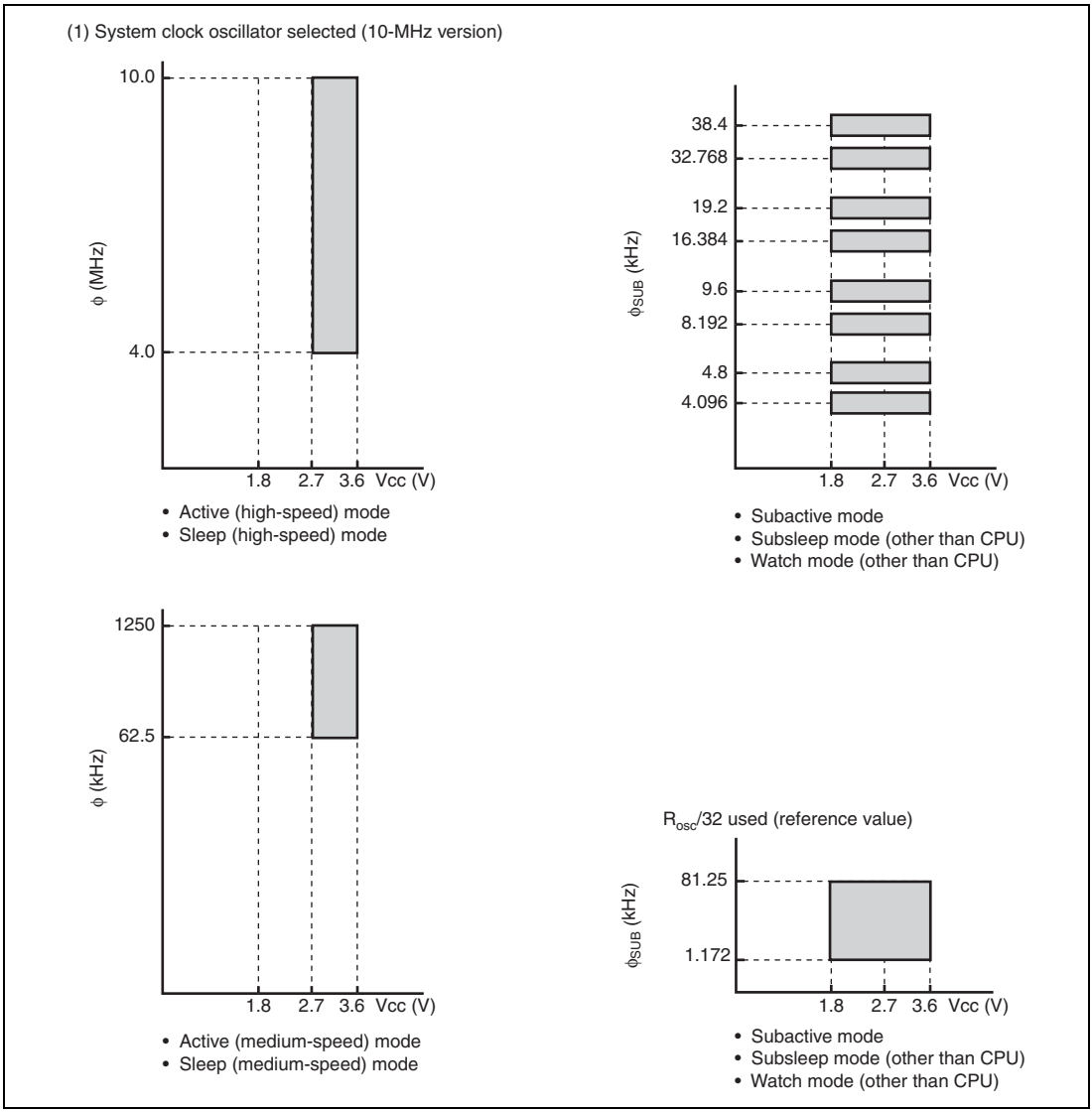
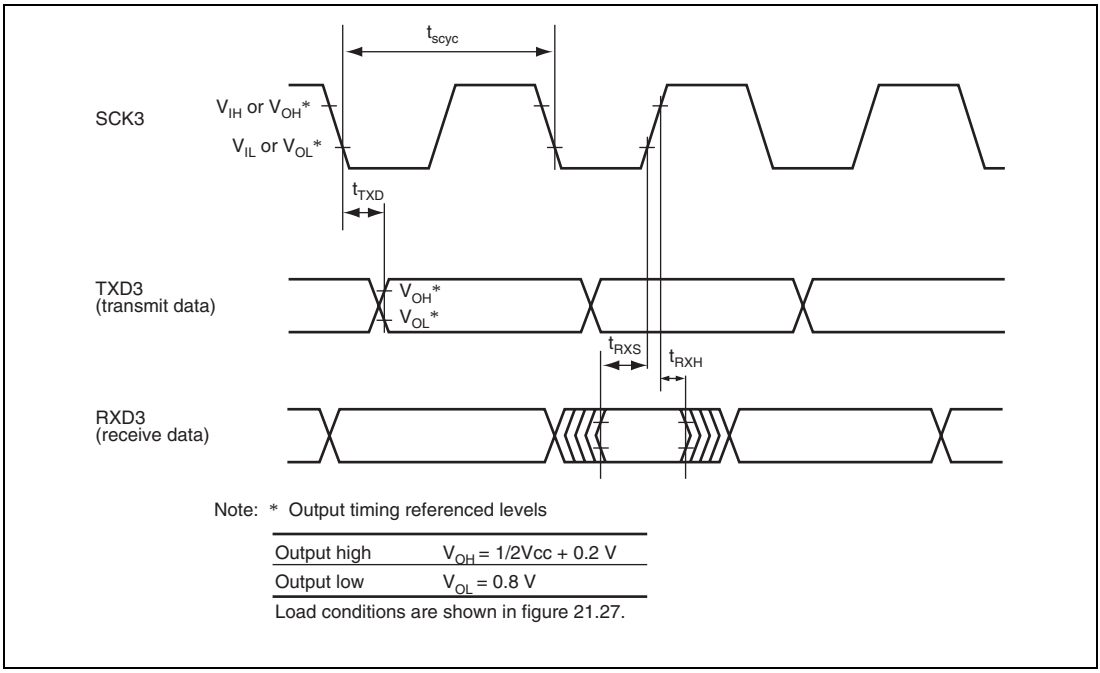


Figure 21.3 Power Supply Voltage and Operating Frequency Range (1)

Table 21.15 Serial Interface Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item		Symbol	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
Input clock cycle	Asynchronous	t_{scyc}		4	—	—	t_{cyc} or t_{subcyc}	Figure 21.18
	Clock synchronous			6	—	—		
Input clock pulse width		t_{SCKW}		0.4	—	0.6	t_{scyc}	Figure 21.18
Transmit data delay time (clock synchronous)		t_{TXD}		—	—	1	t_{cyc} or t_{subcyc}	Figure 21.19
Receive data setup time (clock synchronous)		t_{RXS}		400.0	—	—	ns	Figure 21.19
Receive data hold time (clock synchronous)		t_{RXH}		400.0	—	—	ns	Figure 21.19



Note: * Output timing referenced levels

Output high	V_{OH} = 1/2Vcc + 0.2 V
Output low	V_{OL} = 0.8 V

Load conditions are shown in figure 21.27.

Figure 21.19 SCI3 Input/Output Timing in Clock Synchronous Mode

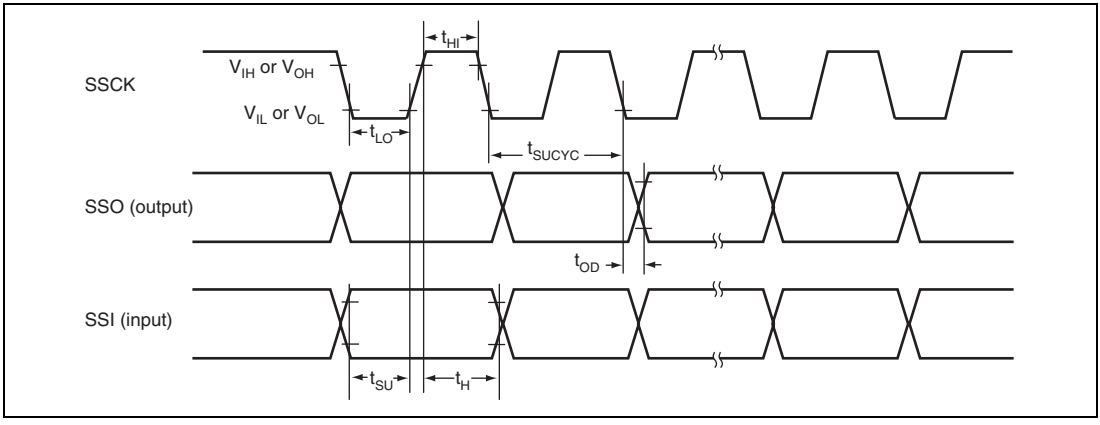


Figure 21.20 SSU Input/Output Timing in Clock Synchronous Mode

Table A.4 Number of Cycles in Each Instruction

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ADD	ADD.B #xx:8, Rd	1					
	ADD.B Rs, Rd	1					
	ADD.W #xx:16, Rd	2					
	ADD.W Rs, Rd	1					
	ADD.L #xx:32, ERd	3					
	ADD.L ERs, ERd	1					
ADDS	ADDS #1/2/4, ERd	1					
ADDX	ADDX #xx:8, Rd	1					
	ADDX Rs, Rd	1					
AND	AND.B #xx:8, Rd	1					
	AND.B Rs, Rd	1					
	AND.W #xx:16, Rd	2					
	AND.W Rs, Rd	1					
	AND.L #xx:32, ERd	3					
	AND.L ERs, ERd	2					
ANDC	ANDC #xx:8, CCR	1					
BAND	BAND #xx:3, Rd	1					
	BAND #xx:3, @ERd	2			1		
	BAND #xx:3, @aa:8	2			1		
Bcc	BRA d:8 (BT d:8)	2					
	BRN d:8 (BF d:8)	2					
	BHI d:8	2					
	BLS d:8	2					
	BCC d:8 (BHS d:8)	2					
	BCS d:8 (BLO d:8)	2					
	BNE d:8	2					
	BEQ d:8	2					
	BVC d:8	2					
	BVS d:8	2					
	BPL d:8	2					
	BMI d:8	2					
	BGE d:8	2					

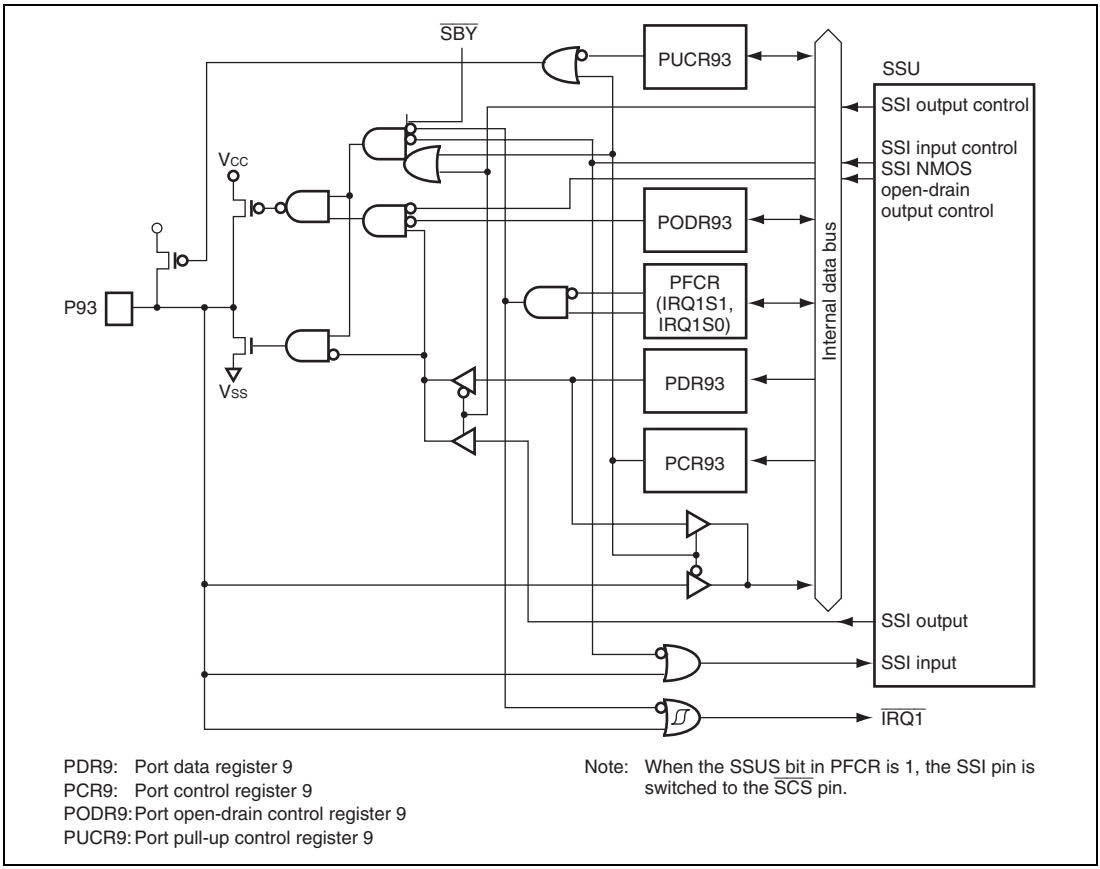


Figure B.4 (a) Port 9 Block Diagram (P93)