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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	4MHz
Connectivity	I²C, IrDA, SCI, SSU
Peripherals	POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN
Supplier Device Package	32-VQFN (5x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38602rft4wv

Tables

- Power-down state
  Transition to power-down state by SLEEP instruction

2.1 Address Space and Memory Map

The address space of this LSI is 64 Kbytes, which includes the program area and the data area. Figure 2.1 shows the memory map.

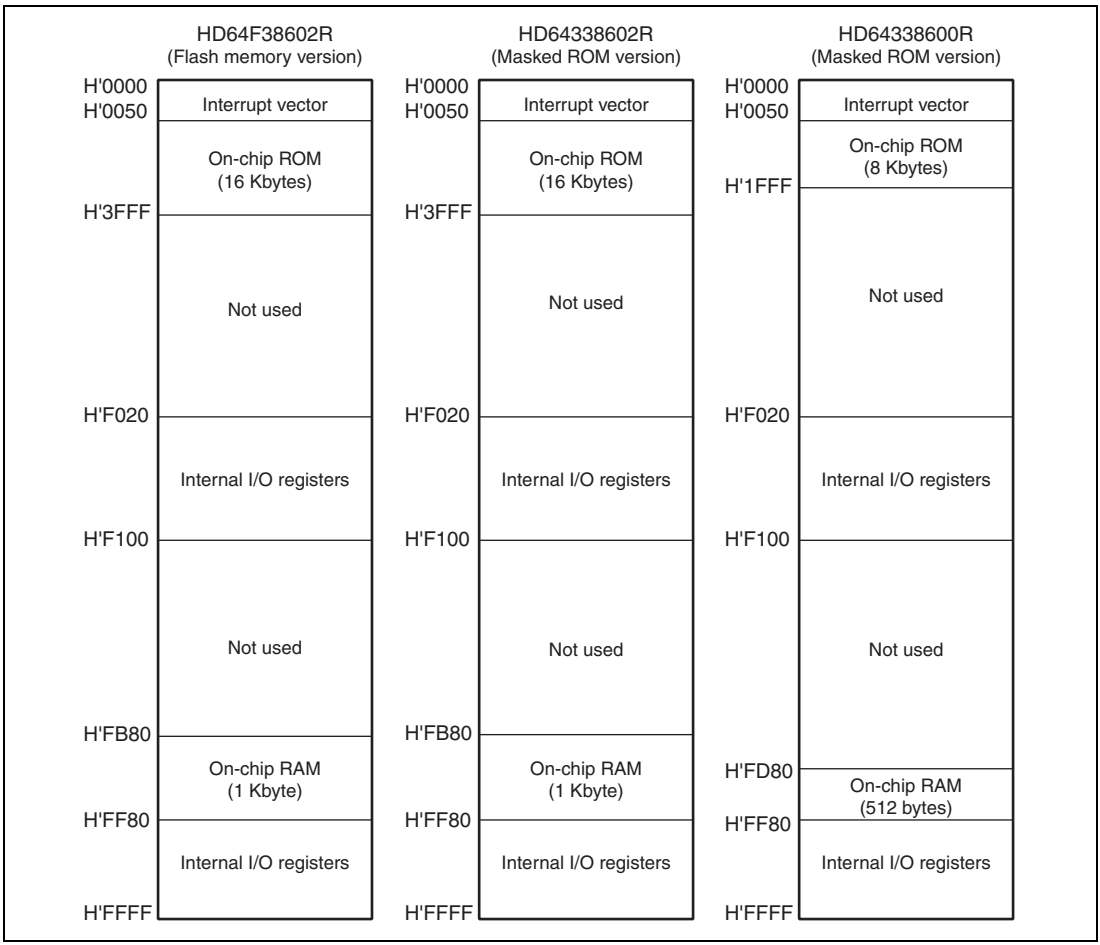


Figure 2.1 Memory Map

3.8 Usage Notes

3.8.1 Notes on Stack Area Use

When word data is accessed in this LSI, the least significant bit of the address is regarded as 0. Access to the stack always takes place in word size, so the stack pointer (SP: R7) should never indicate an odd address. To save register values, use PUSH.W Rn (MOV.W Rn, @–SP) or PUSH.L ERn (MOV.L ERn, @–SP). To restore register values, use POP.W Rn (MOV.W @SP+, Rn) or POP.L ERn (MOV.L @SP+, ERn).

Setting an odd address in SP may cause a program to crash. An example is shown in figure 3.6.

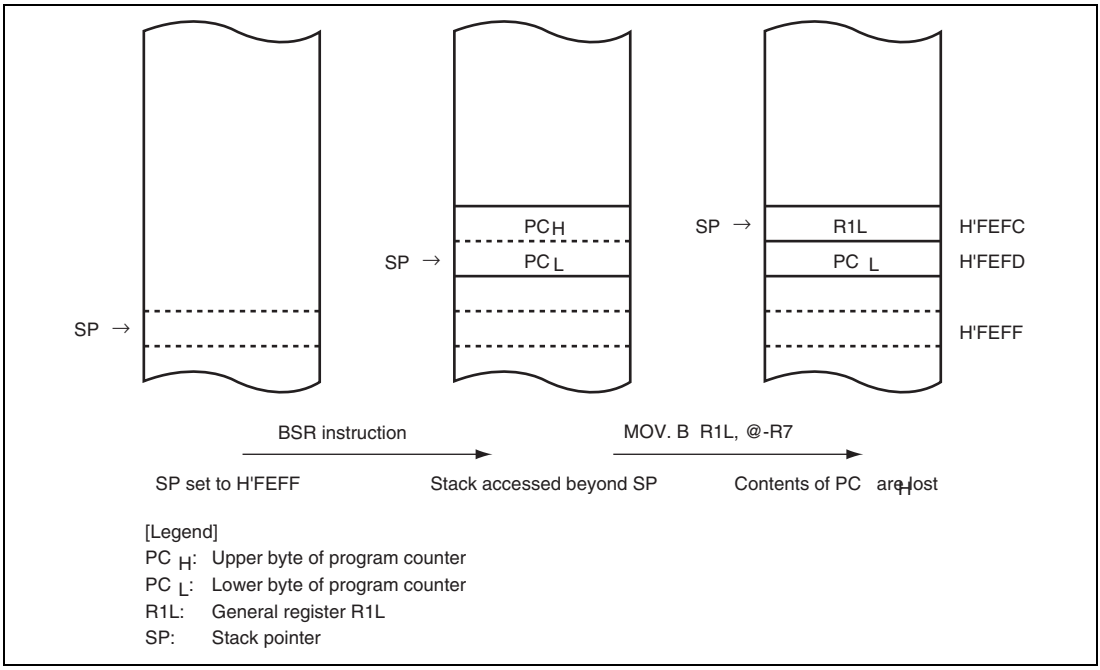


Figure 3.6 Operation when Odd Address is Set in SP

When CCR contents are saved to the stack during interrupt exception handling or restored when an RTE instruction is executed, this also takes place in word size. Both the upper and lower bytes of word data are saved to the stack; on return, the even address contents are restored to CCR while the odd address contents are ignored.

6.2.3 Erase Block Register 1 (EBR1)

EBR1 specifies the erase block of flash memory. EBR1 is initialized to H'00 when the SWE bit in FLMCR1 is 0. Do not set more than one bit at a time, as this will cause all the bits in EBR1 to be automatically cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	—	Reserved Although these bits are readable/writable, only 0 should be written to.
4	EB4	0	R/W	When this bit is set to 1, a12-Kbyte area of H'1000 to H'3FFF will be erased.
3	EB3	0	R/W	When this bit is set to 1, a 1-Kbyte area of H'0C00 to H'0FFF will be erased.
2	EB2	0	R/W	When this bit is set to 1, a 1-Kbyte area of H'0800 to H'0BFF will be erased.
1	EB1	0	R/W	When this bit is set to 1, a 1-Kbyte area of H'0400 to H'07FF will be erased.
0	EB0	0	R/W	When this bit is set to 1, a 1-Kbyte area of H'0000 to H'03FF will be erased.

6.2.4 Flash Memory Power Control Register (FLPWCR)

FLPWCR enables or disables a transition to the flash memory power-down mode when this LSI enters the subactive mode. There are two modes: mode in which operation of the power supply circuit of flash memory is partly halted in power-down mode and flash memory can be read, and mode in which even if a transition is made to subactive mode, operation of the power supply circuit of flash memory is retained and flash memory can be read.

Bit	Bit Name	Initial Value	R/W	Description
7	PDWND	0	R/W	Power-Down Disable When this bit is 0 and a transition is made to subactive mode, the flash memory enters the power-down mode. When this bit is 1, the flash memory remains in the normal mode even after a transition is made to subactive mode.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

Table 6.2 Boot Mode Operation

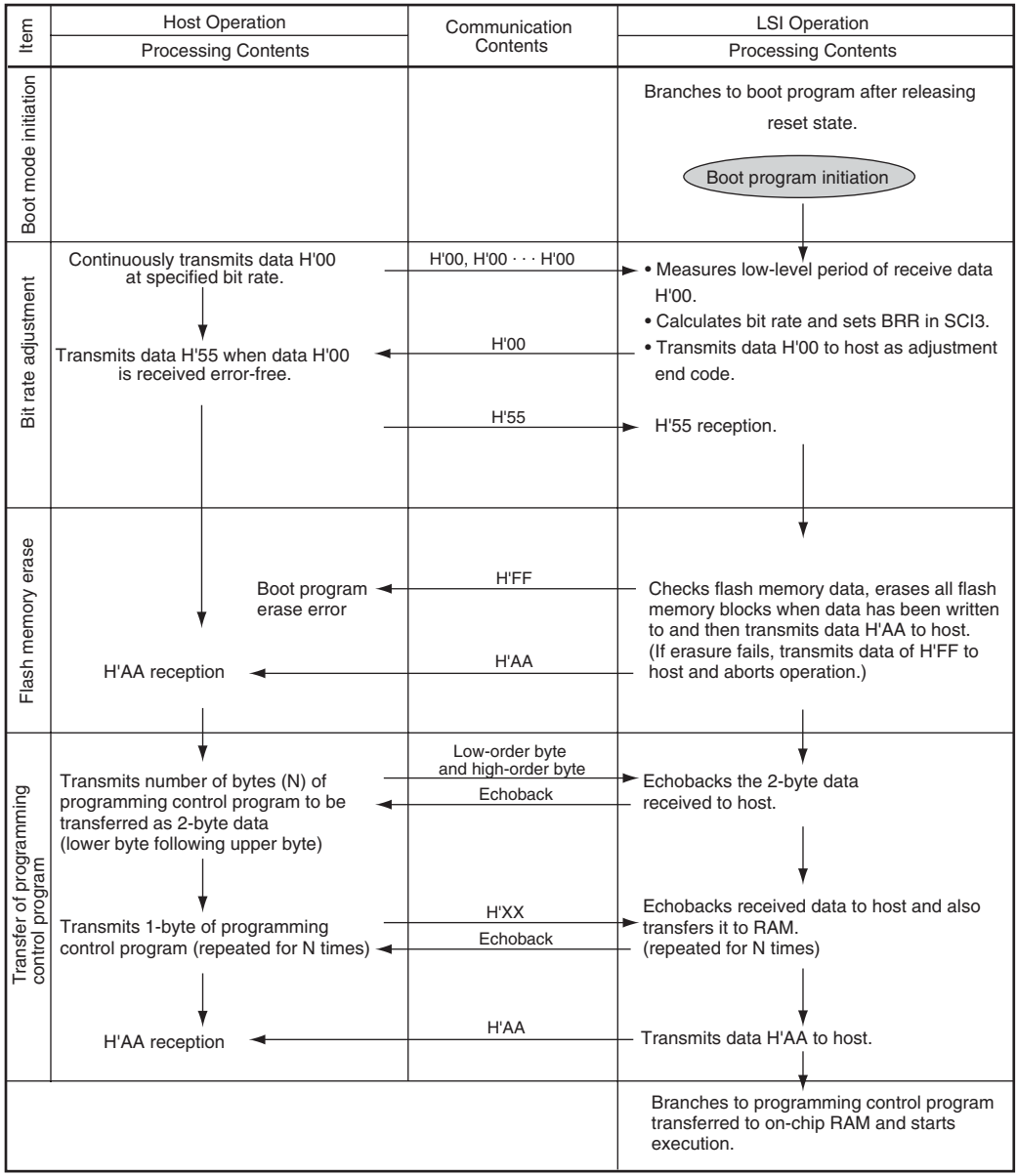


Table 6.3 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate is Possible

Host Bit Rate	System Clock Frequency Range of LSI
9,600 bps	8 to 10 MHz
4,800 bps	4 to 10 MHz
2,400 bps	2 to 10 MHz

6.3.2 Programming/Erasure in User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user programming/erasing control program. The user must prepare the settings for branching to the user programming/erasing control program and means to transfer programming data for on-board programming. The flash memory must contain the user programming/erasing control program or a program that transfer the user programming/erasing control program from external memory. Since the flash memory cannot be read during programming/erasure, transfer the user programming/erasing control program to on-chip RAM, as in boot mode. Figure 6.2 shows a sample procedure for programming/erasure in user program mode. Prepare a user programming/erasing control program in accordance with the description in section 6.4, Flash Memory Programming/Erasure.

The system clock oscillator must be used when programming or erasing the flash memory.

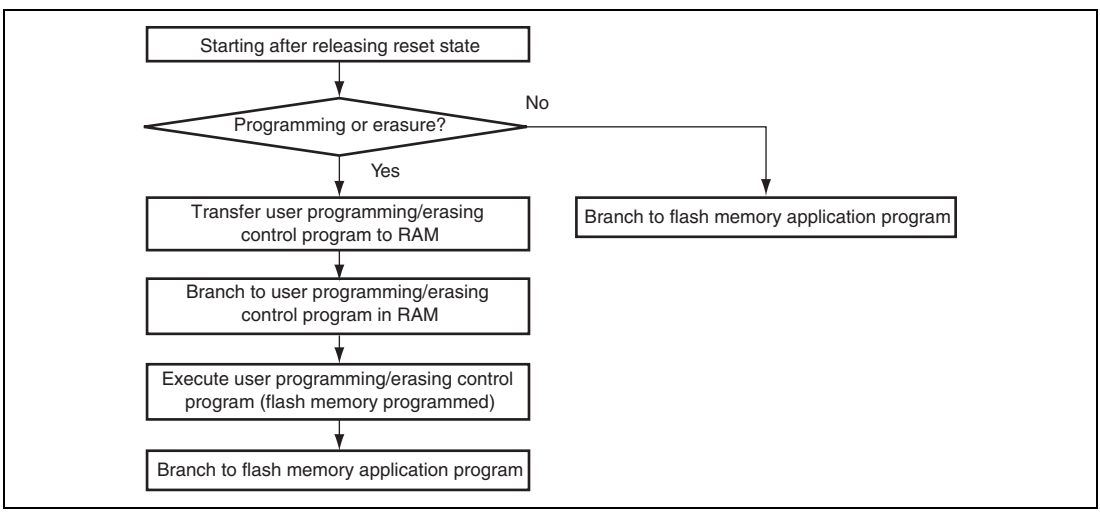


Figure 6.2 Programming/Erasing Flowchart Example in User Program Mode

8.3.5 Input Pull-Up MOS

Port 8 has an on-chip input pull-up MOS function that can be controlled by software. When a PCR8 bit is cleared to 0, setting the corresponding PUCR8 bit to 1 turns on the input pull-up MOS for that pin. The input pull-up MOS function is in the off state after a reset.

(n = 4 to 2)

PCR8n	0		1
PUCR8n	0	1	x
Input Pull-Up MOS	Off	On	Off

[Legend] x: Don't care.

8.4 Port 9

Port 9 is an I/O port also functioning as an SSU I/O pin, IIC2 I/O pin and interrupt pin. Figure 8.4 shows its pin configuration.

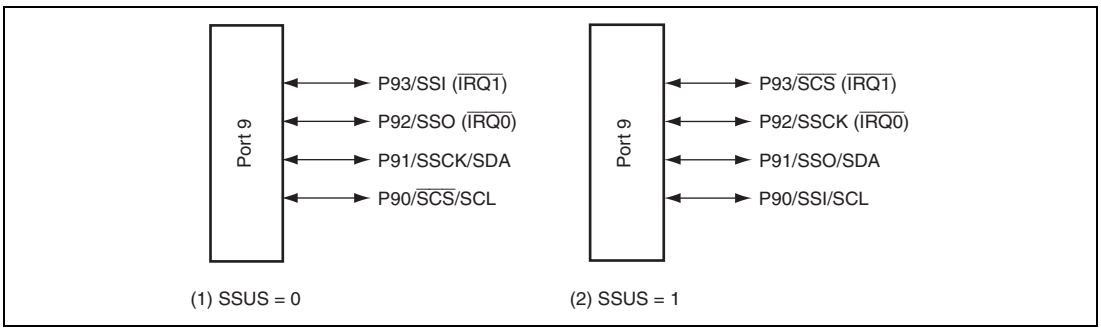


Figure 8.4 Port 9 Pin Configuration

Port 9 has the following registers.

- Port data register 9 (PDR9)
- Port control register 9 (PCR9)
- Port open-drain control register 9 (PODR9)
- Port pull-up control register 9 (PUCR9)

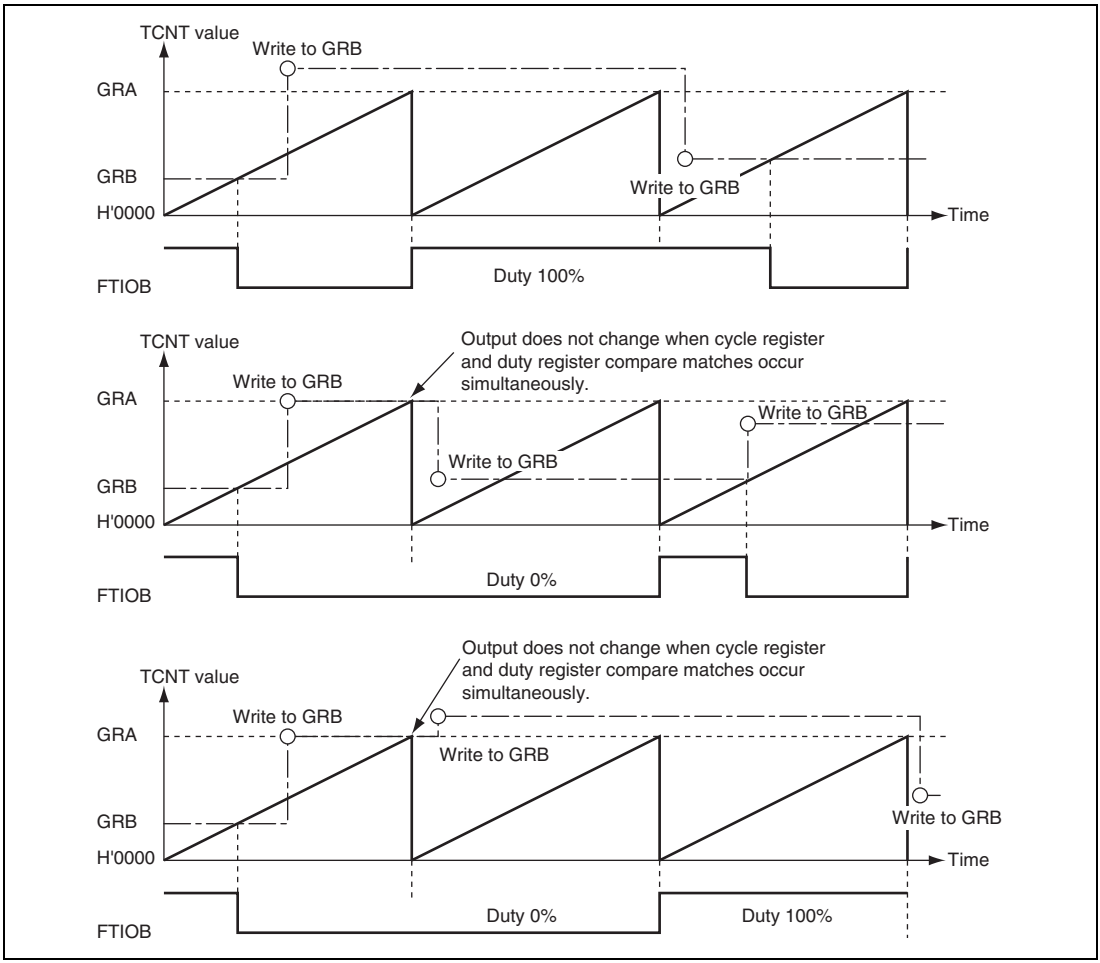


Figure 10.13 PWM Mode Example
(TOB, TOC, and TOD = 1: initial output values are set to 1)

Section 12 Watchdog Timer

This LSI incorporates the watchdog timer (WDT). The WDT is an 8-bit timer that can generate an internal reset signal if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow.

When this watchdog timer function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows.

12.1 Features

The WDT features are described below.

- Selectable from eleven counter input clocks
  Ten internal clock sources (ϕ/64, ϕ/128, ϕ/256, ϕ/512, ϕ/1024, ϕ/2048, ϕ/4096, ϕ/8192, ϕ_w/16, and ϕ_w/256) or the on-chip oscillator (R_{OSC}/2048) can be selected as the timer-counter clock.
- Watchdog timer mode
  If the counter overflows, this LSI is internally reset.
- Interval timer mode
  If the counter overflows, an interval timer interrupt is generated.
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (The WDT is operating as the initial value. For details, refer to section 5.4, Module Standby Function.)

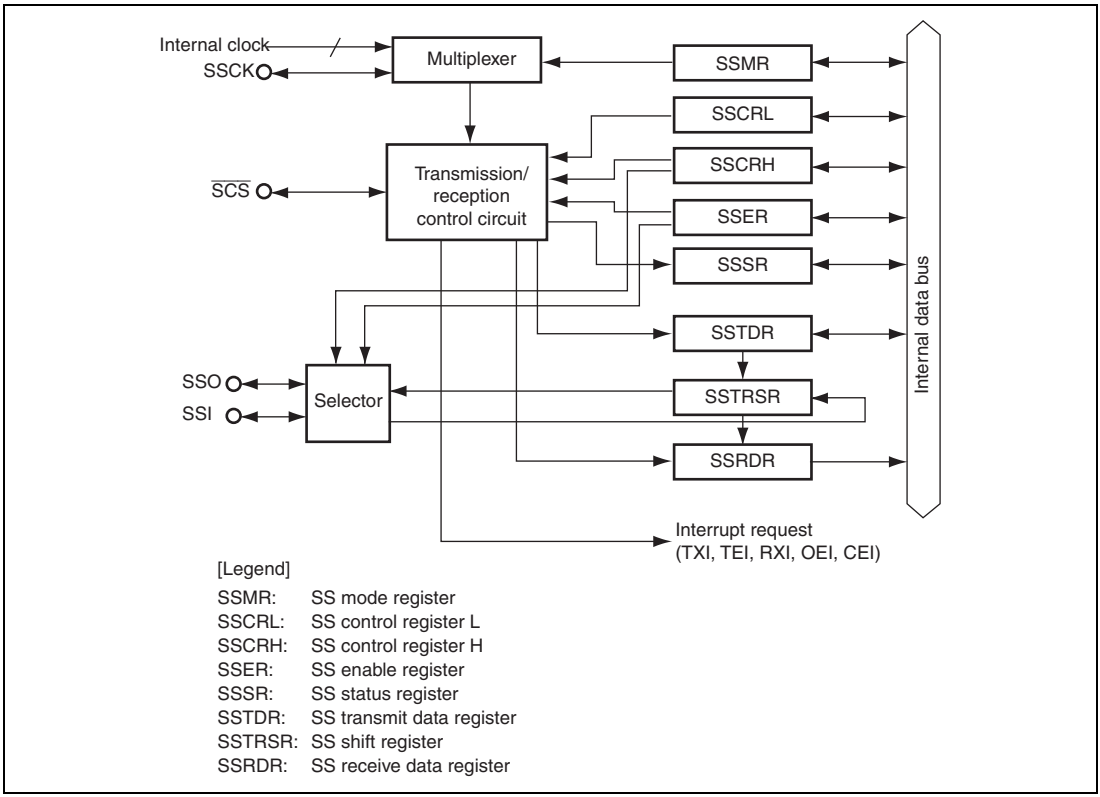


Figure 15.1 Block Diagram of SSU

15.2 Input/Output Pins

Table 15.1 shows the pin configuration of the SSU.

Table 15.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
SSU clock	SSCK	I/O	SSU clock input/output
SSU data input/output	SSI	I/O	SSU data input/output
SSU data input/output	SSO	I/O	SSU data input/output
SSU chip select input/output	$\overline{\text{SCS}}$	I/O	SSU chip select input/output

17.4.3 Operating States of A/D Converter

Table 17.2 shows the operating states of the A/D converter.

Table 17.2 Operating States of A/D Converter

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
AMR	Reset	Functions	Retained	Retained	Functions/ Retained*2	Retained	Retained	Retained
ADSR	Reset	Functions	Functions	Retained	Functions/ Retained*2	Functions/ Retained*2	Retained	Retained
ADRR	Retained*1	Functions	Functions	Retained	Functions/ Retained*2	Functions/ Retained*2	Retained	Retained

Notes: 1. Undefined at a power-on reset.
2. Function if ϕw/2 is selected as the internal clock. Halted and retained otherwise.

17.5 Example of Use

An example of how the A/D converter can be used is given below, using channel 1 (pin AN1) as the analog input channel. Figure 17.3 shows the operation timing.

1. Bits CH3 to CH0 in the A/D mode register (AMR) are set to 0101, making pin AN1 the analog input channel. A/D interrupts are enabled by setting bit IENAD to 1, and A/D conversion is started by setting bit ADSF to 1.
2. When A/D conversion is completed, bit IRRAD is set to 1, and the A/D conversion result is stored in ADRR. At the same time bit ADSF is cleared to 0, and the A/D converter goes to the idle state.
3. Bit IENAD = 1, so an A/D conversion end interrupt is requested.
4. The A/D interrupt handling routine starts.
5. The A/D conversion result is read and processed.
6. The A/D interrupt handling routine ends.

If bit ADSF is set to 1 again afterward, A/D conversion starts and steps 2 through 6 take place.

18.2 Input/Output Pins

Table 18.1 shows the pin configuration of the comparators.

Table 18.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
Comparator reference voltage	VCref	Input	Comparator reference voltage pin (external input)
Analog input channel 0	COMP0	Input	Comparator analog input pin 0
Analog input channel 1	COMP1	Input	Comparator analog input pin 1

18.3 Register Descriptions

The comparators have the following registers. For details on register addresses and register states during each processing, refer to section 20, List of Registers.

- Compare control registers 0, 1 (CMCR0, CMCR1)
- Compare data register (CMDR)

18.3.1 Compare Control Registers 0, 1 (CMCR0, CMCR1)

CMCR0 and CMCR1 control the comparators.

Bit	Bit Name	Initial Value	R/W	Description
7	CME	0	R/W	Comparator Enable 0: Comparator halted 1: Comparator operates
6	CMIE	0	R/W	Comparator Interrupt Enable 0: Disables a comparator interrupt 1: Enables a comparator interrupt
5	CMR	0	R/W	Comparator Reference Voltage Select 0: Selects internal power supply as reference voltage 1: Reference voltage is input from VCref pin For the combination of the CMR and CMLS bits.

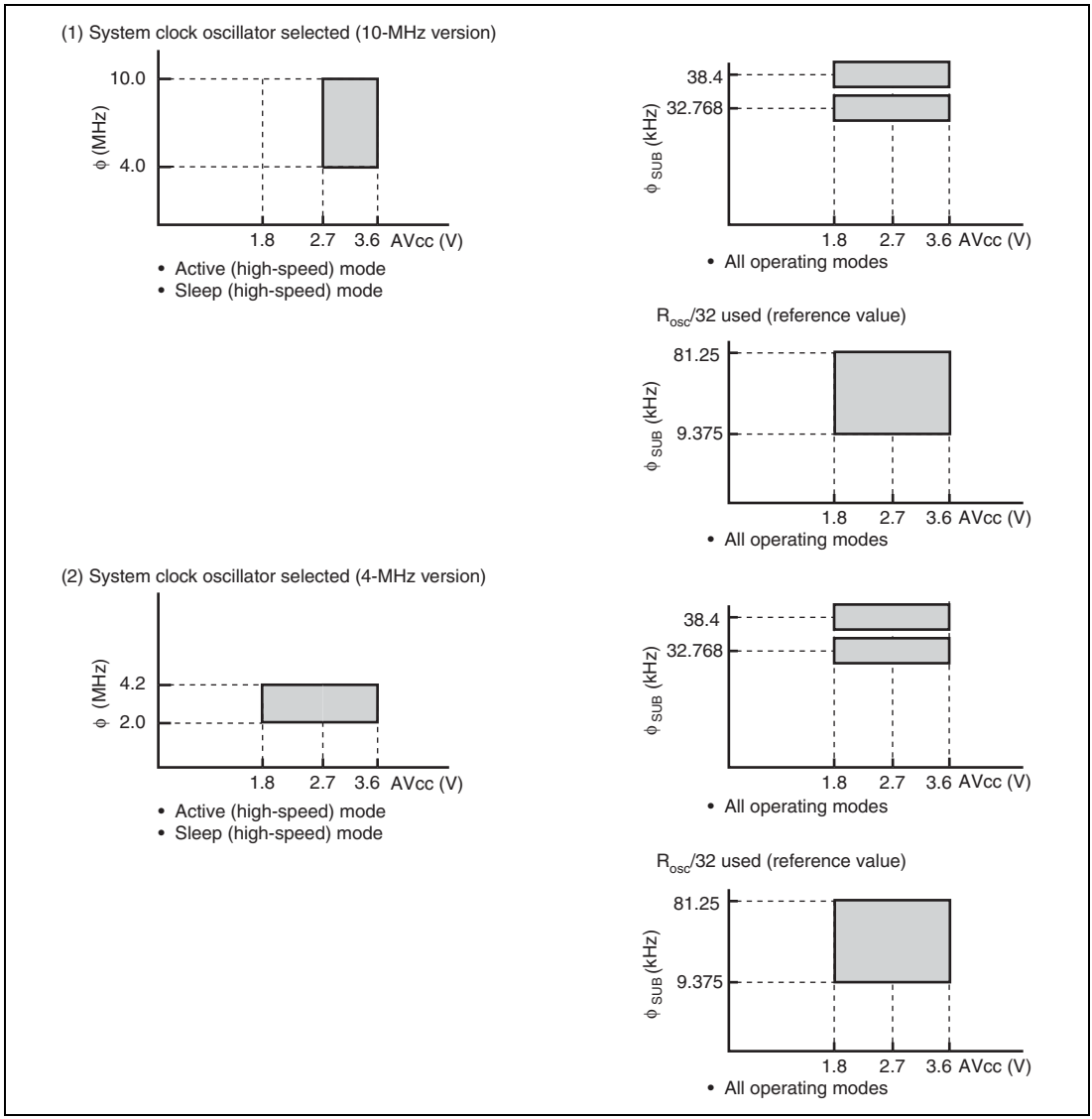


Figure 21.6 Analog Power Supply Voltage and Operating Frequency Range of A/D Converter (1)

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Subsleep mode supply current	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W/2)	—	3.5	—	µA	*1*2 Reference value
			V_{CC} = 2.7 V, on-chip oscillator/32 (ϕ_{SUB} = ϕ_W = R_{OSC}/32)	—	34	—		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator (ϕ_{SUB} = ϕ_W)	—	5.1	16.0		*1*2
Watch mode supply current	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator	—	0.5	—	µA	*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator	—	1.5	5.0		*1*2
Standby mode supply current	I_{STBY}	V_{CC}	V_{CC} = 3.0 V, Ta = 25°C, 32-kHz crystal resonator not used	—	0.1	—	µA	*1*2 Reference value
			32-kHz crystal resonator not used	—	1.0	5.0		*1*2
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	—	—	V	
Permissible output low current (per pin)	I_{OL}	Output pins except port 8		—	—	0.5	mA	
		Port 8		—	—	15.0		
Permissible output low current (total)	ΣI_{OL}	Output pins except port 8		—	—	20.0	mA	
		Port 8		—	—	45.0		

Table 21.4 Serial Interface Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, unless otherwise specified.

Item		Symbol	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
Input clock cycle	Asynchronous	t_{scyc}		4	—	—	t_{cyc} or t_{subcyc}	Figure 21.18
	Clock synchronous			6	—	—		
Input clock pulse width		t_{SCKW}		0.4	—	0.6	t_{scyc}	Figure 21.18
Transmit data delay time (clock synchronous)		t_{TXD}		—	—	1	t_{cyc} or t_{subcyc}	Figure 21.19
Receive data setup time (clock synchronous)		t_{RXS}		400.0	—	—	ns	Figure 21.19
Receive data hold time (clock synchronous)		t_{RXH}		400.0	—	—	ns	Figure 21.19

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Active mode supply current	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.1	—	mA	Max. guideline = 1.1 × typ. *1*2
			Active (medium-speed) mode, V_{CC} = 3 V, f_{OSC} = 4.2 MHz, ϕ_{osc}/64	—	0.3	0.5		*1*2 4-MHz version
			Active (medium-speed) mode, V_{CC} = 3 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	0.5	0.7		*1*2 10-MHz version
Sleep mode supply current	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.3	—	mA	Max. guideline = 1.1 × typ. *1*2
			V_{CC} = 3 V, f_{OSC} = 4.2 MHz	—	1.0	1.5		*1*2 4-MHz version
			V_{CC} = 3 V, f_{OSC} = 10 MHz	—	1.8	2.7		*1*2 10-MHz version
Subactive mode supply current	I_{SUB}	V_{CC}	V_{CC} = 1.8 V, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/2$)	—	4.0	—	µA	*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/8$)	—	3.6	—		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W/2$)	—	7.4	—		*1*2 Reference value
			V_{CC} = 2.7 V, on-chip oscillator/32 ($\phi_{SUB} = \phi_W = R_{OSC}/32$)	—	40	—		*1*2 Reference value
			V_{CC} = 2.7 V, 32-kHz crystal resonator ($\phi_{SUB} = \phi_W$)	—	13	25		*1*2

Appendix

A. Instruction Set

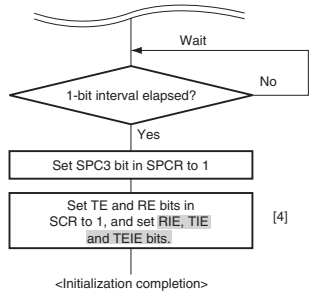
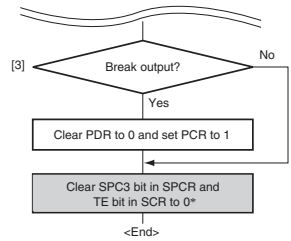
A.1 Instruction List

Condition Code

Symbol	Description
Rd	General destination register
Rs	General source register
Rn	General register
ERd	General destination register (address register or 32-bit register)
ERs	General source register (address register or 32-bit register)
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
PC	Program counter
SP	Stack pointer
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
disp	Displacement
→	Transfer from the operand on the left to the operand on the right, or transition from the state on the left to the state on the right
+	Addition of the operands on both sides
–	Subtraction of the operand on the right from the operand on the left
×	Multiplication of the operands on both sides
÷	Division of the operand on the left by the operand on the right
∧	Logical AND of the operands on both sides
∨	Logical OR of the operands on both sides
⊕	Logical exclusive OR of the operands on both sides
¬	NOT (logical complement)
( ), < >	Contents of operand

Note: General registers include 8-bit registers (R0H to R7H and R0L to R7L) and 16-bit registers (R0 to R7 and E0 to E7).

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
BIOR	BIOR #xx:3, Rd	1					
	BIOR #xx:3, @ERd	2			1		
	BIOR #xx:3, @aa:8	2			1		
BIST	BIST #xx:3, Rd	1					
	BIST #xx:3, @ERd	2			2		
	BIST #xx:3, @aa:8	2			2		
BIXOR	BIXOR #xx:3, Rd	1					
	BIXOR #xx:3, @ERd	2			1		
	BIXOR #xx:3, @aa:8	2			1		
BLD	BLD #xx:3, Rd	1					
	BLD #xx:3, @ERd	2			1		
	BLD #xx:3, @aa:8	2			1		
BNOT	BNOT #xx:3, Rd	1					
	BNOT #xx:3, @ERd	2			2		
	BNOT #xx:3, @aa:8	2			2		
	BNOT Rn, Rd	1					
	BNOT Rn, @ERd	2			2		
	BNOT Rn, @aa:8	2			2		
BOR	BOR #xx:3, Rd	1					
	BOR #xx:3, @ERd	2			1		
	BOR #xx:3, @aa:8	2			1		
BSET	BSET #xx:3, Rd	1					
	BSET #xx:3, @ERd	2			2		
	BSET #xx:3, @aa:8	2			2		
	BSET Rn, Rd	1					
	BSET Rn, @ERd	2			2		
	BSET Rn, @aa:8	2			2		
BSR	BSR d:8	2		1			
	BSR d:16	2		1			2
BST	BST #xx:3, Rd	1					
	BST #xx:3, @ERd	2			2		
	BST #xx:3, @aa:8	2			2		

Item	Page	Revisions (See Manual for Details)
Figure 14.4 Sample SCI3 Initialization Flowchart	258	Modified  [[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Setting bits TE and RE enables the TXD3 and RXD3 pins to be used. Also set the RIE, TIE, and TEIE bits, depending on whether interrupts are required. In asynchronous mode, the bits are marked at transmission and idled at reception to wait for the start bit.
Figure 14.6 Sample Serial Transmission Flowchart (Asynchronous Mode)	260	Modified  [3] To output a break in serial transmission, after setting PCR to 1 and PDR to 0, clear the SPC3 bit in SPCR and the TE bit in SCR to 0. Note: * When the SPC3 bit in SPCR is cleared to 0, the pin functions as an I/O port.
14.5 Operation in Clock Synchronous Mode	264	Deleted … After 8-bit data is output, the transmission line holds the MSB state. In clock synchronous mode, no parity ~~or multiprocessor~~ bit is added.
14.6 Multiprocessor Communication Function	270	This section is deleted.